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#### Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2012-20e-so

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2.3 Divide Support

The dsPIC DSC devices feature a 16/16-bit signed fractional divide operation, as well as 32/16-bit and 16/16-bit signed and unsigned integer divide operations, in the form of single instruction iterative divides. The following instructions and data sizes are supported:

- 1. DIVF 16/16 signed fractional divide
- 2. DIV.sd 32/16 signed divide
- 3. DIV.ud 32/16 unsigned divide
- 4. DIV.s 16/16 signed divide
- 5. DIV.u 16/16 unsigned divide

The 16/16 divides are similar to the 32/16 (same number of iterations), but the dividend is either zero-extended or sign-extended during the first iteration.

The divide instructions must be executed within a REPEAT loop. Any other form of execution (e.g., a series of discrete divide instructions) will not function correctly because the instruction flow depends on RCOUNT. The divide instruction does not automatically set up the RCOUNT value and it must, therefore, be explicitly and correctly specified in the REPEAT instruction, as shown in Table 2-1 (REPEAT executes the target instruction {operand value+1} times). The REPEAT loop count must be setup for 18 iterations of the DIV/DIVF instruction. Thus, a complete divide operation requires 19 cycles.

**Note:** The divide flow is interruptible; however, the user needs to save the context as appropriate.

#### TABLE 2-1: DIVIDE INSTRUCTIONS

Instruction	Function
DIVF	Signed fractional divide: Wm/Wn $\rightarrow$ W0; Rem $\rightarrow$ W1
DIV.sd	Signed divide: (Wm+1:Wm)/Wn $\rightarrow$ W0; Rem $\rightarrow$ W1
DIV.s	Signed divide: Wm/Wn $\rightarrow$ W0; Rem $\rightarrow$ W1
DIV.ud	Unsigned divide: (Wm+1:Wm)/Wn $\rightarrow$ W0; Rem $\rightarrow$ W1
DIV.u	Unsigned divide: Wm/Wn $\rightarrow$ W0; Rem $\rightarrow$ W1

# dsPIC30F2011/2012/3012/3013



### 3.2.2 DATA SPACES

The X data space is used by all instructions and supports all addressing modes. There are separate read and write data buses. The X read data bus is the return data path for all instructions that view data space as combined X and Y address space. It is also the X address space data path for the dual operand read instructions (MAC class). The X write data bus is the only write path to data space for all instructions.

The X data space also supports Modulo Addressing for all instructions, subject to Addressing mode restrictions. Bit-Reversed Addressing is only supported for writes to X data space.

The Y data space is used in concert with the X data space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths. No writes occur across the Y bus. This class of instructions dedicates two W register pointers, W10 and W11, to always address Y data space, independent of X data space, whereas W8 and W9 always address X data space. Note that during accumulator write back, the data address space is considered a combination of X and Y data spaces, so the write occurs across the X bus. Consequently, the write can be to any address in the entire data space.

The Y data space can only be used for the data prefetch operation associated with the MAC class of instructions. It also supports Modulo Addressing for automated circular buffers. Of course, all other instructions can access the Y data address space through the X data path as part of the composite linear space.

The boundary between the X and Y data spaces is defined as shown in Figure 3-7 and is not user programmable. Should an EA point to data outside its own assigned address space, or to a location outside physical memory, an all zero word/byte is returned. For example, although Y address space is visible by all non-MAC instructions using any addressing mode, an attempt by a MAC instruction to fetch data from that space using W8 or W9 (X space pointers) returns 0x0000.

#### TABLE 3-2: EFFECT OF INVALID MEMORY ACCESSES

Attempted Operation	Data Returned
EA = an unimplemented address	0x0000
W8 or W9 used to access Y data space in a MAC instruction	0x0000
W10 or W11 used to access X data space in a MAC instruction	0x0000

All Effective Addresses are 16 bits wide and point to bytes within the data space. Therefore, the data space address range is 64 Kbytes or 32K words.

## 3.2.3 DATA SPACE WIDTH

The core data width is 16 bits. All internal registers are organized as 16-bit wide words. Data space memory is organized in byte addressable, 16-bit wide blocks.

### 3.2.4 DATA ALIGNMENT

To help maintain backward compatibility with PIC® MCU devices and improve data space memory usage efficiency, the dsPIC30F instruction set supports both word and byte operations. Data is aligned in data memory and registers as words, but all data space EAs resolve to bytes. Data byte reads read the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the X data path (no byte accesses are possible from the Y data path as the MAC class of instruction can only fetch words). That is, data memory and registers are organized as two parallel byte wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register which matches the byte address.

As a consequence of this byte accessibility, all Effective Address calculations (including those generated by the DSP operations which are restricted to word-sized data) are internally scaled to step through word-aligned memory. For example, the core would recognize that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care should be taken when mixing byte and word operations, or translating from 8-bit MCU code. Should a misaligned read or write be attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed, whereas if it occurred on a write, the instruction is executed, but the write does not occur. In either case, a trap is then executed, allowing the system and/or user to examine the machine state prior to execution of the address fault.

#### FIGURE 3-9: DATA ALIGNMENT

	15 <b>MSB</b>	8 7	LSB	0	
0001	Byte 1		Byte 0		0000
0003	Byte 3		Byte 2		0002
0005	Byte 5		Byte 4		0004

#### 4.2.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and an ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 3-3).

Note:	Υ	space	Modulo	Addressing	EA
	cal	culations	assume	word-sized	data
	(LS				

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding Start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

#### 4.2.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags as well as a W register field to specify the W address registers. The XWM and YWM fields select which registers operate with Modulo Addressing. If XWM = 15, X RAGU and X WAGU Modulo Addressing is disabled. Similarly, if YWM = 15, Y AGU Modulo Addressing is disabled.

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 3-3). Modulo Addressing is enabled for X data space when XWM is set to any value other than '15' and the XMODEN bit is set at MODCON<15>.

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y data space when YWM is set to any value other than '15' and the YMODEN bit is set at MODCON<14>.

### FIGURE 4-1: MODULO ADDRESSING OPERATION EXAMPLE



## 6.0 DATA EEPROM MEMORY

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "dsPIC30F Family Reference Manual" (DS70046). For more information on the device instruction set and programming, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

The data EEPROM memory is readable and writable during normal operation over the entire VDD range. The data EEPROM memory is directly mapped in the program memory address space.

The four SFRs used to read and write the program Flash memory are used to access data EEPROM memory, as well. As described in **Section 5.5 "Control Registers"**, these registers are:

- NVMCON
- NVMADR
- NVMADRU
- NVMKEY

The EEPROM data memory allows read and write of single words and 16-word blocks. When interfacing to data memory, NVMADR, in conjunction with the NVMADRU register, are used to address the EEPROM location being accessed. TBLRDL and TBLWTL instructions are used to read and write data EEPROM. The dsPIC30F devices have up to 8 Kbytes (4K words) of data EEPROM with an address range from 0x7FF000 to 0x7FFFFE.

A word write operation should be preceded by an erase of the corresponding memory location(s). The write typically requires 2 ms to complete, but the write time varies with voltage and temperature. A program or erase operation on the data EEPROM does not stop the instruction flow. The user is responsible for waiting for the appropriate duration of time before initiating another data EEPROM write/ erase operation. Attempting to read the data EEPROM while a programming or erase operation is in progress results in unspecified data.

Control bit WR initiates write operations similar to program Flash writes. This bit cannot be cleared, only set, in software. They are cleared in hardware at the completion of the write operation. The inability to clear the WR bit in software prevents the accidental or premature termination of a write operation.

The WREN bit, when set, allows a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location. The address register NVMADR remains unchanged.

Note: Interrupt flag bit NVMIF in the IFS0 register is set when write is complete. It must be cleared in software.

## 6.1 Reading the Data EEPROM

A TBLRD instruction reads a word at the current program word address. This example uses W0 as a pointer to data EEPROM. The result is placed in register W4 as shown in Example 6-1.

#### EXAMPLE 6-1: DATA EEPROM READ

MOV	#LOW_ADDR_WORD,W0	;	Init	Point	ter
MOV	<pre>#HIGH_ADDR_WORD,W1</pre>				
MOV	W1,TBLPAG				
TBLRDL	[ WO ], W4	;	read	data	EEPROM

#### TABLE 7-1: PORTB REGISTER MAP FOR dsPIC30F2011/3012

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		Reset	State	
TRISB	02C6	—	—	—	—	—		—	—	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	0000	0000	1111	1111
PORTB	02C8	_	_	_	_	_	_	_	_	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	0000	0000	0000	0000
LATB	02CB	_	_	_	_	_	_		_	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000	0000	0000	0000

Legend: — = unimplemented bit, read as '0'

#### TABLE 7-2: PORTB REGISTER MAP FOR dsPIC30F2012/3013

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISB	02C6	_	—	_	—	—	_	TRISB9	TRISB8	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	0000 0011 1111 1111
PORTB	02C8	_	_	_	_	—	_	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	0000 0000 0000 0000
LATB	02CB		_		-	-		LATB9	LATB8	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

#### TABLE 7-3: PORTC REGISTER MAP FOR dsPIC30F2011/2012/3012/3013

SFR Nam	e Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISC	02CC	TRISC15	TRISC14	TRISC13	-	-	-	_	-	-	-	-	—	_	—	—	_	1110 0000 0000 0000
PORTO	02CE	RC15	RC14	RC13	_	—	—	_	—	_	-	—	_	_	_	_	_	0000 0000 0000 0000
LATC	02D0	LATC15	LATC14	LATC13	-	_	_	_	—	_	-	—	_	_	_	_	_	0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

#### TABLE 7-4: PORTD REGISTER MAP FOR dsPIC30F2011/3012

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISD	02D2	-	-	—	_	-	_	—	_	-		_		_	_		TRISD0	0000 0000 0000 0000
PORTD	02D4	_	_	_	—	—	_	_	—	—	—	—	_	—	_	_	RD0	0000 0000 0000 0000
LATD	02D6	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	LATD0	0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

## 8.0 INTERRUPTS

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "dsPIC30F Family Reference Manual" (DS70046). For more information on the device instruction set and programming, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

The dsPIC30F sensor family has up to 21 interrupt sources and 4 processor exceptions (traps) which must be arbitrated based on a priority scheme.

The CPU is responsible for reading the Interrupt Vector Table (IVT) and transferring the address contained in the interrupt vector to the program counter. The interrupt vector is transferred from the program data bus into the program counter via a 24-bit wide multiplexer on the input of the program counter.

The Interrupt Vector Table (IVT) and Alternate Interrupt Vector Table (AIVT) are placed near the beginning of program memory (0x000004). The IVT and AIVT are shown in Figure 8-1.

The interrupt controller is responsible for pre-processing the interrupts and processor exceptions before they are presented to the processor core. The peripheral interrupts and traps are enabled, prioritized and controlled using centralized Special Function Registers (SFRs):

- IFS0<15:0>, IFS1<15:0>, IFS2<15:0> All interrupt request flags are maintained in these three registers. The flags are set by their respective peripherals or external signals and they are cleared via software.
- IEC0<15:0>, IEC1<15:0>, IEC2<15:0> All interrupt enable control bits are maintained in these three registers. These control bits are used to individually enable interrupts from the peripherals or external signals.
- IPC0<15:0> through IPC10<7:0> The user assignable priority level associated with each of these 41 interrupts is held centrally in these eleven registers.
- IPL<3:0> The current CPU priority level is explicitly stored in the IPL bits. IPL<3> is present in the CORCON register, whereas IPL<2:0> are present in the STATUS register (SR) in the processor core.

- INTCON1<15:0>, INTCON2<15:0> Global interrupt control functions are derived from these two registers. INTCON1 contains the control and status flags for the processor exceptions. The INTCON2 register controls the external interrupt request signal behavior and the use of the alternate vector table.
  - Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

All interrupt sources can be user assigned to one of 7 priority levels, 1 through 7, through the IPCx registers. Each interrupt source is associated with an interrupt vector, as shown in Table 8-1. Levels 7 and 1 represent the highest and lowest maskable priorities, respectively.

Note: Assigning a priority level of '0' to an interrupt source is equivalent to disabling that interrupt.

If the NSTDIS bit (INTCON1<15>) is set, nesting of interrupts is prevented. Thus, if an interrupt is currently being serviced, processing of a new interrupt is prevented even if the new interrupt is of higher priority than the one currently being serviced.

Note: The IPL bits become read-only whenever the NSTDIS bit has been set to '1'.

Certain interrupts have specialized control bits for features like edge or level triggered interrupts, interrupt-on-change, etc. Control of these features remains within the peripheral module which generates the interrupt.

The DISI instruction can be used to disable the processing of interrupts of priorities 6 and lower for a certain number of instructions, during which the DISI bit (INTCON2<14>) remains set.

When an interrupt is serviced, the PC is loaded with the address stored in the vector location in program memory that corresponds to the interrupt. There are 63 different vectors within the IVT (refer to Table 8-1). These vectors are contained in locations 0x000004 through 0x0000FE of program memory (refer to Table 8-1). These locations contain 24-bit addresses, and in order to preserve robustness, an address error trap takes place if the PC attempts to fetch any of these words during normal execution. This prevents execution of random data as a result of accidentally decrementing a PC into vector space, accidentally mapping a data space address into vector space, or the PC rolling over to 0x000000 after reaching the end of implemented program memory space. Execution of a GOTO instruction to this vector space also generates an address error trap.

## 8.1 Interrupt Priority

The user-assignable interrupt priority bits (IP<2:0>) for each individual interrupt source are located in the LS 3 bits of each nibble within the IPCx register(s). Bit 3 of each nibble is not used and is read as a '0'. These bits define the priority level assigned to a particular interrupt by the user.

Note:	The user-assignable priority levels start at
	0 as the lowest priority and level 7 as the
	highest priority.

Natural Order Priority is determined by the position of an interrupt in the vector table, and only affects interrupt operation when multiple interrupts with the same user-assigned priority become pending at the same time.

Table 8-1 lists the interrupt numbers and interrupt sources for the dsPIC30F2011/2012/3012/3013 devices and their associated vector numbers.

- **Note 1:** The natural order priority scheme has 0 as the highest priority and 53 as the lowest priority.
  - **2:** The natural order priority number is the same as the INT number.

The ability for the user to assign every interrupt to one of seven priority levels means that the user can assign a very high overall priority level to an interrupt with a low natural order priority. For example, the PLVD (Low Voltage Detect) can be given a priority of 7. The INTO (External Interrupt 0) may be assigned to priority level 1, thus giving it a very low effective priority.

#### TABLE 8-1:INTERRUPT VECTOR TABLE

Interrupt Number	Vector Number	Interrupt Source						
	Highest I	Natural Order Priority						
0	8	INT0 – External Interrupt 0						
1	9	IC1 – Input Capture 1						
2	10	OC1 – Output Compare 1						
3	11	T1 – Timer 1						
4	12	IC2 – Input Capture 2						
5	13	OC2 – Output Compare 2						
6	14	T2 – Timer2						
7	15	T3 – Timer3						
8	16	SPI1						
9	17	U1RX – UART1 Receiver						
10	18	U1TX – UART1 Transmitter						
11	19	ADC – ADC Convert Done						
12	20	NVM – NVM Write Complete						
13	21	SI2C – I <sup>2</sup> C <sup>™</sup> Slave Interrupt						
14	22	MI2C – I <sup>2</sup> C Master Interrupt						
15	23	Input Change Interrupt						
16	24	INT1 – External Interrupt 1						
17-22	25-30	Reserved						
23	31	INT2 – External Interrupt 2						
24	32	U2RX <sup>(1)</sup> – UART2 Receiver						
25	33	U2TX <sup>(1)</sup> – UART2 Transmitter						
26-41	34-49	Reserved						
42	50	LVD – Low-Voltage Detect						
43-53	51-61	Reserved						
Lowest Natural Order Priority								

Note 1: Only the dsPIC30F3013 has UART2 and the U2RX, U2TX interrupts. These locations are reserved for the dsPIC30F2011/2012/3012.

## dsPIC30F2011/2012/3012/3013

NOTES:

### 12.4.2 PWM PERIOD

The PWM period is specified by writing to the PRx register. The PWM period can be calculated using Equation 12-1.

#### EQUATION 12-1:

 $PWM \ period = [(PRx) + 1] \cdot 4 \cdot Tosc \cdot$  $(TMRx \ prescale \ value)$ 

PWM frequency is defined as 1/[PWM period].

When the selected TMRx is equal to its respective period register, PRx, the following four events occur on the next increment cycle:

- TMRx is cleared.
- The OCx pin is set.
  - Exception 1: If PWM duty cycle is 0x0000, the OCx pin remains low.
  - Exception 2: If duty cycle is greater than PRx, the pin remains high.
- The PWM duty cycle is latched from OCxRS into OCxR.
- The corresponding timer interrupt flag is set.

See Figure 12-2 for key PWM period comparisons. Timer3 is referred to in Figure 12-2 for clarity.



## 12.5 Output Compare Operation During CPU Sleep Mode

When the CPU enters Sleep mode, all internal clocks are stopped. Therefore, when the CPU enters the Sleep state, the output compare channel drives the pin to the active state that was observed prior to entering the CPU Sleep state.

For example, if the pin was high when the CPU entered the Sleep state, the pin remains high. Likewise, if the pin was low when the CPU entered the Sleep state, the pin remains low. In either case, the output compare module resumes operation when the device wakes up.

### 12.6 Output Compare Operation During CPU Idle Mode

When the CPU enters the Idle mode, the output compare module can operate with full functionality.

The output compare channel operates during the CPU Idle mode if the OCSIDL bit (OCxCON<13>) is at logic '0' and the selected time base (Timer2 or Timer3) is enabled and the TSIDL bit of the selected timer is set to logic '0'.

## 12.7 Output Compare Interrupts

The output compare channels have the ability to generate an interrupt on a compare match, for whichever Match mode has been selected.

For all modes except the PWM mode, when a compare event occurs, the respective interrupt flag (OCxIF) is asserted and an interrupt is generated if enabled. The OCxIF bit is located in the corresponding IFS register and must be cleared in software. The interrupt is enabled via the respective compare interrupt enable (OCxIE) bit located in the corresponding IEC Control register.

For the PWM mode, when an event occurs, the respective timer interrupt flag (T2IF or T3IF) is asserted and an interrupt is generated if enabled. The IF bit is located in the IFS0 register and must be cleared in software. The interrupt is enabled via the respective timer interrupt enable bit (T2IE or T3IE) located in the IEC0 Control register. The output compare interrupt flag is never set during the PWM mode of operation.

## TABLE 14-2: I<sup>2</sup>C REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
I2CRCV	0200		—			_		—	Receive Register						0000 0000 0000 0000			
I2CTRN	0202	_	_	_	_	-	_	_	— — Transmit Register						0000 0000 1111 1111			
I2CBRG	0204	_	_	_	_	-	_	_	Baud Rate Generator						0000 0000 0000 0000			
I2CCON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0001 0000 0000 0000
I2CSTAT	0208	ACKSTAT	TRSTAT	_	_	-	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000 0000 0000 0000
I2CADD	020A	_	—	_		_	_	Address Register						0000 0000 0000 0000				

Legend: — = unimplemented bit, read as '0'

Note: Refer to the "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

## 16.1 A/D Result Buffer

The module contains a 16-word dual port read-only buffer, called ADCBUF0...ADCBUFF, to buffer the A/D results. The RAM is 12 bits wide but the data obtained is represented in one of four different 16-bit data formats. The contents of the sixteen A/D Conversion Result Buffer registers, ADCBUF0 through ADCBUFF, cannot be written by user software.

## 16.2 Conversion Operation

After the ADC module has been configured, the sample acquisition is started by setting the SAMP bit. Various sources, such as a programmable bit, timer time-outs and external events, will terminate acquisition and start a conversion. When the A/D conversion is complete, the result is loaded into ADCBUF0...ADCBUFF, and the DONE bit and the A/D interrupt flag, ADIF, are set after the number of samples specified by the SMPI bit. The ADC module can be configured for different interrupt rates as described in Section 16.3 "Selecting the Conversion Sequence".

The following steps should be followed for doing an A/D conversion:

- 1. Configure the ADC module:
  - Configure analog pins, voltage reference and digital I/O
  - Select A/D input channels
  - Select A/D conversion clock
  - Select A/D conversion trigger
  - Turn on ADC module
- 2. Configure A/D interrupt (if required):
  - Clear ADIF bit
  - Select A/D interrupt priority
- 3. Start sampling
- 4. Wait the required acquisition time
- 5. Trigger acquisition end, start conversion
- 6. Wait for A/D conversion to complete, by either:
  - Waiting for the A/D interrupt, or
  - Waiting for the DONE bit to get set
- 7. Read A/D result buffer; clear ADIF if required

### 16.3 Selecting the Conversion Sequence

Several groups of control bits select the sequence in which the A/D connects inputs to the sample/hold channel, converts a channel, writes the buffer memory and generates interrupts.

The sequence is controlled by the sampling clocks.

The SMPI bits select the number of acquisition/conversion sequences that would be performed before an interrupt occurs. This can vary from 1 sample per interrupt to 16 samples per interrupt.

The BUFM bit will split the 16-word results buffer into two 8-word groups. Writing to the 8-word buffers will be alternated on each interrupt event.

Use of the BUFM bit will depend on how much time is available for the moving of the buffers after the interrupt.

If the processor can quickly unload a full buffer within the time it takes to acquire and convert one channel, the BUFM bit can be '0' and up to 16 conversions (corresponding to the 16 input channels) may be done per interrupt. The processor will have one acquisition and conversion time to move the sixteen conversions.

If the processor cannot unload the buffer within the acquisition and conversion time, the BUFM bit should be '1'. For example, if SMPI<3:0> (ADCON2<5:2>) = 0111, then eight conversions will be loaded into 1/2 of the buffer, following which an interrupt occurs. The next eight conversions will be loaded into the other 1/2 of the buffer. The processor will have the entire time between interrupts to move the eight conversions.

The ALTS bit can be used to alternate the inputs selected during the sampling sequence. The input multiplexer has two sets of sample inputs: MUX A and MUX B. If the ALTS bit is '0', only the MUX A inputs are selected for sampling. If the ALTS bit is '1' and SMPI<3:0> = 0000 on the first sample/convert sequence, the MUX A inputs are selected and on the next acquire/convert sequence, the MUX B inputs are selected.

The CSCNA bit (ADCON2<10>) will allow the multiplexer input to be alternately scanned across a selected number of analog inputs for the MUX A group. The inputs are selected by the ADCSSL register. If a particular bit in the ADCSSL register is '1', the corresponding input is selected. The inputs are always scanned from lower to higher numbered inputs, starting after each interrupt. If the number of inputs selected is greater than the number of samples taken per interrupt, the higher numbered inputs are unused.

## dsPIC30F2011/2012/3012/3013

Any interrupt that is individually enabled (using the corresponding IE bit) and meets the prevailing priority level will be able to wake-up the processor. The processor will process the interrupt and branch to the ISR. The Sleep Status bit in the RCON register is set upon wake-up.

Note: In spite of various delays applied (TPOR, TLOCK and TPWRT), the crystal oscillator (and PLL) may not be active at the end of the time-out (e.g., for low-frequency crystals). In such cases, if FSCM is enabled, then the device will detect this as a clock failure and process the clock failure trap, the FRC oscillator will be enabled and the user will have to re-enable the crystal oscillator. If FSCM is not enabled, then the device will simply suspend execution of code until the clock is stable and will remain in Sleep until the oscillator clock has started.

All Resets will wake-up the processor from Sleep mode. Any Reset, other than POR, will set the Sleep Status bit. In a POR, the Sleep bit is cleared.

If the Watchdog Timer is enabled, then the processor will wake-up from Sleep mode upon WDT time-out. The Sleep and WDTO Status bits are both set.

## 17.6.2 IDLE MODE

In Idle mode, the clock to the CPU is shut down while peripherals keep running. Unlike Sleep mode, the clock source remains active.

Several peripherals have a control bit in each module that allows them to operate during Idle.

LPRC Fail-Safe Clock remains active if clock failure detect is enabled.

The processor wakes up from Idle if at least one of the following conditions has occurred:

- any interrupt that is individually enabled (IE bit is '1') and meets the required priority level
- any Reset (POR, BOR, MCLR)
- WDT time-out

Upon wake-up from Idle mode, the clock is re-applied to the CPU and instruction execution begins immediately, starting with the instruction following the PWRSAV instruction.

Any interrupt that is individually enabled (using IE bit) and meets the prevailing priority level will be able to wake-up the processor. The processor will process the interrupt and branch to the ISR. The Idle Status bit in the RCON register is set upon wake-up.

Any Reset other than POR will set the Idle Status bit. On a POR, the Idle bit is cleared.

If Watchdog Timer is enabled, then the processor will wake-up from Idle mode upon WDT time-out. The Idle and WDTO Status bits are both set.

Unlike wake-up from Sleep, there are no time delays involved in wake-up from Idle.

## 17.7 Device Configuration Registers

The Configuration bits in each device Configuration register specify some of the device modes and are programmed by a device programmer, or by using the In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) feature of the device. Each device Configuration register is a 24-bit register, but only the lower 16 bits of each register are used to hold configuration data. There are five device Configuration registers available to the user:

- 1. FOSC (0xF80000): Oscillator Configuration Register
- 2. FWDT (0xF80002): Watchdog Timer Configuration Register
- 3. FBORPOR (0xF80004): BOR and POR Configuration Register
- 4. FGS (0xF8000A): General Code Segment Configuration Register
- 5. FICD (0xF8000C): Debug Configuration Register

The placement of the Configuration bits is automatically handled when you select the device in your device programmer. The desired state of the Configuration bits may be specified in the source code (dependent on the language tool used), or through the programming interface. After the device has been programmed, the application software may read the Configuration bit values through the table read instructions. For additional information, please refer to the Programming Specifications of the device.

Note: If the code protection Configuration fuse bits (FGS<GCP> and FGS<GWRP>) have been programmed, an erase of the entire code-protected device is only possible at voltages  $VDD \ge 4.5V$ .

# dsPIC30F2011/2012/3012/3013

	L 10-2.				-		n
Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycle s	Status Flags Affected
9	BTG	BTG	f,#bit4	Bit Toggle f	1	1	None
		BTG	Ws,#bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC	f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC	Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS	f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS	Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST	f,#bit4	Bit Test f	1	1	Z
		BTST.C	Ws,#bit4	Bit Test Ws to C	1	1	С
		BTST.Z	Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C	Ws,Wb	Bit Test Ws <wb> to C</wb>	1	1	С
		BTST.Z	Ws,Wb	Bit Test Ws <wb> to Z</wb>	1	1	Z
13	BTSTS	BTSTS	f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C	Ws,#bit4	Bit Test Ws to C, then Set	1	1	С
		BTSTS.Z	Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL	lit23	Call subroutine	2	2	None
		CALL	Wn	Call indirect subroutine	1	2	None
15	CLR	CLR	f	f = 0x0000	1	1	None
		CLR	WREG	WRFG = 0x0000	1	1	None
		CLR	Ws	$W_{S} = 0x0000$	1	1	None
		CLR	Acc Wx Wxd Wy Wyd AWB	Clear Accumulator	1	1	
16		CLRWDT		Clear Watchdog Timer	1	1	WDTO Sleep
17	COM	COM	f	$f - \overline{f}$	1	1	N 7
	00101	COM	f WREC	WREG $-\overline{f}$	1	1	N Z
		COM	We Wd	Wd = Ws	1	1	N Z
18	CP	CD	f		1	1	
10		CP	1 Wb #1;+5	Compare Wb with lit5	1	1	
		CP	Wb,#1105	Compare Wb with Wc (Wb _ Wc)	1	1	
10	CDO	CP CD0	MD, WS	Compare f with 0x0000	1	1	
19	CFU	CPU	L	Compare Wa with 0x0000	1	1	
20	CDR	CPU	WS £	Compare fixith WREC, with Porrow	1	1	
20	CFD	CPB		Compare What with Life with Derrow	1	1	
		CPB	WD,#11t5	Compare Wb with IIIS, with Borrow	1	1	
		СЪВ	WD,WS	(Wb - Ws - C)	1		C,DC,N,OV,Z
21	CPSEQ	CPSEQ	Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
22	CPSGT	CPSGT	Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
23	CPSLT	CPSLT	Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
24	CPSNE	CPSNE	Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
25	DAW	DAW	Wn	Wn = decimal adjust Wn	1	1	С
26	DEC	DEC	f	f = f -1	1	1	C,DC,N,OV,Z
		DEC	f,WREG	WREG = f -1	1	1	C,DC,N,OV,Z
		DEC	Ws,Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
27	DEC2	DEC2	f	f = f -2	1	1	C,DC,N,OV,Z
		DEC2	f,WREG	WREG = f -2	1	1	C,DC,N,OV,Z
		DEC2	Ws,Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
28	DISI	DISI	#lit14	Disable Interrupts for k instruction cycles	1	1	None

### TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)

## 19.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC<sup>®</sup> DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

#### 19.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC<sup>®</sup> Flash MCUs and dsPIC<sup>®</sup> Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

#### 19.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC<sup>®</sup> Flash microcontrollers and dsPIC<sup>®</sup> DSCs with the powerful, yet easyto-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 19.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC<sup>®</sup> and dsPIC<sup>®</sup> Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming<sup>™</sup>.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 19.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit<sup>™</sup> 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit<sup>™</sup> 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 19.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 19.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM<sup>™</sup> and dsPICDEM<sup>™</sup> demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ<sup>®</sup> security ICs, CAN, IrDA<sup>®</sup>, PowerSmart battery management, SEEVAL<sup>®</sup> evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

DC CHA	ARACTER	Standard Operating Conditions: 2.5V to 5.5V         (unless otherwise stated)         Operating temperature       -40°C ≤TA ≤+85°C for Industrial         -40°C ≤TA ≤+125°C for Extended							
Param No.	Symbol	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions		
	Vol	Output Low Voltage <sup>(2)</sup>							
DO10		I/O ports	—	—	0.6	V	Iol = 8.5 mA, Vdd = 5V		
			—	—	0.15	V	IOL = 2.0 mA, VDD = 3V		
DO16		OSC2/CLKO	—	—	0.6	V	IOL = 1.6 mA, VDD = 5V		
		(RC or EC Osc mode)	—	—	0.72	V	IOL = 2.0 mA, VDD = 3V		
	Voh	Output High Voltage <sup>(2)</sup>							
DO20		I/O ports	Vdd - 0.7	—	—	V	Iон = -3.0 mA, Vdd = 5V		
			Vdd - 0.2	—	—	V	Iон = -2.0 mA, Vdd = 3V		
DO26		OSC2/CLKO	Vdd - 0.7	—	—	V	IOH = -1.3 mA, VDD = 5V		
		(RC or EC Osc mode)	Vdd - 0.1	—	—	V	Iон = -2.0 mA, Vdd = 3V		
		Capacitive Loading Specs on Output Pins <sup>(2)</sup>							
DO50	Cosc2	OSC2/SOSC2 pin	_	_	15	pF	In XTL, XT, HS and LP modes when external clock is used to drive OSC1.		
DO56	Cio	All I/O pins and OSC2	_	—	50	pF	RC or EC Osc mode		
DO58	Св	SCL, SDA	_	—	400	pF	In I <sup>2</sup> C mode		
<b>Note 1:</b> Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and									

#### TABLE 20-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

are not tested.2: These parameters are characterized but not tested in manufacturing.

DC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V         (unless otherwise stated)         Operating temperature       -40°C ≤TA ≤+85°C for Industrial         -40°C ≤TA ≤+125°C for Extended						
Param No.	Symbol	Characteristic	Min	Typ <sup>(1)</sup>	Max	Units	Conditions			
		Data EEPROM Memory <sup>(2)</sup>								
D120	ED	Byte Endurance	100K	1M	—	E/W	-40° C ≤TA ≤+85°C			
D121	Vdrw	VDD for Read/Write	Vmin	_	5.5	V	Using EECON to Read/Write VMIN = Minimum operating voltage			
D122	TDEW	Erase/Write Cycle Time	0.8	2	2.6	ms	RTSP			
D123	Tretd	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated			
D124	IDEW	IDD During Programming	—	10	30	mA	Row Erase			
		Program Flash Memory <sup>(2)</sup>								
D130	Eр	Cell Endurance	10K	100K	—	E/W	-40° C ≤TA ≤+85°C			
D131	Vpr	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage			
D132	VEB	VDD for Bulk Erase	4.5		5.5	V				
D133	VPEW	VDD for Erase/Write	3.0		5.5	V				
D134	TPEW	Erase/Write Cycle Time	0.8	2	2.6	ms	RTSP			
D135	Tretd	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated			
D137	IPEW	IDD During Programming	—	10	30	mA	Row Erase			
D138	IEB	IDD During Programming	—	10	30	mA	Bulk Erase			

#### TABLE 20-12: DC CHARACTERISTICS: PROGRAM AND EEPROM

Note 1: Data in "Typ" column is at 5V,  $25^{\circ}$ C unless otherwise stated.

2: These parameters are characterized but not tested in manufacturing.

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