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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	20
Program Memory Size	12KB (4K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f2012-20i-sp

NOTES:

dsPIC30F2011/2012/3012/3013

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	Description
SCL	I/O	ST	Synchronous serial clock input/output for I ² C™.
SDA	I/O	ST	Synchronous serial data input/output for I ² C.
SOSCO	O	—	32 kHz low-power oscillator crystal output.
SOSCI	I	ST/CMOS	32 kHz low-power oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
T1CK	I	ST	Timer1 external clock input.
T2CK	I	ST	Timer2 external clock input.
U1RX	I	ST	UART1 Receive.
U1TX	O	—	UART1 Transmit.
U1ARX	I	ST	UART1 Alternate Receive.
U1ATX	O	—	UART1 Alternate Transmit.
U2RX	I	ST	UART2 Receive.
U2TX	O	—	UART2 Transmit.
VDD	P	—	Positive supply for logic and I/O pins.
VSS	P	—	Ground reference for logic and I/O pins.
VREF+	I	Analog	Analog Voltage Reference (High) input.
VREF-	I	Analog	Analog Voltage Reference (Low) input.

Legend: CMOS = CMOS compatible input or output Analog = Analog input
ST = Schmitt Trigger input with CMOS levels O = Output
I = Input P = Power

3.1.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

This architecture fetches 24-bit wide program memory. Consequently, instructions are always aligned. However, as the architecture is modified Harvard, data can also be present in program space.

There are two methods by which program space can be accessed: via special table instructions, or through the remapping of a 16K word program space page into the upper half of data space (see **Section 3.1.2 “Data Access from Program Memory Using Program Space Visibility”**). The **TBLRD** and **TBLWT** instructions offer a direct method of reading or writing the lsw of any address within program space, without going through data space. The **TBLRDH** and **TBLWTH** instructions are the only method whereby the upper 8 bits of a program space word can be accessed as data.

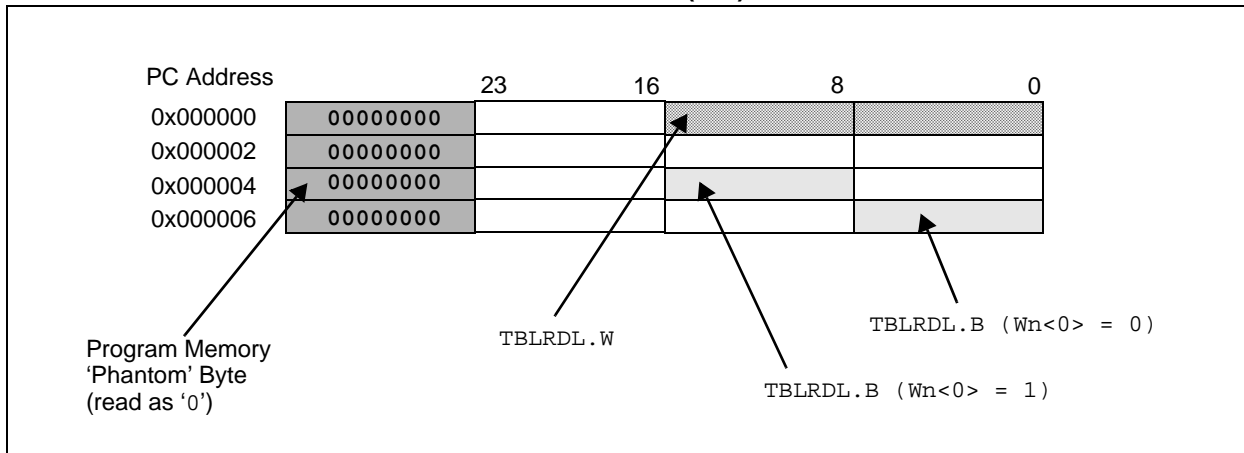
The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to data space addresses. Program memory can thus be regarded as two 16-bit word wide address spaces, residing side by side, each with the same address range. **TBLRD** and **TBLWT** access the space which contains the lsw, and **TBLRDH** and **TBLWTH** access the space which contains the MSB.

Figure 3-2 shows how the EA is created for table operations and data space accesses (PSV = 1). Here, **P<23:0>** refers to a program space word, whereas **D<15:0>** refers to a data space word.

A set of table instructions are provided to move byte or word-sized data to and from program space. See Figure 3-4 and Figure 3-5.

1. **TBLRD**: Table Read Low
Word: Read the LS Word of the program address; **P<15:0>** maps to **D<15:0>**.
Byte: Read one of the LSB of the program address;
P<7:0> maps to the destination byte when byte select = 0;
P<15:8> maps to the destination byte when byte select = 1.
2. **TBLWTL**: Table Write Low (refer to **Section 5.0 “Flash Program Memory”** for details on Flash Programming)
3. **TBLRDH**: Table Read High
Word: Read the MS Word of the program address; **P<23:16>** maps to **D<7:0>**; **D<15:8>** will always be = 0.
Byte: Read one of the MSB of the program address;
P<23:16> maps to the destination byte when byte select = 0;
 The destination byte will always be = 0 when byte select = 1.
4. **TBLWTH**: Table Write High (refer to **Section 5.0 “Flash Program Memory”** for details on Flash Programming)

FIGURE 3-3: PROGRAM DATA TABLE ACCESS (lsw)



3.2 Data Address Space

The core has two data spaces. The data spaces can be considered either separate (for some DSP instructions), or as one unified linear address range (for MCU instructions). The data spaces are accessed using two Address Generation Units (AGUs) and separate data paths.

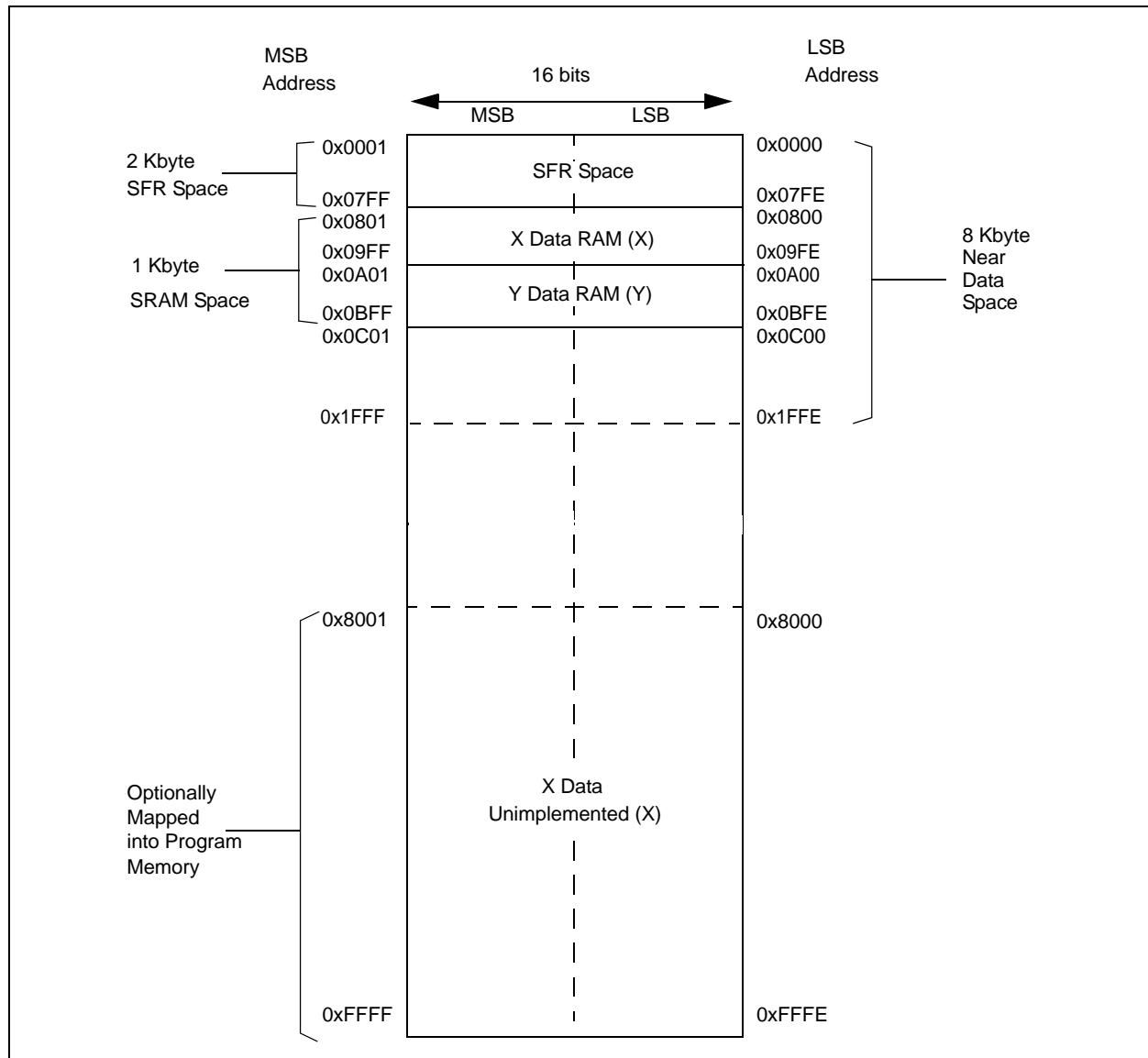
3.2.1 DATA SPACE MEMORY MAP

The data space memory is split into two blocks, X and Y data space. A key element of this architecture is that Y space is a subset of X space, and is fully contained within X space. In order to provide an apparent Linear Addressing space, X and Y spaces have contiguous addresses.

When executing any instruction other than one of the MAC class of instructions, the X block consists of the 64 Kbyte data address space (including all Y addresses). When executing one of the MAC class of instructions, the X block consists of the 64 Kbyte data address space, excluding the Y address block (for data reads only). In other words, all other instructions regard the entire data memory as one composite address space. The MAC class instructions extract the Y address space from data space and address it using EAs sourced from W10 and W11. The remaining X data space is addressed using W8 and W9. Both address spaces are concurrently accessed only with the MAC class instructions.

The data space memory map for the dsPIC30F2011 and dsPIC30F2012 is shown in Figure 3-6. The data space memory map for the dsPIC30F3012 and dsPIC30F3013 is shown in Figure 3-7.

FIGURE 3-6: dsPIC30F2011/2012 DATA SPACE MEMORY MAP



6.0 DATA EEPROM MEMORY

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the “dsPIC30F Family Reference Manual” (DS70046). For more information on the device instruction set and programming, refer to the “16-bit MCU and DSC Programmer’s Reference Manual” (DS70157).

The data EEPROM memory is readable and writable during normal operation over the entire VDD range. The data EEPROM memory is directly mapped in the program memory address space.

The four SFRs used to read and write the program Flash memory are used to access data EEPROM memory, as well. As described in **Section 5.5 “Control Registers”**, these registers are:

- NVMCON
- NVMADR
- NVMADRU
- NVMKEY

The EEPROM data memory allows read and write of single words and 16-word blocks. When interfacing to data memory, NVMADR, in conjunction with the NVMADRU register, are used to address the EEPROM location being accessed. TBLRD and TBLWTL instructions are used to read and write data EEPROM. The dsPIC30F devices have up to 8 Kbytes (4K words) of data EEPROM with an address range from 0x7FF000 to 0x7FFFFE.

A word write operation should be preceded by an erase of the corresponding memory location(s). The write typically requires 2 ms to complete, but the write time varies with voltage and temperature.

A program or erase operation on the data EEPROM does not stop the instruction flow. The user is responsible for waiting for the appropriate duration of time before initiating another data EEPROM write/erase operation. Attempting to read the data EEPROM while a programming or erase operation is in progress results in unspecified data.

Control bit WR initiates write operations similar to program Flash writes. This bit cannot be cleared, only set, in software. They are cleared in hardware at the completion of the write operation. The inability to clear the WR bit in software prevents the accidental or premature termination of a write operation.

The WREN bit, when set, allows a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location. The address register NVMADR remains unchanged.

Note: Interrupt flag bit NVMIF in the IFS0 register is set when write is complete. It must be cleared in software.

6.1 Reading the Data EEPROM

A TBLRD instruction reads a word at the current program word address. This example uses W0 as a pointer to data EEPROM. The result is placed in register W4 as shown in Example 6-1.

EXAMPLE 6-1: DATA EEPROM READ

```
MOV    #LOW_ADDR_WORD,W0 ; Init Pointer
MOV    #HIGH_ADDR_WORD,W1
MOV    W1,TBLPAG
TBLRD  [ W0 ], W4          ; read data EEPROM
```

TABLE 7-5: PORTD REGISTER MAP FOR dsPIC30F2012/3013

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISD	02D2	—	—	—	—	—	—	TRISD9	TRISD8	—	—	—	—	—	—	—	—	0000 0011 0000 0000
PORTD	02D4	—	—	—	—	—	—	RD9	RD8	—	—	—	—	—	—	—	—	0000 0000 0000 0000
LATD	02D6	—	—	—	—	—	—	LATD9	LATD8	—	—	—	—	—	—	—	—	0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

TABLE 7-6: PORTF REGISTER MAP FOR dsPIC30F2012/3013

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TRISF	02DE	—	—	—	—	—	—	—	—	—	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	—	—	0000 0000 0111 1100
PORTF	02E0	—	—	—	—	—	—	—	—	—	RF6	RF5	RF4	RF3	RF2	—	—	0000 0000 0000 0000
LATF	02E2	—	—	—	—	—	—	—	—	—	LATF6	LATF5	LATF4	LATF3	LATF2	—	—	0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

Note: The dsPIC30F2011/3012 devices do not have TRISF, PORTF, or LATF.

Address Error Trap:

This trap is initiated when any of the following circumstances occurs:

1. A misaligned data word access is attempted.
2. A data fetch from our unimplemented data memory location is attempted.
3. A data access of an unimplemented program memory location is attempted.
4. An instruction fetch from vector space is attempted.

<p>Note: In the MAC class of instructions, wherein the data space is split into X and Y data space, unimplemented X space includes all of Y space, and unimplemented Y space includes all of X space.</p>
--

5. Execution of a “BRA #literal” instruction or a “GOTO #literal” instruction, where *literal* is an unimplemented program memory address.
6. Executing instructions after modifying the PC to point the unimplemented program memory addresses. The PC may be modified by loading a value into the stack and executing a RETURN instruction.

Stack Error Trap:

This trap is initiated under the following conditions:

- The Stack Pointer is loaded with a value which is greater than the (user programmable) limit value written into the SPLIM register (stack overflow).
- The Stack Pointer is loaded with a value which is less than 0x0800 (simple stack underflow).

Oscillator Fail Trap:

This trap is initiated if the external oscillator fails and operation becomes reliant on an internal RC backup.

8.3.2 HARD AND SOFT TRAPS

It is possible that multiple traps can become active within the same cycle (e.g., a misaligned word stack write to an overflowed address). In such a case, the fixed priority shown in Figure 8-2 is implemented, which may require the user to check if other traps are pending, in order to completely correct the Fault.

Soft traps include exceptions of priority level 8 through level 11, inclusive. The arithmetic error trap (level 11) falls into this category of traps.

Hard traps include exceptions of priority level 12 through level 15, inclusive. The address error (level 12), stack error (level 13) and oscillator error (level 14) traps fall into this category.

Each hard trap that occurs must be acknowledged before code execution of any type can continue. If a lower priority hard trap occurs while a higher priority trap is pending, acknowledged, or is being processed, a hard trap conflict occurs.

The device is automatically Reset in a hard trap conflict condition. The TRAPR Status bit (RCON<15>) is set when the Reset occurs, so that the condition may be detected in software.

dsPIC30F2011/2012/3012/3013

FIGURE 10-1: 32-BIT TIMER2/3 BLOCK DIAGRAM

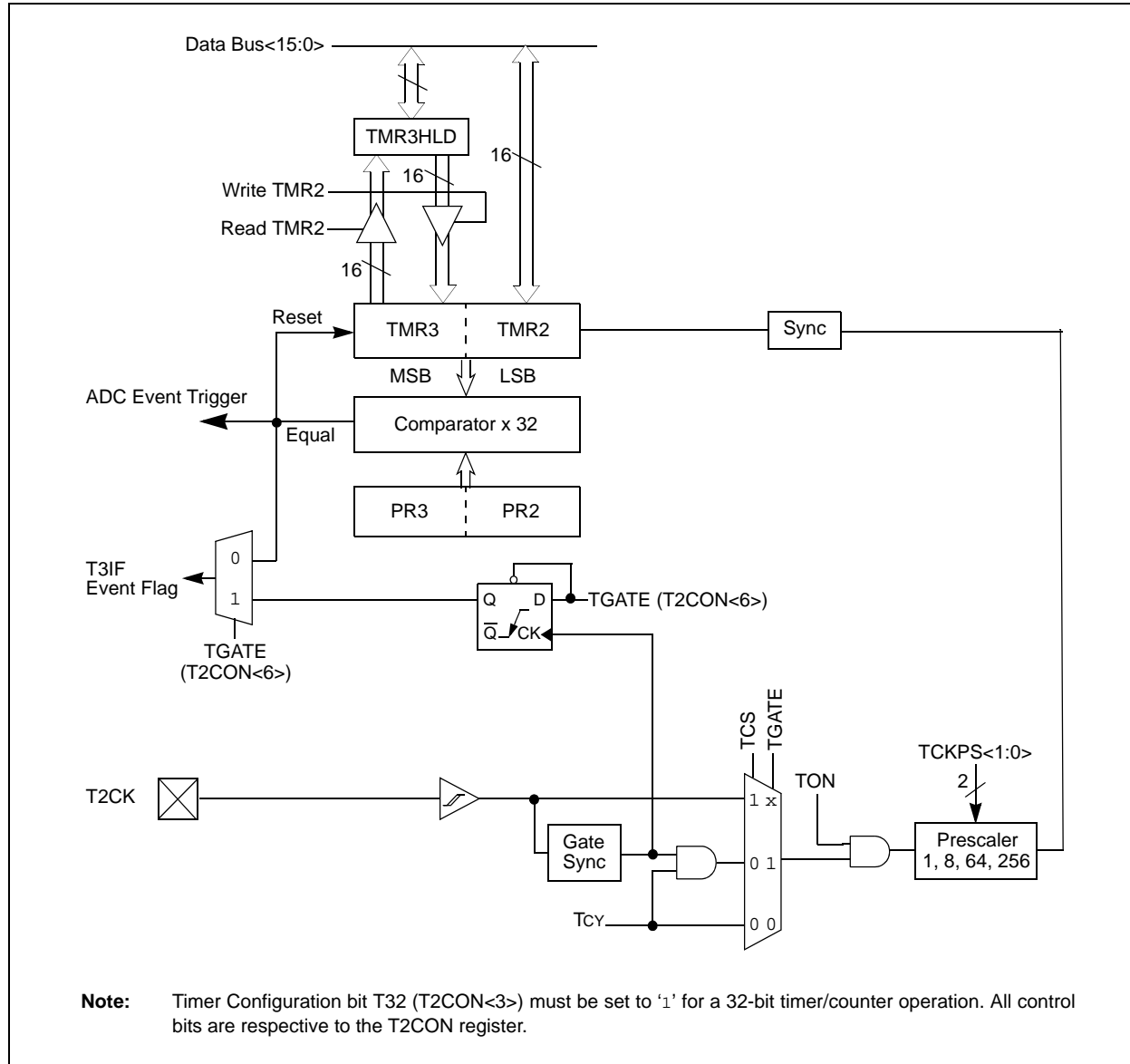


TABLE 11-1: INPUT CAPTURE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
IC1BUF	0140	Input 1 Capture Register																uuuu uuuu uuuu uuuu
IC1CON	0142	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000	
IC2BUF	0144	Input 2 Capture Register																uuuu uuuu uuuu uuuu
IC2CON	0146	—	—	ICSIDL	—	—	—	—	—	ICTMR	ICI<1:0>	ICOV	ICBNE	ICM<2:0>			0000 0000 0000 0000	

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'
Note: Refer to the “dsPIC30F Family Reference Manual” (DS70046) for descriptions of register bit fields.

14.2 I²C Module Addresses

The I2CADD register contains the Slave mode addresses. The register is a 10-bit register.

If the A10M bit (I2CCON<10>) is '0', the address is interpreted by the module as a 7-bit address. When an address is received, it is compared to the 7 LSb of the I2CADD register.

If the A10M bit is '1', the address is assumed to be a 10-bit address. When an address is received, it will be compared with the binary value '11110 A9 A8' (where A9 and A8 are two Most Significant bits of I2CADD). If that value matches, the next address will be compared with the Least Significant 8 bits of I2CADD, as specified in the 10-bit addressing protocol.

The 7-bit I²C Slave Addresses supported by the dsPIC30F are shown in Table 14-1.

TABLE 14-1: 7-BIT I²C™ SLAVE ADDRESSES

0x00	General call address or start byte
0x01-0x03	Reserved
0x04-0x07	Hs-mode Master codes
0x04-0x77	Valid 7-bit addresses
0x78-0x7b	Valid 10-bit addresses (lower 7 bits)
0x7c-0x7f	Reserved

14.3 I²C 7-bit Slave Mode Operation

Once enabled (I2CEN = 1), the slave module will wait for a Start bit to occur (i.e., the I²C module is 'Idle'). Following the detection of a Start bit, 8 bits are shifted into I2CRSR and the address is compared against I2CADD. In 7-bit mode (A10M = 0), bits I2CADD<6:0> are compared against I2CRSR<7:1> and I2CRSR<0> is the R_W bit. All incoming bits are sampled on the rising edge of SCL.

If an address match occurs, an acknowledgement will be sent, and the slave event interrupt flag (SI2CIF) is set on the falling edge of the ninth (ACK) bit. The address match does not affect the contents of the I2CRCV buffer or the RBF bit.

14.3.1 SLAVE TRANSMISSION

If the R_W bit received is a '1', then the serial port will go into Transmit mode. It will send ACK on the ninth bit and then hold SCL to '0' until the CPU responds by writing to I2CTRNL. SCL is released by setting the SCLREL bit, and 8 bits of data are shifted out. Data bits are shifted out on the falling edge of SCL, such that SDA is valid during SCL high. The interrupt pulse is sent on the falling edge of the ninth clock pulse, regardless of the status of the ACK received from the master.

14.3.2 SLAVE RECEPTION

If the R_W bit received is a '0' during an address match, then Receive mode is initiated. Incoming bits are sampled on the rising edge of SCL. After 8 bits are received, if I2CRCV is not full or I2COV is not set, I2CRSR is transferred to I2CRCV. ACK is sent on the ninth clock.

If the RBF flag is set, indicating that I2CRCV is still holding data from a previous operation (RBF = 1), then ACK is not sent; however, the interrupt pulse is generated. In the case of an overflow, the contents of the I2CRSR are not loaded into the I2CRCV.

Note: The I2CRCV will be loaded if the I2COV bit = 1 and the RBF flag = 0. In this case, a read of the I2CRCV was performed but the user did not clear the state of the I2COV bit before the next receive occurred. The acknowledgement is not sent (ACK = 1) and the I2CRCV is updated.

14.4 I²C 10-bit Slave Mode Operation

In 10-bit mode, the basic receive and transmit operations are the same as in the 7-bit mode. However, the criteria for address match is more complex.

The I²C specification dictates that a slave must be addressed for a write operation with two address bytes following a Start bit.

The A10M bit is a control bit that signifies that the address in I2CADD is a 10-bit address rather than a 7-bit address. The address detection protocol for the first byte of a message address is identical for 7-bit and 10-bit messages, but the bits being compared are different.

I2CADD holds the entire 10-bit address. Upon receiving an address following a Start bit, I2CRSR <7:3> is compared against a literal '11110' (the default 10-bit address) and I2CRSR<2:1> are compared against I2CADD<9:8>. If a match occurs and if R_W = 0, the interrupt pulse is sent. The ADD10 bit will be cleared to indicate a partial address match. If a match fails or R_W = 1, the ADD10 bit is cleared and the module returns to the Idle state.

The low byte of the address is then received and compared with I2CADD<7:0>. If an address match occurs, the interrupt pulse is generated and the ADD10 bit is set, indicating a complete 10-bit address match. If an address match did not occur, the ADD10 bit is cleared and the module returns to the Idle state.

15.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF or U2TXIF) is located in the corresponding interrupt flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on the UTXISEL control bit:

- a) If UTXISEL = 0, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR). This means that the transmit buffer has at least one empty word.
- b) If UTXISEL = 1, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR) and the transmit buffer is empty.

Switching between the two Interrupt modes during operation is possible and sometimes offers more flexibility.

15.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) will cause the UxTX line to be driven to logic '0'. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a Break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB, or starting other transmitter activity. Transmission of a Break character does not generate a transmit interrupt.

15.4 Receiving Data

15.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

1. Set up the UART (see **Section 15.3.1 "Transmitting in 8-bit data mode"**).
2. Enable the UART (see **Section 15.3.1 "Transmitting in 8-bit data mode"**).
3. A receive interrupt will be generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read the received data from UxRXREG. The act of reading UxRXREG will move the next word to the top of the receive FIFO, and the PERR and FERR values will be updated.

15.4.2 RECEIVE BUFFER (UxRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = 1 indicates that the receive buffer has data available. URXDA = 0 implies that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer will be read and no data shift will occur within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a Power Saving mode.

15.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding interrupt flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

- a) If URXISEL<1:0> = 00 or 01, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the receive buffer. There may be one or more characters in the receive buffer.
- b) If URXISEL<1:0> = 10, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 3 characters.
- c) If URXISEL<1:0> = 11, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

15.5 Reception Error Handling

15.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

- a) The receive buffer is full.
- b) The Receive Shift register is full, but unable to transfer the character to the receive buffer.
- c) The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

Once OERR is set, no further data is shifted in UxRSR (until the OERR bit is cleared in software or a Reset occurs). The data held in UxRSR and UxRXREG remains valid.

16.4 Programming the Start of Conversion Trigger

The conversion trigger will terminate acquisition and start the requested conversions.

The SSRC<2:0> bits select the source of the conversion trigger. The SSRC bits provide for up to four alternate sources of conversion trigger.

When SSRC<2:0> = 000, the conversion trigger is under software control. Clearing the SAMP bit will cause the conversion trigger.

When SSRC<2:0> = 111 (Auto-Start mode), the conversion trigger is under A/D clock control. The SAMC bits select the number of A/D clocks between the start of acquisition and the start of conversion. This provides the fastest conversion rates on multiple channels. SAMC must always be at least one clock cycle.

Other trigger sources can come from timer modules or external interrupts.

16.5 Aborting a Conversion

Clearing the ADON bit during a conversion will abort the current conversion and stop the sampling sequencing until the next sampling trigger. The ADCBUF will not be updated with the partially completed A/D conversion sample. That is, the ADCBUF will continue to contain the value of the last completed conversion (or the last value written to the ADCBUF register).

If the clearing of the ADON bit coincides with an auto-start, the clearing has a higher priority and a new conversion will not start.

After the A/D conversion is aborted, a 2 TAD wait is required before the next sampling may be started by setting the SAMP bit.

16.6 Selecting the ADC Conversion Clock

The ADC conversion requires 14 TAD. The source of the ADC conversion clock is software selected, using a 6-bit counter. There are 64 possible options for TAD.

The internal RC oscillator is selected by setting the ADRC bit.

For correct ADC conversions, the ADC conversion clock (TAD) must be selected to ensure a minimum TAD time of 334 nsec (for VDD = 5V). Refer to **Section 20.0 “Electrical Characteristics”** for minimum TAD under other operating conditions.

Example 16-1 shows a sample calculation for the ADCS<5:0> bits, assuming a device operating speed of 30 MIPS.

EXAMPLE 16-1: ADC CONVERSION CLOCK AND SAMPLING RATE CALCULATION

Minimum TAD = 334 nsec
TCY = 33.33 nsec (30 MIPS)

$$\begin{aligned} \text{ADCS}<5:0> &= 2 \frac{\text{TAD}}{\text{TCY}} - 1 \\ &= 2 \cdot \frac{334 \text{ nsec}}{33.33 \text{ nsec}} - 1 \\ &= 19.04 \end{aligned}$$

Therefore,
Set ADCS<5:0> = 19

$$\begin{aligned} \text{Actual TAD} &= \frac{\text{TCY}}{2} (\text{ADCS}<5:0> + 1) \\ &= \frac{33.33 \text{ nsec}}{2} (19 + 1) \\ &= 334 \text{ nsec} \end{aligned}$$

If SSRC<2:0> = ‘111’ and SAMC<4:0> = ‘00001’

Since,

$$\begin{aligned} \text{Sampling Time} &= \text{Acquisition Time} + \text{Conversion Time} \\ &= 1 \text{ TAD} + 14 \text{ TAD} \\ &= 15 \times 334 \text{ nsec} \end{aligned}$$

Therefore,

$$\begin{aligned} \text{Sampling Rate} &= \frac{1}{(15 \times 334 \text{ nsec})} \\ &= \sim 200 \text{ kHz} \end{aligned}$$

EQUATION 16-1: ADC CONVERSION CLOCK

$$\text{TAD} = \text{TCY} * (0.5 * (\text{ADCS}<5:0> + 1))$$

17.4 Watchdog Timer (WDT)

17.4.1 WATCHDOG TIMER OPERATION

The primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction. The WDT is a free-running timer which runs off an on-chip RC oscillator, requiring no external component. Therefore, the WDT timer will continue to operate even if the main processor clock (e.g., the crystal oscillator) fails.

17.4.2 ENABLING AND DISABLING THE WDT

The Watchdog Timer can be “Enabled” or “Disabled” only through a Configuration bit (FWDTEN) in the Configuration register, FWDTE.

Setting FWDTEN = 1 enables the Watchdog Timer. The enabling is done when programming the device. By default, after chip erase, FWDTEN bit = 1. Any device programmer capable of programming dsPIC30F devices allows programming of this and other Configuration bits.

If enabled, the WDT will increment until it overflows or “times out”. A WDT time-out will force a device Reset (except during Sleep). To prevent a WDT time-out, the user must clear the Watchdog Timer using a CLRWDTE instruction.

If a WDT times out during Sleep, the device will wake-up. The WDTO bit in the RCON register will be cleared to indicate a wake-up resulting from a WDT time-out.

Setting FWDTEN = 0 allows user software to enable/disable the Watchdog Timer via the SWDTEN (RCON<5>) control bit.

17.5 Low-Voltage Detect

The Low-Voltage Detect (LVD) module is used to detect when the VDD of the device drops below a threshold value, VLVD, which is determined by the LVDL<3:0> bits (RCON<11:8>) and is thus user programmable. The internal voltage reference circuitry requires a nominal amount of time to stabilize, and the BGST bit (RCON<13>) indicates when the voltage reference has stabilized.

In some devices, the LVD threshold voltage may be applied externally on the LVDIN pin.

The LVD module is enabled by setting the LVDEN bit (RCON<12>).

17.6 Power-Saving Modes

There are two power-saving states that can be entered through the execution of a special instruction, PWRSAV; these are Sleep and Idle.

The format of the PWRSAV instruction is as follows:

PWRSAV <parameter>, where ‘parameter’ defines Idle or Sleep mode.

17.6.1 SLEEP MODE

In Sleep mode, the clock to the CPU and peripherals is shut down. If an on-chip oscillator is being used, it is shut down.

The Fail-Safe Clock Monitor is not functional during Sleep since there is no clock to monitor. However, LPRC clock remains active if WDT is operational during Sleep.

The brown-out protection circuit and the Low-Voltage Detect circuit, if enabled, will remain functional during Sleep.

The processor wakes up from Sleep if at least one of the following conditions has occurred:

- any interrupt that is individually enabled and meets the required priority level
- any Reset (POR, BOR and MCLR)
- WDT time-out

On waking up from Sleep mode, the processor will restart the same clock that was active prior to entry into Sleep mode. When clock switching is enabled, bits COSC<2:0> will determine the oscillator source that will be used on wake-up. If clock switch is disabled, then there is only one system clock.

Note: If a POR or BOR occurred, the selection of the oscillator is based on the FOS<2:0> and FPR<4:0> Configuration bits.

If the clock source is an oscillator, the clock to the device will be held off until OST times out (indicating a stable oscillator). If PLL is used, the system clock is held off until LOCK = 1 (indicating that the PLL is stable). In either case, TPOR, TLOCK and TPWRT delays are applied.

If EC, FRC, LPRC or ERC oscillators are used, then a delay of TPOR (~ 10 μs) is applied. This is the smallest delay possible on wake-up from Sleep.

Moreover, if LP oscillator was active during Sleep and LP is the oscillator used on wake-up, then the start-up delay will be equal to TPOR. PWRT delay and OST timer delay are not applied. In order to have the smallest possible start-up delay when waking up from Sleep, one of these faster wake-up options should be selected before entering Sleep.

dsPIC30F2011/2012/3012/3013

TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
66	RRNC	RRNC <i>f</i>	<i>f</i> = Rotate Right (No Carry) <i>f</i>	1	1	N,Z
		RRNC <i>f</i> , WREG	WREG = Rotate Right (No Carry) <i>f</i>	1	1	N,Z
		RRNC <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = Rotate Right (No Carry) <i>Ws</i>	1	1	N,Z
67	SAC	SAC <i>Acc</i> , #Slit4, <i>Wdo</i>	Store Accumulator	1	1	None
		SAC.R <i>Acc</i> , #Slit4, <i>Wdo</i>	Store Rounded Accumulator	1	1	None
68	SE	SE <i>Ws</i> , <i>Wnd</i>	<i>Wnd</i> = sign-extended <i>Ws</i>	1	1	C,N,Z
69	SETM	SETM <i>f</i>	<i>f</i> = 0xFFFF	1	1	None
		SETM WREG	WREG = 0xFFFF	1	1	None
		SETM <i>Ws</i>	<i>Ws</i> = 0xFFFF	1	1	None
70	SFTAC	SFTAC <i>Acc</i> , <i>Wn</i>	Arithmetic Shift Accumulator by (<i>Wn</i>)	1	1	OA,OB,OAB,SA,SB,SAB
		SFTAC <i>Acc</i> , #Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB,SA,SB,SAB
71	SL	SL <i>f</i>	<i>f</i> = Left Shift <i>f</i>	1	1	C,N,OV,Z
		SL <i>f</i> , WREG	WREG = Left Shift <i>f</i>	1	1	C,N,OV,Z
		SL <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = Left Shift <i>Ws</i>	1	1	C,N,OV,Z
		SL <i>Wb</i> , <i>Wns</i> , <i>Wnd</i>	<i>Wnd</i> = Left Shift <i>Wb</i> by <i>Wns</i>	1	1	N,Z
		SL <i>Wb</i> , #lit5, <i>Wnd</i>	<i>Wnd</i> = Left Shift <i>Wb</i> by lit5	1	1	N,Z
72	SUB	SUB <i>Acc</i>	Subtract Accumulators	1	1	OA,OB,OAB,SA,SB,SAB
		SUB <i>f</i>	<i>f</i> = <i>f</i> - WREG	1	1	C,DC,N,OV,Z
		SUB <i>f</i> , WREG	WREG = <i>f</i> - WREG	1	1	C,DC,N,OV,Z
		SUB #lit10, <i>Wn</i>	<i>Wn</i> = <i>Wn</i> - lit10	1	1	C,DC,N,OV,Z
		SUB <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Wb</i> - <i>Ws</i>	1	1	C,DC,N,OV,Z
		SUB <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = <i>Wb</i> - lit5	1	1	C,DC,N,OV,Z
73	SUBB	SUBB <i>f</i>	<i>f</i> = <i>f</i> - WREG - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB <i>f</i> , WREG	WREG = <i>f</i> - WREG - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB #lit10, <i>Wn</i>	<i>Wn</i> = <i>Wn</i> - lit10 - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Wb</i> - <i>Ws</i> - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = <i>Wb</i> - lit5 - (\overline{C})	1	1	C,DC,N,OV,Z
74	SUBR	SUBR <i>f</i>	<i>f</i> = WREG - <i>f</i>	1	1	C,DC,N,OV,Z
		SUBR <i>f</i> , WREG	WREG = WREG - <i>f</i>	1	1	C,DC,N,OV,Z
		SUBR <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Ws</i> - <i>Wb</i>	1	1	C,DC,N,OV,Z
		SUBR <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = lit5 - <i>Wb</i>	1	1	C,DC,N,OV,Z
75	SUBBR	SUBBR <i>f</i>	<i>f</i> = WREG - <i>f</i> - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR <i>f</i> , WREG	WREG = WREG - <i>f</i> - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Ws</i> - <i>Wb</i> - (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = lit5 - <i>Wb</i> - (\overline{C})	1	1	C,DC,N,OV,Z
76	SWAP	SWAP.b <i>Wn</i>	<i>Wn</i> = nibble swap <i>Wn</i>	1	1	None
		SWAP <i>Wn</i>	<i>Wn</i> = byte swap <i>Wn</i>	1	1	None
77	TBLRDH	TBLRDH <i>Ws</i> , <i>Wd</i>	Read Prog<23:16> to <i>Wd</i> <7:0>	1	2	None
78	TBLRDL	TBLRDL <i>Ws</i> , <i>Wd</i>	Read Prog<15:0> to <i>Wd</i>	1	2	None
79	TBLWTH	TBLWTH <i>Ws</i> , <i>Wd</i>	Write <i>Ws</i> <7:0> to Prog<23:16>	1	2	None
80	TBLWTL	TBLWTL <i>Ws</i> , <i>Wd</i>	Write <i>Ws</i> to Prog<15:0>	1	2	None
81	ULNK	ULNK	Unlink frame pointer	1	1	None
82	XOR	XOR <i>f</i>	<i>f</i> = <i>f</i> .XOR. WREG	1	1	N,Z
		XOR <i>f</i> , WREG	WREG = <i>f</i> .XOR. WREG	1	1	N,Z
		XOR #lit10, <i>Wn</i>	<i>Wd</i> = lit10 .XOR. <i>Wd</i>	1	1	N,Z
		XOR <i>Wb</i> , <i>Ws</i> , <i>Wd</i>	<i>Wd</i> = <i>Wb</i> .XOR. <i>Ws</i>	1	1	N,Z
		XOR <i>Wb</i> , #lit5, <i>Wd</i>	<i>Wd</i> = <i>Wb</i> .XOR. lit5	1	1	N,Z
83	ZE	ZE <i>Ws</i> , <i>Wnd</i>	<i>Wnd</i> = Zero-extend <i>Ws</i>	1	1	C,Z,N

19.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

19.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

19.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

19.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/librarian features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

19.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

19.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

19.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

19.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

dsPIC30F2011/2012/3012/3013

TABLE 20-15: PLL CLOCK TIMING SPECIFICATIONS (VDD = 2.5 TO 5.5 V)

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
OS50	FPLLI	PLL Input Frequency Range ⁽²⁾	4	—	10	MHz	EC with 4x PLL
			4	—	10	MHz	EC with 8x PLL
			4	—	7.5 ⁽⁴⁾	MHz	EC with 16x PLL
			4	—	10	MHz	XT with 4x PLL
			4	—	10	MHz	XT with 8x PLL
			4	—	7.5 ⁽⁴⁾	MHz	XT with 16x PLL
			5 ⁽³⁾	—	10	MHz	HS/2 with 4x PLL
			5 ⁽³⁾	—	10	MHz	HS/2 with 8x PLL
			5 ⁽³⁾	—	7.5 ⁽⁴⁾	MHz	HS/2 with 16x PLL
			4	—	8.33 ⁽³⁾	MHz	HS/3 with 4x PLL
			4	—	8.33 ⁽³⁾	MHz	HS/3 with 8x PLL
			4	—	7.5 ⁽⁴⁾	MHz	HS/3 with 16x PLL
OS51	FSYS	On-Chip PLL Output ⁽²⁾	16	—	120	MHz	EC, XT, HS/2, HS/3 modes with PLL
OS52	TLOC	PLL Start-up Time (Lock Time)	—	20	50	μs	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: Limited by oscillator frequency range.

4: Limited by device operating frequency range.

TABLE 20-16: PLL JITTER

AC CHARACTERISTICS		Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
OS61	x4 PLL	—	0.251	0.413	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0 to 3.6V
		—	0.251	0.413	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0 to 3.6V
		—	0.256	0.47	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5 to 5.5V
		—	0.256	0.47	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5 to 5.5V
	x8 PLL	—	0.355	0.584	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0 to 3.6V
		—	0.355	0.584	%	-40°C ≤ TA ≤ +125°C	VDD = 3.0 to 3.6V
		—	0.362	0.664	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5 to 5.5V
		—	0.362	0.664	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5 to 5.5V
	x16 PLL	—	0.67	0.92	%	-40°C ≤ TA ≤ +85°C	VDD = 3.0 to 3.6V
		—	0.632	0.956	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5 to 5.5V
		—	0.632	0.956	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5 to 5.5V
		—	0.632	0.956	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5 to 5.5V

Note 1: These parameters are characterized but not tested in manufacturing.

dsPIC30F2011/2012/3012/3013

FIGURE 20-10: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS

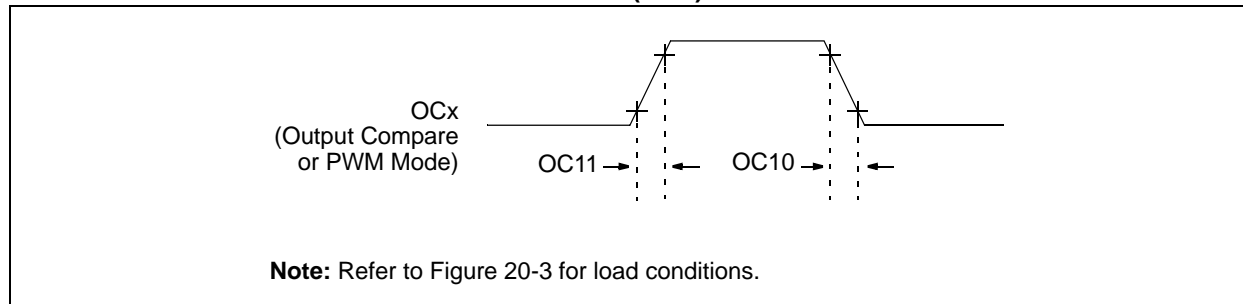


TABLE 20-27: OUTPUT COMPARE MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

- Note 1:** These parameters are characterized but not tested in manufacturing.
- Note 2:** Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

dsPIC30F2011/2012/3012/3013

FIGURE 20-11: OC/PWM MODULE TIMING CHARACTERISTICS

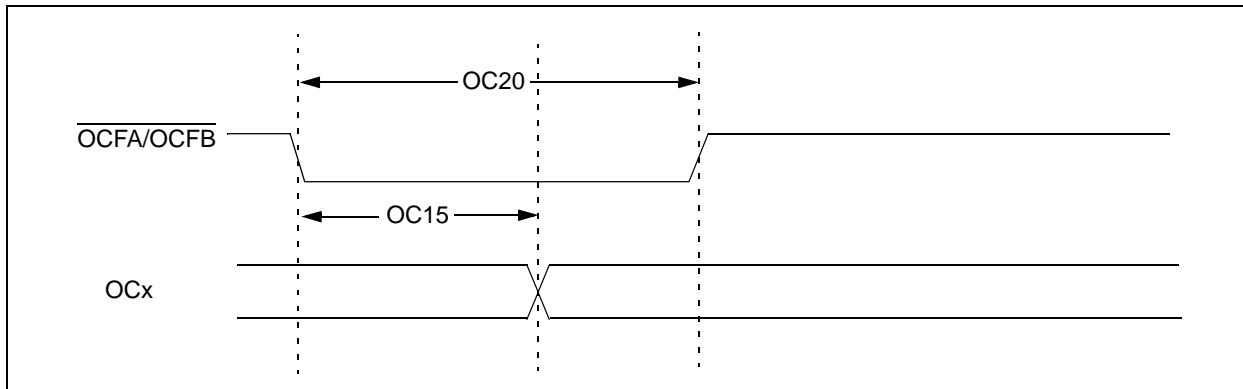


TABLE 20-28: SIMPLE OC/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions
OC15	TFD	Fault Input to PWM I/O Change	—	—	50	ns	
OC20	TFLT	Fault Input Pulse Width	50	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

Note 2: Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

dsPIC30F2011/2012/3012/3013

TABLE 20-33: I²C™ BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic		Min ⁽¹⁾	Max	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM20	TF:SCL	SDA and SCL Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	—	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	—	—	ns	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	After this period the first clock pulse is generated
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 1)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	Tcy/2 (BRG + 1)	—	ns	
			400 kHz mode	Tcy/2 (BRG + 1)	—	ns	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 1)	—	ns	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	—	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	—	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	

Note 1: BRG is the value of the I²C Baud Rate Generator. Refer to **Section 21. “Inter-Integrated Circuit™ (I²C)”** (DS70068) in the *dsPIC30F Family Reference Manual* (DS70046).

2: Maximum pin capacitance = 10 pF for all I²C™ pins (for 1 MHz mode only).