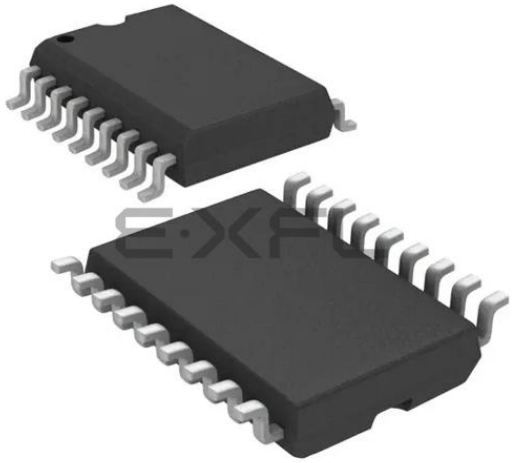

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 30 MIPs |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 24KB (8K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 18-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 18-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3012-30i-so |

**NOTES:**

**FIGURE 1-4: dsPIC30F3013 BLOCK DIAGRAM**

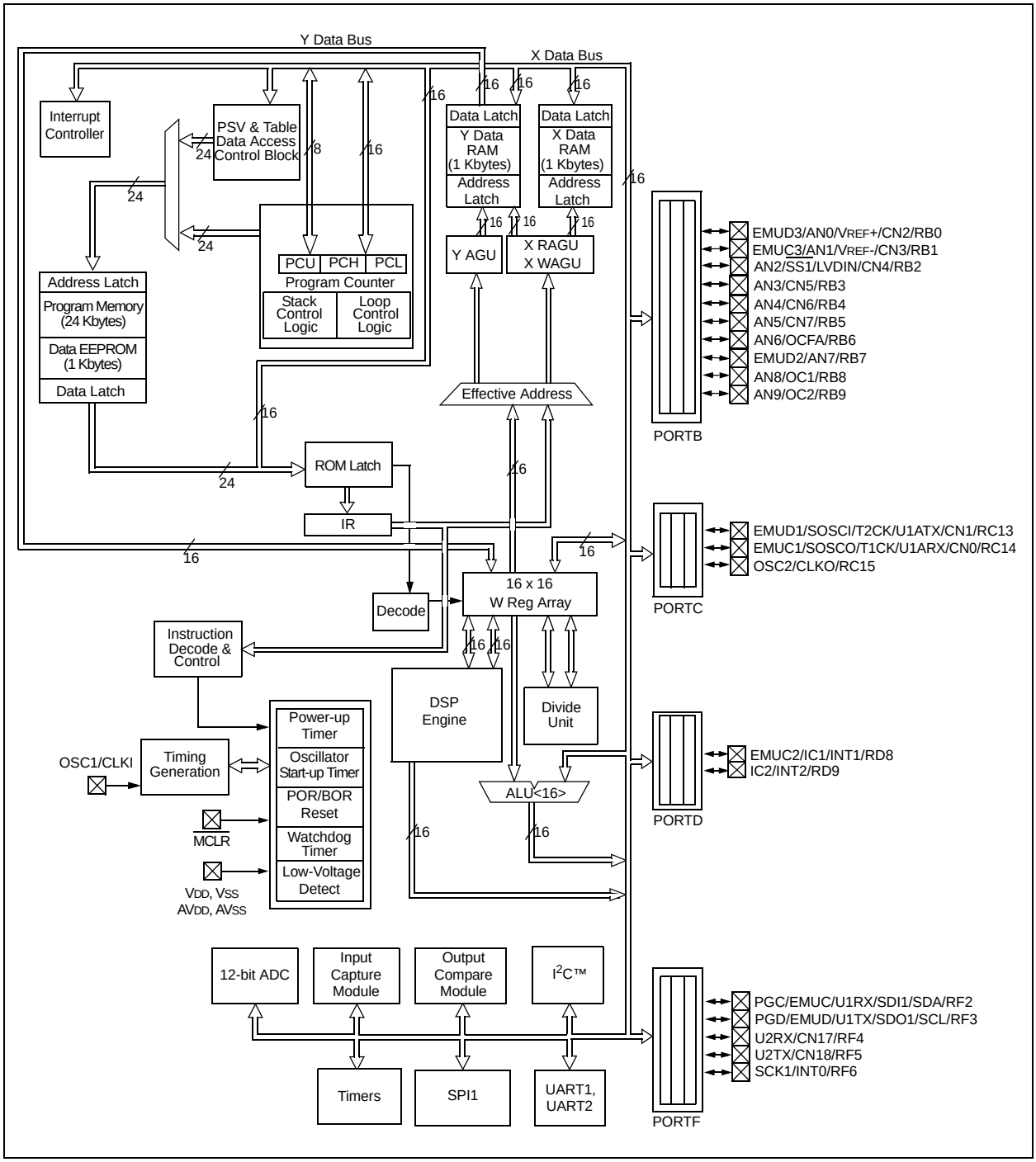
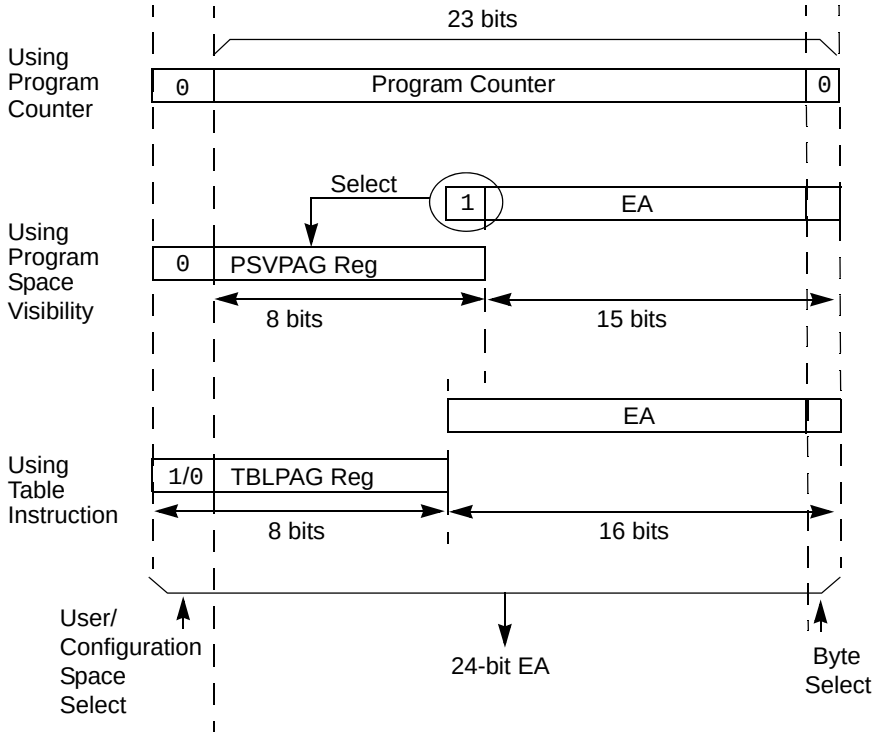


**TABLE 3-1: PROGRAM SPACE ADDRESS CONSTRUCTION**

| Access Type | Access Space | Program Space Address | | | | |
|---|---|---|---|---|---|---|
| | | <23> | <22:16> | <15> | <14:1> | <0> |
| Instruction Access | User | 0 | PC<22:1> | | | 0 |
| TBLRD/TBLWT | User (TBLPAG<7> = 0) | TBLPAG<7:0> | | Data EA<15:0> | | |
| TBLRD/TBLWT | Configuration (TBLPAG<7> = 1) | TBLPAG<7:0> | | Data EA<15:0> | | |
| Program Space Visibility | User | 0 | PSVPAG<7:0> | | Data EA<14:0> | |

**FIGURE 3-2: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**




**Note:** Program space visibility cannot be used to access bits <23:16> of a word in program memory.

## 5.4 RTSP Operation

The dsPIC30F Flash program memory is organized into rows and panels. Each row consists of 32 instructions or 96 bytes. Each panel consists of 128 rows or 4K x 24 instructions. RTSP allows the user to erase one row (32 instructions) at a time and to program four instructions at one time. RTSP may be used to program multiple program memory panels, but the table pointer must be changed at each panel boundary.

Each panel of program memory contains write latches that hold 32 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the panel write latches. The data to be programmed into the panel is loaded in sequential order into the write latches; instruction 0, instruction 1, etc. The instruction words loaded must always be from a 32 address boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the write latches. Programming is performed by setting the special bits in the NVMCON register. 32 TBLWTL and four TBLWTH instructions are required to load the 32 instructions. If multiple panel programming is required, the Table Pointer needs to be changed and the next set of multiple write latches written.

All of the table write operations are single-word writes (2 instruction cycles), because only the table latches are written. A programming cycle is required for programming each row.

The Flash Program Memory is readable, writable and erasable during normal operation over the entire VDD range.

## 5.5 Control Registers

The four SFRs used to read and write the program Flash memory are:

- NVMCON
- NVMADR
- NVMADRU
- NVMKEY

### 5.5.1 NVMCON REGISTER

The NVMCON register controls which blocks are to be erased, which memory type is to be programmed, and start of the programming cycle.

### 5.5.2 NVMADR REGISTER

The NVMADR register is used to hold the lower two bytes of the Effective Address. The NVMADR register captures the EA<15:0> of the last table instruction that has been executed and selects the row to write.

### 5.5.3 NVMADRU REGISTER

The NVMADRU register is used to hold the upper byte of the Effective Address. The NVMADRU register captures the EA<23:16> of the last table instruction that has been executed.

### 5.5.4 NVMKEY REGISTER

NVMKEY is a write-only register that is used for write protection. To start a programming or an erase sequence, the user must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.6 "Programming Operations"** for further details.

| | |
|---|---|
| **Note:** | The user can also directly write to the NVMADR and NVMADRU registers to specify a program memory address for erasing or programming. |

**TABLE 8-3: dsPIC30F3013 INTERRUPT CONTROLLER REGISTER MAP**

| SFR Name | ADR | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INTCON1 | 0080 | NSTDIS | — | — | — | — | OVATE | OVBTE | COVTE | — | — | — | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 0000 0000 0000 |
| INTCON2 | 0082 | ALTIVT | DISI | — | — | — | — | — | — | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 0000 0000 0000 0000 |
| IFS0 | 0084 | CNIF | MI2CIF | SI2CIF | NVMIF | ADIF | U1TXIF | U1RXIF | SPI1IF | T3IF | T2IF | OC2IF | IC2IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 0000 0000 0000 |
| IFS1 | 0086 | — | — | — | — | — | — | U2TXIF | U2RXIF | INT2IF | — | — | — | — | — | — | INT1IF | 0000 0000 0000 0000 |
| IFS2 | 0088 | — | — | — | — | — | LVDIF | — | — | — | — | — | — | — | — | — | — | 0000 0000 0000 0000 |
| IEC0 | 008C | CNIE | MI2CIE | SI2CIE | NVMIE | ADIE | U1TXIE | U1RXIE | SPI1IE | T3IE | T2IE | OC2IE | IC2IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 0000 0000 0000 |
| IEC1 | 008E | — | — | — | — | — |  | U2TXIE | U2RXIE | INT2IE | — | — | — | — | — | — | INT1IE | 0000 0000 0000 0000 |
| IEC2 | 0090 | — | — | — | — | — | LVDIE | — | — | — | — | — | — | — | — | — | — | 0000 0000 0000 0000 |
| IPC0 | 0094 | — | T1IP<2:0> | | | — | OC1IP<2:0> | | | — | IC1IP<2:0> | | | — | INT0IP<2:0> | | | 0100 0100 0100 0100 |
| IPC1 | 0096 | — | T31P<2:0> | | | — | T2IP<2:0> | | | — | OC2IP<2:0> | | | — | IC2IP<2:0> | | | 0100 0100 0100 0100 |
| IPC2 | 0098 | — | ADIP<2:0> | | | — | U1TXIP<2:0> | | | — | U1RXIP<2:0> | | | — | SPI1IP<2:0> | | | 0100 0100 0100 0100 |
| IPC3 | 009A | — | CNIP<2:0> | | | — | MI2CIP<2:0> | | | — | SI2CIP<2:0> | | | — | NVMIP<2:0> | | | 0100 0100 0100 0100 |
| IPC4 | 009C | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP<2:0> | | | 0000 0000 0000 0100 |
| IPC5 | 009E | — | INT2IP<2:0> | | | — | — | — | — | — | — | — | — | — | | | | 0100 0000 0000 0000 |
| IPC6 | 00A0 | — | — | — | — | — | — | — | — | — | U2TXIP<2:0> | | | — | U2RXIP<2:0> | | | 0000 0000 0100 0100 |
| IPC7 | 00A2 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 0000 0000 0000 |
| IPC8 | 00A4 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 0000 0000 0000 |
| IPC9 | 00A6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 0000 0000 0000 |
| IPC10 | 00A8 | — | — | — | — | — | LVDIP<2:0> | | | — | — | — | — | — | — | — | — | 0000 0100 0000 0000 |

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**Note:** Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

**FIGURE 13-1: SPI BLOCK DIAGRAM**

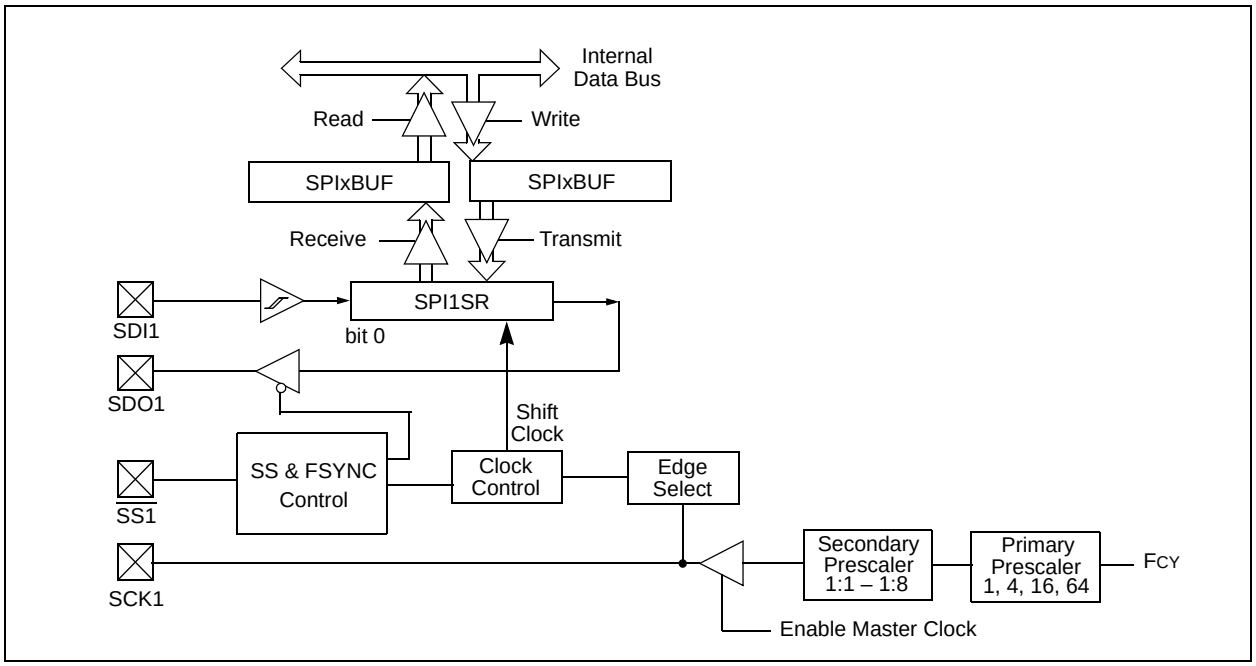



Figure 13-2 depicts the a master/slave connection between two processors. In Master mode, the clock is generated by prescaling the system clock. Data is transmitted as soon as a value is written to SPI1BUF. The interrupt is generated at the middle of the transfer of the last bit.

In Slave mode, data is transmitted and received as external clock pulses appear on SCK. Again, the interrupt is generated when the last bit is latched. If $\overline{SS1}$ control is enabled, then transmission and reception are enabled only when $\overline{SS1}$ = low. The SDO1 output will be disabled in $\overline{SS1}$ mode with $\overline{SS1}$ high.

The clock provided to the module is (FOSC/4). This clock is then prescaled by the primary (PPRE<1:0>) and the secondary (SPRE<2:0>) prescale factors. The CKE bit determines whether transmit occurs on transition from active clock state to Idle clock state, or vice versa. The CKP bit selects the Idle state (high or low) for the clock.

### 13.1.1 WORD AND BYTE COMMUNICATION

A control bit, MODE16 (SPI1CON<10>), allows the module to communicate in either 16-bit or 8-bit mode. 16-bit operation is identical to 8-bit operation except that the number of bits transmitted is 16 instead of 8.

The user software must disable the module prior to changing the MODE16 bit. The SPI module is reset when the MODE16 bit is changed by the user.

A basic difference between 8-bit and 16-bit operation is that the data is transmitted out of bit 7 of the SPI1SR for 8-bit operation, and data is transmitted out of bit 15 of the SPI1SR for 16-bit operation. In both modes, data is shifted into bit 0 of the SPI1SR.

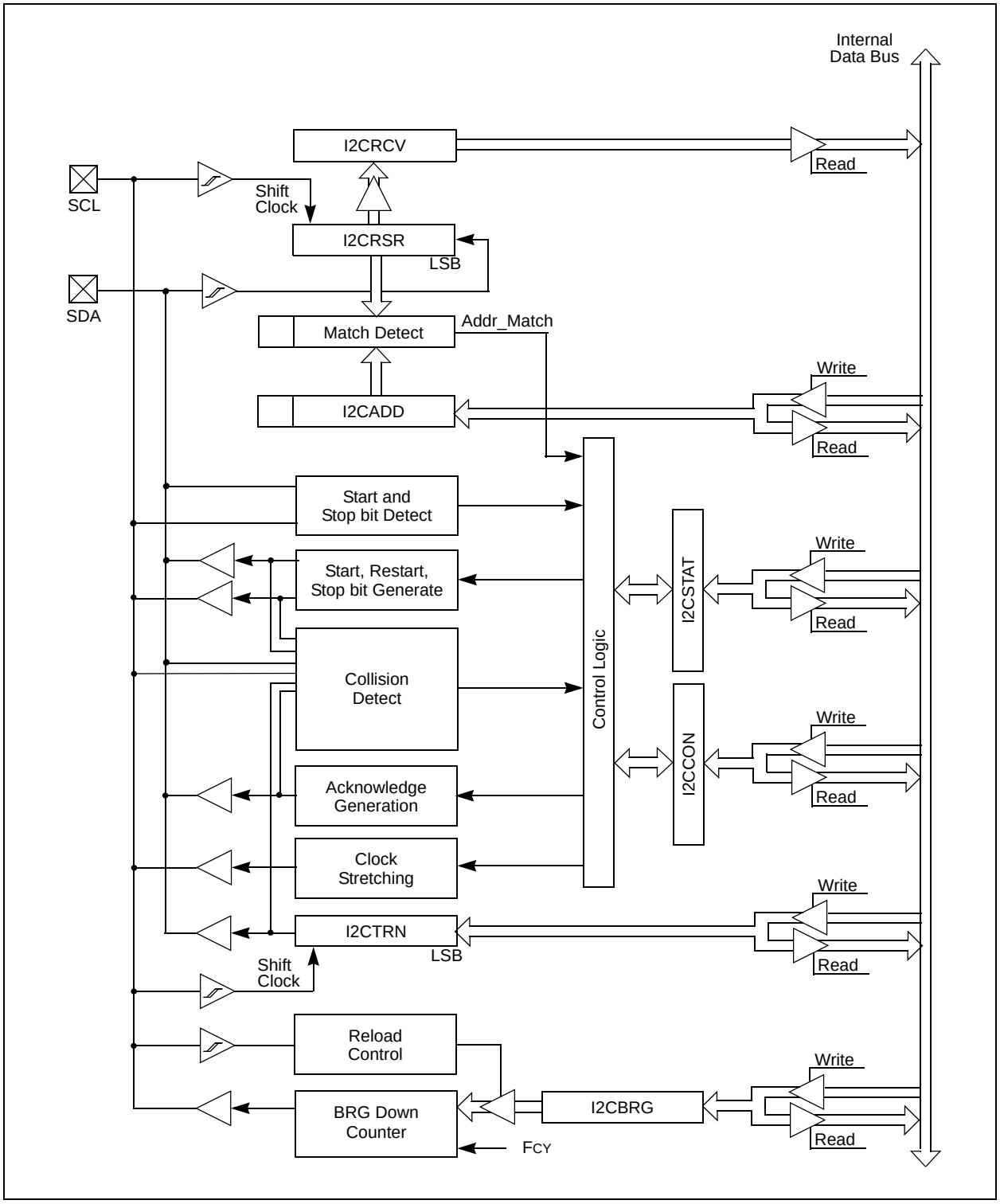
### 13.1.2 SDO1 DISABLE

A control bit, DISSDO, is provided to the SPI1CON register to allow the SDO1 output to be disabled. This will allow the SPI module to be connected in an input only configuration. SDO1 can also be used for general purpose I/O.

## 13.2 Framed SPI Support

The module supports a basic framed SPI protocol in Master or Slave mode. The control bit, FRMEN, enables framed SPI support and causes the $\overline{SS1}$ pin to perform the Frame Synchronization Pulse (FSYNC) function. The control bit, SPIFSD, determines whether the $\overline{SS1}$ pin is an input or an output (i.e., whether the module receives or generates the Frame Synchronization Pulse). The frame pulse is an active-high pulse for a single SPI clock cycle. When Frame Synchronization is enabled, the data transmission starts only on the subsequent transmit edge of the SPI clock.

**FIGURE 14-2: I²C™ BLOCK DIAGRAM**



#### 14.4.1 10-BIT MODE SLAVE TRANSMISSION

Once a slave is addressed in this fashion with the full 10-bit address (we will refer to this state as “PRIOR_ADDR_MATCH”), the master can begin sending data bytes for a slave reception operation.

#### 14.4.2 10-BIT MODE SLAVE RECEPTION

Once addressed, the master can generate a Repeated Start, reset the high byte of the address and set the R_W bit without generating a Stop bit, thus initiating a slave transmit operation.

### 14.5 Automatic Clock Stretch

In the Slave modes, the module can synchronize buffer reads and write to the master device by clock stretching.

#### 14.5.1 TRANSMIT CLOCK STRETCHING

Both 10-bit and 7-bit Transmit modes implement clock stretching by asserting the SCLREL bit after the falling edge of the ninth clock, if the TBF bit is cleared, indicating the buffer is empty.

In Slave Transmit modes, clock stretching is always performed irrespective of the STREN bit.

Clock synchronization takes place following the ninth clock of the transmit sequence. If the device samples an ACK on the falling edge of the ninth clock and if the TBF bit is still clear, then the SCLREL bit is automatically cleared. The SCLREL being cleared to ‘0’ will assert the SCL line low. The user’s ISR must set the SCLREL bit before transmission is allowed to continue. By holding the SCL line low, the user has time to service the ISR and load the contents of the I2CTRN before the master device can initiate another transmit sequence.

| | |
|---|---|
| **Note 1:** | If the user loads the contents of I2CTRN, setting the TBF bit before the falling edge of the ninth clock, the SCLREL bit will not be cleared and clock stretching will not occur. |
| **2:** | The SCLREL bit can be set in software, regardless of the state of the TBF bit. |

#### 14.5.2 RECEIVE CLOCK STRETCHING

The STREN bit in the I2CCON register can be used to enable clock stretching in Slave Receive mode. When the STREN bit is set, the SCL pin will be held low at the end of each data receive sequence.

#### 14.5.3 CLOCK STRETCHING DURING 7-BIT ADDRESSING (STREN = 1)

When the STREN bit is set in Slave Receive mode, the SCL line is held low when the buffer register is full. The method for stretching the SCL output is the same for both 7 and 10-bit addressing modes.

Clock stretching takes place following the ninth clock of the receive sequence. On the falling edge of the ninth clock at the end of the ACK sequence, if the RBF bit is set, the SCLREL bit is automatically cleared, forcing the SCL output to be held low. The user’s ISR must set the SCLREL bit before reception is allowed to continue. By holding the SCL line low, the user has time to service the ISR and read the contents of the I2CRCV before the master device can initiate another receive sequence. This will prevent buffer overruns from occurring.

| | |
|---|---|
| **Note 1:** | If the user reads the contents of the I2CRCV, clearing the RBF bit before the falling edge of the ninth clock, the SCLREL bit will not be cleared and clock stretching will not occur. |
| **2:** | The SCLREL bit can be set in software regardless of the state of the RBF bit. The user should be careful to clear the RBF bit in the ISR before the next receive sequence in order to prevent an overflow condition. |

#### 14.5.4 CLOCK STRETCHING DURING 10-BIT ADDRESSING (STREN = 1)

Clock stretching takes place automatically during the addressing sequence. Because this module has a register for the entire address, it is not necessary for the protocol to wait for the address to be updated.

After the address phase is complete, clock stretching will occur on each data receive or transmit sequence as was described earlier.

### 14.6 Software Controlled Clock Stretching (STREN = 1)

When the STREN bit is ‘1’, the SCLREL bit may be cleared by software to allow software to control the clock stretching. The logic will synchronize writes to the SCLREL bit with the SCL clock. Clearing the SCLREL bit will not assert the SCL output until the module detects a falling edge on the SCL output and SCL is sampled low. If the SCLREL bit is cleared by the user while the SCL line has been sampled low, the SCL output will be asserted (held low). The SCL output will remain low until the SCLREL bit is set, and all other devices on the $I^2C$ bus have de-asserted SCL. This ensures that a write to the SCLREL bit will not violate the minimum high time requirement for SCL.

If the STREN bit is ‘0’, a software write to the SCLREL bit will be disregarded and have no effect on the SCLREL bit.

### 15.5.2 FRAMING ERROR (FERR)

The FERR bit (UxSTA<2>) is set if a '0' is detected instead of a Stop bit. If two Stop bits are selected, both Stop bits must be '1', otherwise FERR will be set. The read-only FERR bit is buffered along with the received data. It is cleared on any Reset.

### 15.5.3 PARITY ERROR (PERR)

The PERR bit (UxSTA<3>) is set if the parity of the received word is incorrect. This error bit is applicable only if a Parity mode (odd or even) is selected. The read-only PERR bit is buffered along with the received data bytes. It is cleared on any Reset.

### 15.5.4 IDLE STATUS

When the receiver is active (i.e., between the initial detection of the Start bit and the completion of the Stop bit), the RIDLE bit (UxSTA<4>) is '0'. Between the completion of the Stop bit and detection of the next Start bit, the RIDLE bit is '1', indicating that the UART is Idle.

### 15.5.5 RECEIVE BREAK

The receiver will count and expect a certain number of bit times based on the values programmed in the PDSEL (UxMODE<2:1>) and STSEL (UxMODE<0>) bits.

If the break is longer than 13 bit times, the reception is considered complete after the number of bit times specified by PDSEL and STSEL. The URXDA bit is set, FERR is set, zeros are loaded into the receive FIFO, interrupts are generated if appropriate and the RIDLE bit is set.

When the module receives a long break signal and the receiver has detected the Start bit, the data bits and the invalid Stop bit (which sets the FERR), the receiver must wait for a valid Stop bit before looking for the next Start bit. It cannot assume that the break condition on the line is the next Start bit.

Break is regarded as a character containing all '0's with the FERR bit set. The Break character is loaded into the buffer. No further reception can occur until a Stop bit is received. Note that RIDLE goes high when the Stop bit has not yet been received.

## 15.6 Address Detect Mode

Setting the ADDEN bit (UxSTA<5>) enables this special mode in which a 9th bit (URX8) value of '1' identifies the received word as an address, rather than data. This mode is only applicable for 9-bit data communication. The URXISEL control bit does not have any impact on interrupt generation in this mode since an interrupt (if enabled) will be generated every time the received word has the 9th bit set.

## 15.7 Loopback Mode

Setting the LPBACK bit enables this special mode in which the UxTX pin is internally connected to the UxRX pin. When configured for the Loopback mode, the UxRX pin is disconnected from the internal UART receive logic. However, the UxTX pin still functions as in a normal operation.

To select this mode:

a) Configure UART for desired mode of operation.
b) Set LPBACK = 1 to enable Loopback mode.
c) Enable transmission as defined in **Section 15.3 "Transmitting Data"**.

## 15.8 Baud Rate Generator

The UART has a 16-bit Baud Rate Generator to allow maximum flexibility in baud rate generation. The Baud Rate Generator register (UxBRG) is readable and writable. The baud rate is computed as follows:

BRG = 16-bit value held in UxBRG register (0 through 65535)

FCY = Instruction Clock Rate (1/TCY)

The baud rate is given by Equation 15-1.

**EQUATION 15-1: BAUD RATE**

$$\text{Baud Rate} = F_{CY} / (16*(BRG+1))$$

Therefore, the maximum baud rate possible is:

FCY /16 (if BRG = 0),

and the minimum baud rate possible is:

FCY / (16* 65536).

With a full 16-bit Baud Rate Generator at 30 MIPS operation, the minimum baud rate achievable is 28.5 bps.

## 15.9 Auto-Baud Support

To allow the system to determine baud rates of received characters, the input can be optionally linked to a selected capture input (IC1 for UART1 and IC2 for UART2). To enable this mode, you must program the input capture module to detect the falling and rising edges of the Start bit.

**TABLE 15-1: UART1 REGISTER MAP FOR dsPIC30F2011/2012/3012/3013**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U1MODE | 020C | UARTEN | — | USIDL | — | — | ALTIO | — | — | WAKE | LPBACK | ABAUD | — | — | PDSEL1 | PDSEL0 | STSEL | 0000 0000 0000 0000 |
| U1STA | 020E | UTXISEL | — | — | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0000 0001 0001 0000 |
| U1TXREG | 0210 | — | — | — | — | — | — | — | UTX8 | Transmit Register | | | | | | | | 0000 000u uuuu uuuu |
| U1RXREG | 0212 | — | — | — | — | — | — | — | URX8 | Receive Register | | | | | | | | 0000 0000 0000 0000 |
| U1BRG | 0214 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**TABLE 15-2: UART2 REGISTER MAP FOR dsPIC30F3013(1)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U2MODE | 0216 | UARTEN | — | USIDL | — | — | — | — | — | WAKE | LPBACK | ABAUD | — | — | PDSEL1 | PDSEL0 | STSEL | 0000 0000 0000 0000 |
| U2STA | 0218 | UTXISEL | — | — | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0000 0001 0001 0000 |
| U2TXREG | 021A | — | — | — | — | — | — | — | UTX8 | Transmit Register | | | | | | | | 0000 000u uuuu uuuu |
| U2RXREG | 021C | — | — | — | — | — | — | — | URX8 | Receive Register | | | | | | | | 0000 0000 0000 0000 |
| U2BRG | 021E | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 0000 0000 0000 |

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**Note 1:** UART2 is not available on dsPIC30F2011/2012/3012 devices.

**2:** Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

## 16.9 Module Power-Down Modes

The module has two internal power modes.

When the ADON bit is '1', the module is in Active mode; it is fully powered and functional.

When ADON is '0', the module is in Off mode. The digital and analog portions of the circuit are disabled for maximum current savings.

In order to return to the Active mode from Off mode, the user must wait for the ADC circuitry to stabilize.

## 16.10 A/D Operation During CPU Sleep and Idle Modes

### 16.10.1 A/D OPERATION DURING CPU SLEEP MODE

When the device enters Sleep mode, all clock sources to the module are shut down and stay at logic '0'.

If Sleep occurs in the middle of a conversion, the conversion is aborted. The converter will not continue with a partially completed conversion on exit from Sleep mode.

Register contents are not affected by the device entering or leaving Sleep mode.

The ADC module can operate during Sleep mode if the A/D clock source is set to RC (ADRC = 1). When the RC clock source is selected, the ADC module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed which eliminates all digital switching noise from the conversion. When the conversion is complete, the CONV bit will be cleared and the result loaded into the ADCBUF register.

If the A/D interrupt is enabled, the device will wake-up from Sleep. If the A/D interrupt is not enabled, the ADC module will then be turned off, although the ADON bit will remain set.

### 16.10.2 A/D OPERATION DURING CPU IDLE MODE

The ADSIDL bit selects if the module will stop on Idle or continue on Idle. If ADSIDL = 0, the module will continue operation on assertion of Idle mode. If ADSIDL = 1, the module will stop on Idle.

## 16.11 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the ADC module to be turned off, and any conversion and sampling sequence is aborted. The values that are in the ADCBUF registers are not modified. The A/D Result register will contain unknown data after a Power-on Reset.

## 16.12 Output Formats

The A/D result is 12 bits wide. The data buffer RAM is also 12 bits wide. The 12-bit data can be read in one of four different formats. The FORM<1:0> bits select the format. Each of the output formats translates to a 16-bit result on the data bus.

**FIGURE 16-4: A/D OUTPUT DATA FORMATS**

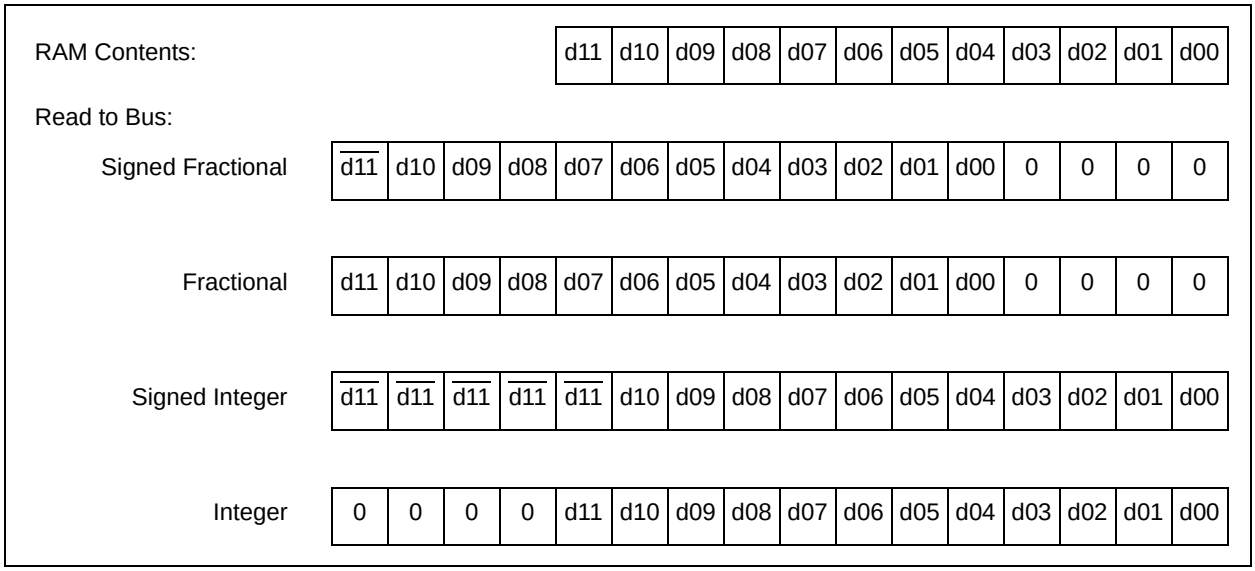
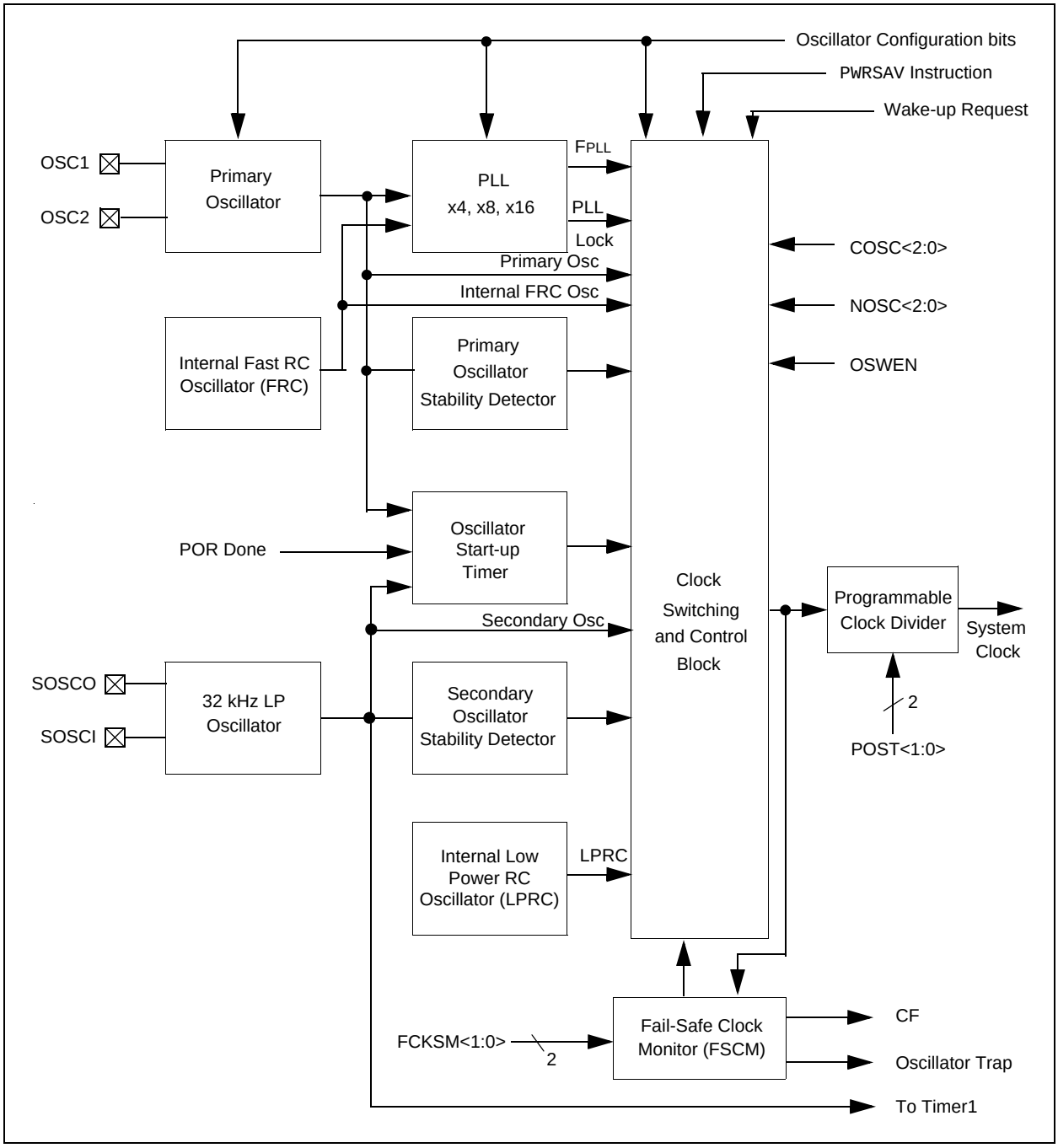


**FIGURE 17-1: OSCILLATOR SYSTEM BLOCK DIAGRAM**



#### 17.3.1.1 POR with Long Crystal Start-up Time (with FSCM Enabled)

The oscillator start-up circuitry is not linked to the POR circuitry. Some crystal circuits (especially low frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after the POR timer and the PWRT have expired:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has not expired (if a crystal oscillator is used).
- The PLL has not achieved a LOCK (if PLL is used).

If the FSCM is enabled and one of the above conditions is true, then a clock failure trap will occur. The device will automatically switch to the FRC oscillator and the user can switch to the desired crystal oscillator in the trap ISR.

#### 17.3.1.2 Operating without FSCM and PWRT

If the FSCM is disabled and the Power-up Timer (PWRT) is also disabled, then the device will exit rapidly from Reset on power-up. If the clock source is FRC, LPRC, ERC or EC, it will be active immediately.

If the FSCM is disabled and the system clock has not started, the device will be in a frozen state at the Reset vector until the system clock starts. From the user's perspective, the device will appear to be in Reset until a system clock is available.

### 17.3.2 BOR: PROGRAMMABLE BROWN-OUT RESET

The BOR (Brown-out Reset) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (i.e., missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

The BOR module allows selection of one of the following voltage trip points (see Table 20-11):

- 2.6V-2.71V
- 4.1V-4.4V
- 4.58V-4.73V

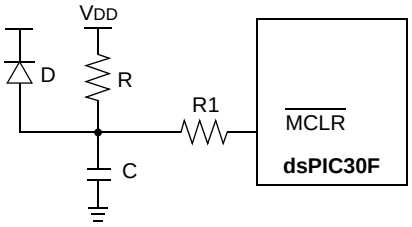
| | |
|---|---|
| **Note:** | The BOR voltage trip points indicated here are nominal values provided for design guidance only. Refer to the Electrical Specifications in the specific device data sheet for BOR voltage limit specifications. |

A BOR will generate a Reset pulse which will reset the device. The BOR will select the clock source based on the device Configuration bit values (FOS<2:0> and FPR<4:0>). Furthermore, if an Oscillator mode is selected, the BOR will activate the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, then the clock will be held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the POR time-out ($T_{POR}$) and the PWRT time-out ($T_{PWRT}$) will be applied before the internal Reset is released. If $T_{PWRT}$ = 0 and a crystal oscillator is being used, then a nominal delay of $T_{FSCM}$ = 100 µs is applied. The total delay in this case is ($T_{POR}$ + $T_{FSCM}$).

The BOR Status bit (RCON<1>) will be set to indicate that a BOR has occurred. The BOR circuit, if enabled, will continue to operate while in Sleep or Idle modes and will reset the device should $V_{DD}$ fall below the BOR threshold voltage.

**FIGURE 17-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW $V_{DD}$ POWER-UP)**




**Note 1:** External Power-on Reset circuit is required only if the $V_{DD}$ power-up slope is too slow. The diode D helps discharge the capacitor quickly when $V_{DD}$ powers down.

**2:** R should be suitably chosen so as to make sure that the voltage drop across R does not violate the device's electrical specifications.

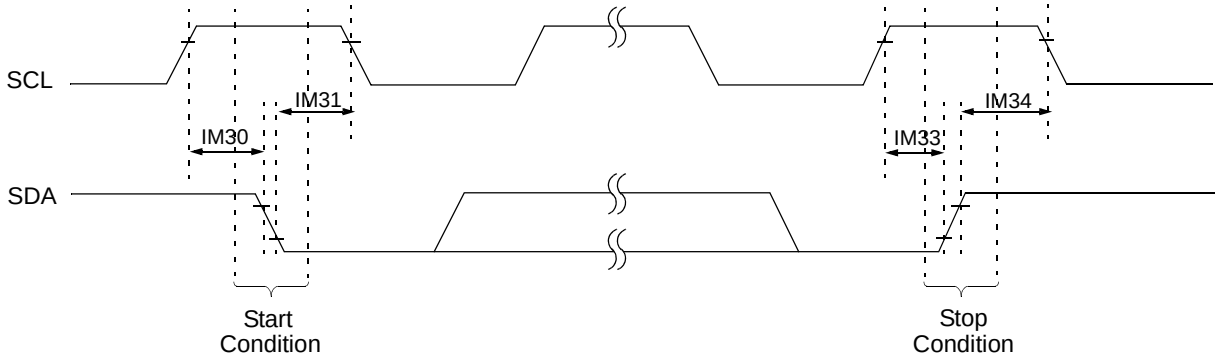
**3:** R1 should be suitably chosen so as to limit any current flowing into $\overline{MCLR}$ from external capacitor C, in the event of $\overline{MCLR}/V_{PP}$ pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

| | |
|---|---|
| **Note:** | Dedicated supervisory devices, such as the MCP1XX and MCP8XX, may also be used as an external Power-on Reset circuit. |

**TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

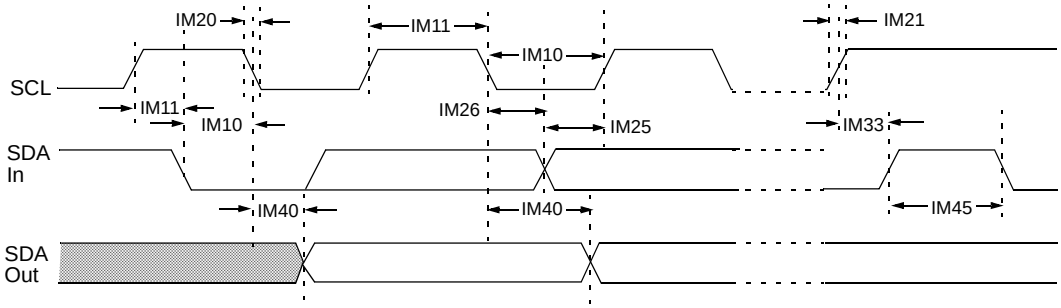
| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 66 | RRNC | RRNC | f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC | Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 67 | SAC | SAC | Acc,#Slit4,Wdo | Store Accumulator | 1 | 1 | None |
| | | SAC.R | Acc,#Slit4,Wdo | Store Rounded Accumulator | 1 | 1 | None |
| 68 | SE | SE | Ws,Wnd | Wnd = sign-extended Ws | 1 | 1 | C,N,Z |
| 69 | SETM | SETM | f | f = 0xFFFF | 1 | 1 | None |
| | | SETM | WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM | Ws | Ws = 0xFFFF | 1 | 1 | None |
| 70 | SFTAC | SFTAC | Acc,Wn | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC | Acc,#Slit6 | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 71 | SL | SL | f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | f,WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | Ws,Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL | Wb,Wns,Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL | Wb,#lit5,Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 72 | SUB | SUB | Acc | Subtract Accumulators | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SUB | f | f = f - WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | f,WREG | WREG = f - WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | #lit10,Wn | Wn = Wn - lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,Ws,Wd | Wd = Wb - Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,#lit5,Wd | Wd = Wb - lit5 | 1 | 1 | C,DC,N,OV,Z |
| 73 | SUBB | SUBB | f | f = f - WREG - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | f,WREG | WREG = f - WREG - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | #lit10,Wn | Wn = Wn - lit10 - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,Ws,Wd | Wd = Wb - Ws - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,#lit5,Wd | Wd = Wb - lit5 - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 74 | SUBR | SUBR | f | f = WREG - f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | f,WREG | WREG = WREG - f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,Ws,Wd | Wd = Ws - Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,#lit5,Wd | Wd = lit5 - Wb | 1 | 1 | C,DC,N,OV,Z |
| 75 | SUBBR | SUBBR | f | f = WREG - f - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | f,WREG | WREG = WREG -f - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,Ws,Wd | Wd = Ws - Wb - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,#lit5,Wd | Wd = lit5 - Wb - ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 76 | SWAP | SWAP.b | Wn | Wn = nibble swap Wn | 1 | 1 | None |
| | | SWAP | Wn | Wn = byte swap Wn | 1 | 1 | None |
| 77 | TBLRDH | TBLRDH | Ws,Wd | Read Prog<23:16> to Wd<7:0> | 1 | 2 | None |
| 78 | TBLRDL | TBLRDL | Ws,Wd | Read Prog<15:0> to Wd | 1 | 2 | None |
| 79 | TBLWTH | TBLWTH | Ws,Wd | Write Ws<7:0> to Prog<23:16> | 1 | 2 | None |
| 80 | TBLWTL | TBLWTL | Ws,Wd | Write Ws to Prog<15:0> | 1 | 2 | None |
| 81 | ULNK | ULNK | | Unlink frame pointer | 1 | 1 | None |
| 82 | XOR | XOR | f | f = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | f,WREG | WREG = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | #lit10,Wn | Wd = lit10 .XOR. Wd | 1 | 1 | N,Z |
| | | XOR | Wb,Ws,Wd | Wd = Wb .XOR. Ws | 1 | 1 | N,Z |
| | | XOR | Wb,#lit5,Wd | Wd = Wb .XOR. lit5 | 1 | 1 | N,Z |
| 83 | ZE | ZE | Ws,Wnd | Wnd = Zero-extend Ws | 1 | 1 | C,Z,N |

**FIGURE 20-16: I²C™ BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 20-3 for load conditions.

**FIGURE 20-17: I²C™ BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 20-3 for load conditions.

**TABLE 20-33: I²C™ BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min(1)** | **Max** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 1) | — | µs | |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 1) | — | µs | |
| IM20 | TF:SCL | SDA and SCL Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 100 | ns | |
| IM21 | TR:SCL | SDA and SCL Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(2) | — | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | ns | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(2) | — | — | ns | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 1) | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 1) | — | µs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 1) | — | µs | After this period the first clock pulse is generated |
| | | | 400 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 1) | — | µs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 1) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 1) | — | µs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 1) | — | ns | |
| | | | 400 kHz mode | TCY/2 (BRG + 1) | — | ns | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 1) | — | ns | |
| IM40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | — | 3500 | ns | |
| | | | 400 kHz mode | — | 1000 | ns | |
| | | | 1 MHz mode(2) | — | — | ns | |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(2) | — | — | µs | |
| IM50 | CB | Bus Capacitive Loading | | — | 400 | pF | |

**Note 1:** BRG is the value of the I²C Baud Rate Generator. Refer to **Section 21. "Inter-Integrated Circuit™ (I²C)"** (DS70068) in the *dsPIC30F Family Reference Manual* (DS70046).

**2:** Maximum pin capacitance = 10 pF for all I²C™ pins (for 1 MHz mode only).

**FIGURE 20-18: I²C™ BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

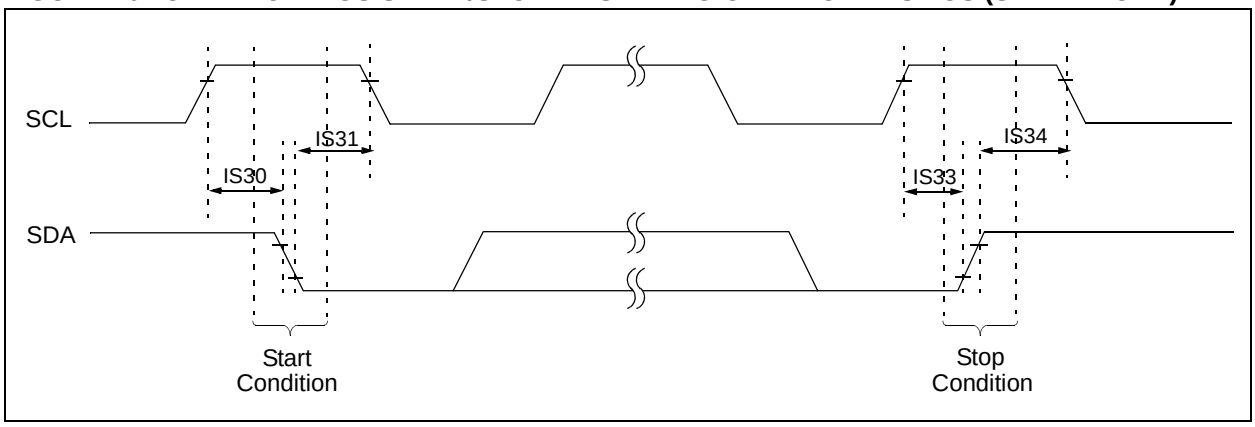



**FIGURE 20-19: I²C™ BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

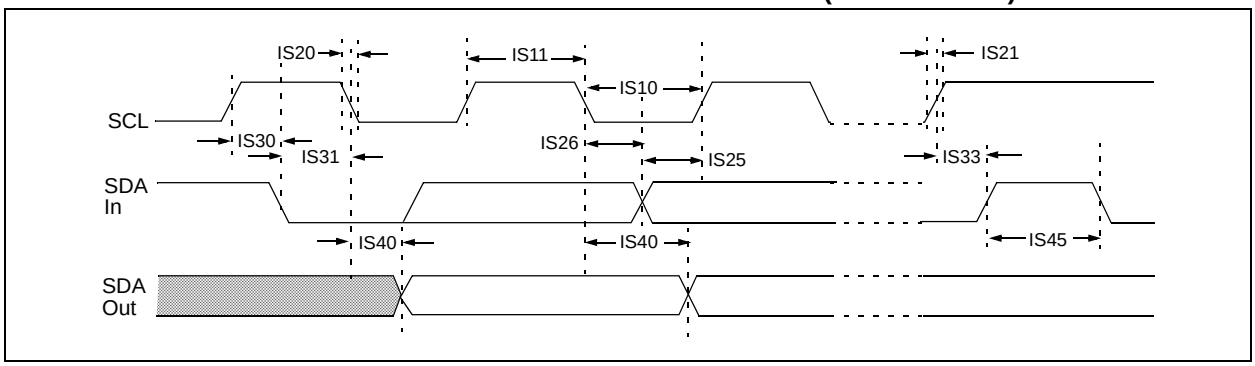


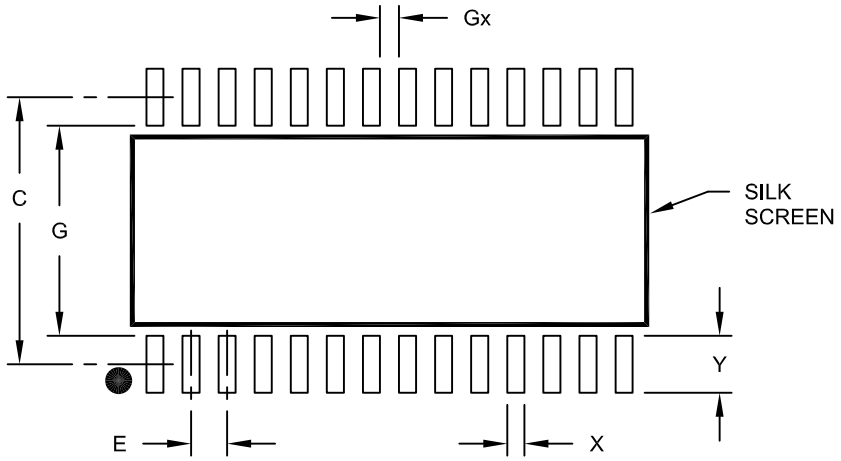

**TABLE 20-34: I²C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)**<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 1.3 | — | µs | Device must operate at a minimum of 10 MHz. |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Device must operate at a minimum of 10 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS20 | TF:SCL | SDA and SCL Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 100 | ns | |
| IS21 | TR:SCL | SDA and SCL Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 300 | ns | |

**Note 1:** Maximum pin capacitance = 10 pF for all I²C™ pins (for 1 MHz mode only).

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width (X28) | X | | | 0.60 |
| Contact Pad Length (X28) | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:

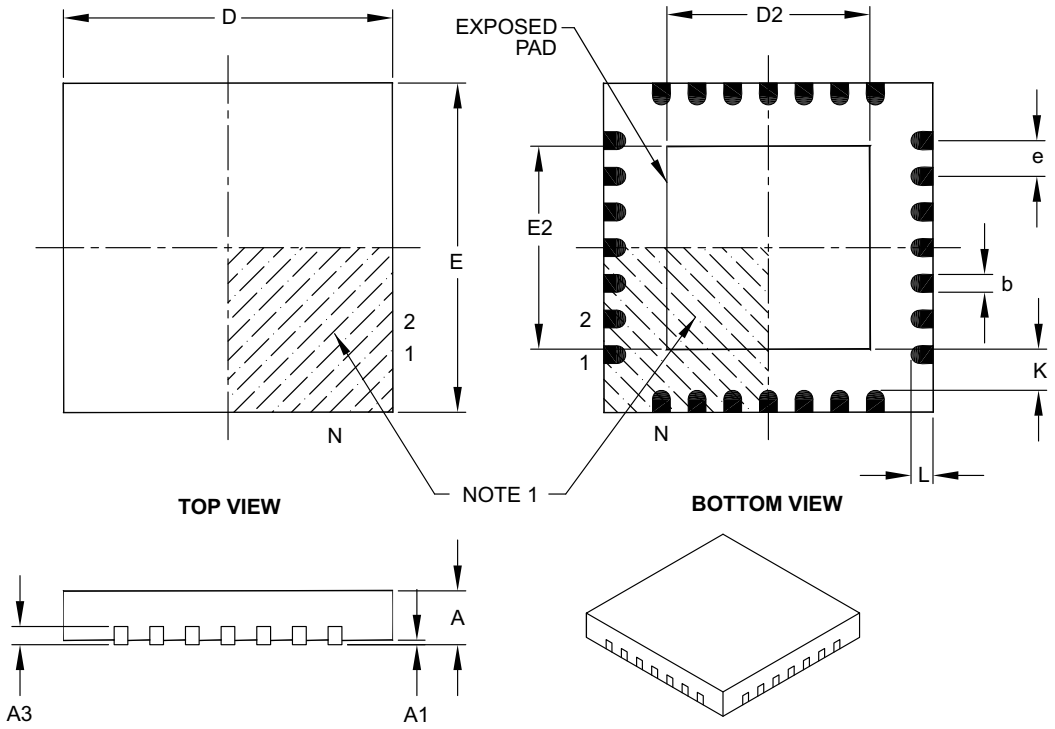
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

## 28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.70 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.70 |
| Contact Width | b | 0.23 | 0.38 | 0.43 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124B

# INDEX

## Numerics



## A



## B



## C



## D