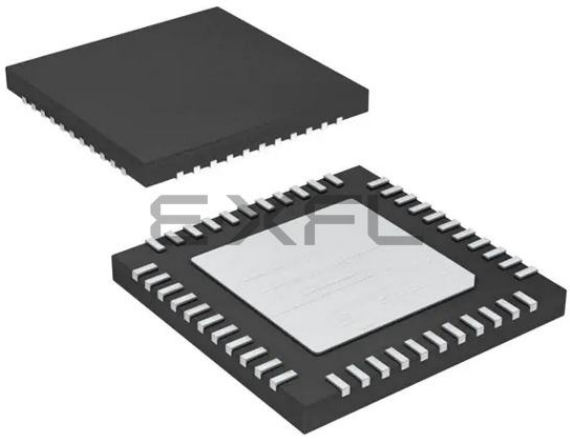

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 30 MIPs |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 20 |
| Program Memory Size | 24KB (8K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | 1K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.5V ~ 5.5V |
| Data Converters | A/D 10x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3013-30i-ml |

# High-Performance, 16-bit Digital Signal Controllers

**Note:** This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*16-bit MCU and DSC Programmer's Reference Manual*" (DS70157).

## High-Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture
- Flexible addressing modes
- 83 base instructions
- 24-bit wide instructions, 16-bit wide data path
- Up to 24 Kbytes on-chip Flash program space
- Up to 2 Kbytes of on-chip data RAM
- Up to 1 Kbytes of nonvolatile data EEPROM
- 16 x 16-bit working register array
- Up to 30 MIPS operation:
  - DC to 40 MHz external clock input
  - 4 MHz - 10 MHz oscillator input with PLL active (4x, 8x, 16x)
- Up to 21 interrupt sources:
  - 8 user-selectable priority levels
  - 3 external interrupt sources
  - 4 processor trap sources

## DSP Features:

- Dual data fetch
- Modulo and Bit-Reversed modes
- Two 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single-cycle hardware fractional/ integer multiplier
- All DSP instructions are single cycle
  - Multiply-Accumulate (MAC) operation
- Single-cycle ±16 shift

## Peripheral Features:

- High-current sink/source I/O pins: 25 mA/25 mA
- Three 16-bit timers/counters; optionally pair up 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 3-wire SPI modules (supports four Frame modes)
- $I^2C$™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- Up to two addressable UART modules with FIFO buffers

## Analog Features:

- 12-bit Analog-to-Digital Converter (ADC) with:
  - 200 ksps conversion rate
  - Up to 10 input channels
  - Conversion available during Sleep and Idle
- Programmable Low-Voltage Detection (PLVD)
- Programmable Brown-out Reset

## Special Microcontroller Features:

- Enhanced Flash program memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100K (typical)
- Data EEPROM memory:
  - 100,000 erase/write cycle (min.) for industrial temperature range, 1M (typical)
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with on-chip low-power RC oscillator for reliable operation
- Fail-Safe Clock Monitor operation:
  - Detects clock failure and switches to on-chip low-power RC oscillator
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™)
- Selectable Power Management modes:
  - Sleep, Idle and Alternate Clock modes

## CMOS Technology:

- Low-power, high-speed Flash technology
- Wide operating voltage range (2.5V to 5.5V)
- Industrial and Extended temperature ranges
- Low-power consumption

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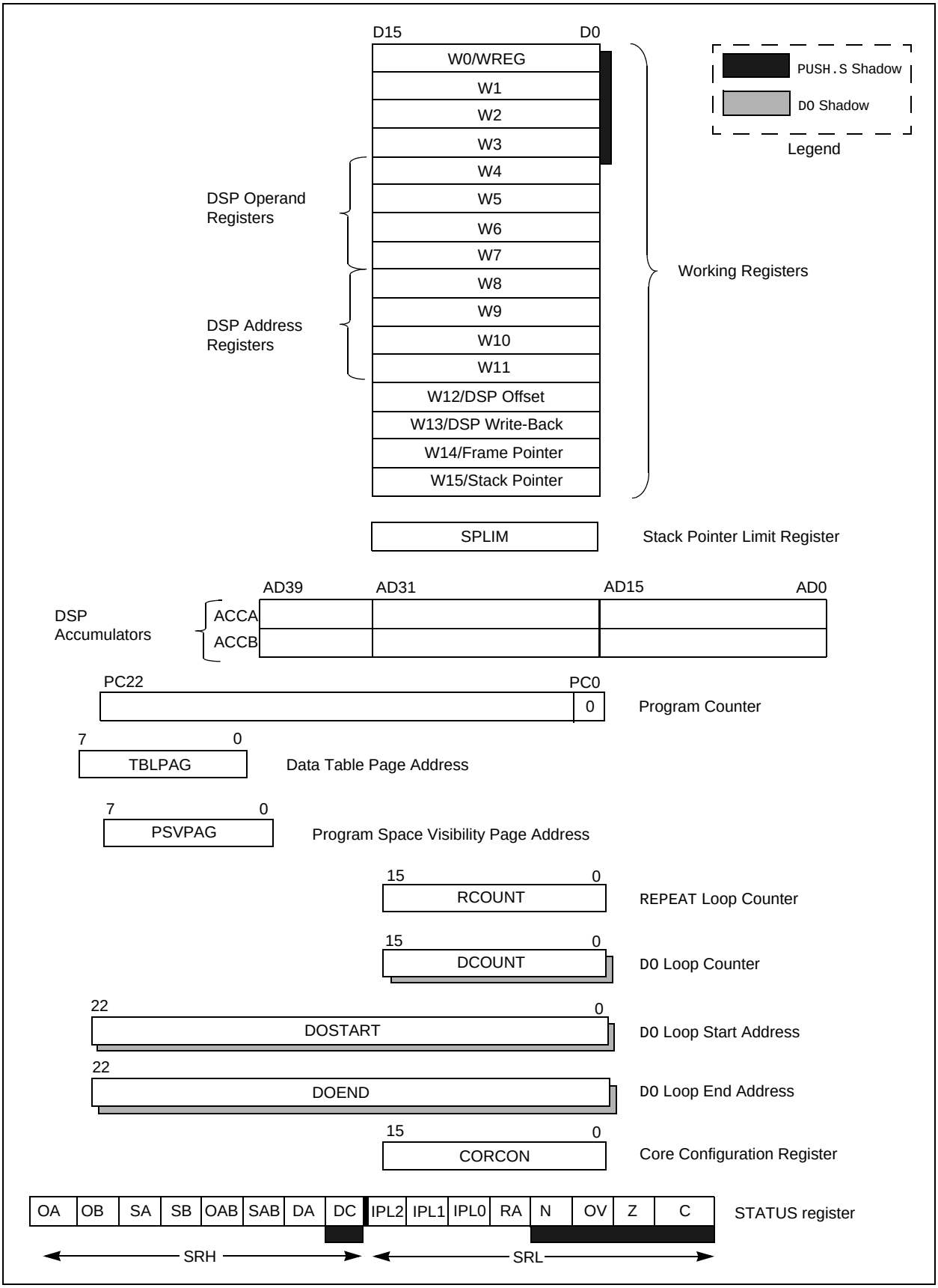
**FIGURE 2-1: PROGRAMMER'S MODEL**



### 4.1.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

| | |
|---|---|
| **Note:** | For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (register offset) field is shared between both source and destination (but typically only used by one). |

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

| | |
|---|---|
| **Note:** | Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes. |

### 4.1.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, utilize a simplified set of addressing modes to allow the user to effectively manipulate the data pointers through register indirect tables.

The two source operand prefetch registers must belong to the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU. W10 and W11 are always directed to the Y AGU. The effective addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

| | |
|---|---|
| **Note:** | Register Indirect with Register Offset addressing is only available for W9 (in X space) and W11 (in Y space). |

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-modified by 2
- Register Indirect Post-modified by 4
- Register Indirect Post-modified by 6
- Register Indirect with Register Offset (Indexed)

### 4.1.5 OTHER INSTRUCTIONS

Besides the various addressing modes outlined above, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ADD Acc, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

## 4.2 Modulo Addressing

Modulo Addressing is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can only be configured to operate in one direction, as there are certain restrictions on the buffer Start address (for incrementing buffers), or end address (for decrementing buffers) based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-2 length. As these buffers satisfy the Start and the end address criteria, they can operate in a Bidirectional mode (i.e., address boundary checks are performed on both the lower and upper address boundaries).

## 6.2 Erasing Data EEPROM

### 6.2.1 ERASING A BLOCK OF DATA EEPROM

In order to erase a block of data EEPROM, the NVMADRU and NVMADR registers must initially point to the block of memory to be erased. Configure NVMCON for erasing a block of data EEPROM and set the WR and WREN bits in the NVMCON register. Setting the WR bit initiates the erase, as shown in Example 6-2.

**EXAMPLE 6-2: DATA EEPROM BLOCK ERASE**

```
; Select data EEPROM block, WR, WREN bits
    MOV     #0x4045,W0
    MOV     W0,NVMCON                   ; Initialize NVMCON SFR

; Start erase cycle by setting WR after writing key sequence
    DISI    #5                          ; Block all interrupts with priority <7 for
                                        ; next 5 instructions
    MOV     #0x55,W0                    ;
    MOV     W0,NVMKEY                   ; Write the 0x55 key
    MOV     #0xAA,W1                    ;
    MOV     W1,NVMKEY                   ; Write the 0xAA key
    BSET    NVMCON,#WR                  ; Initiate erase sequence
    NOP
    NOP
; Erase cycle will complete in 2mS. CPU is not stalled for the Data Erase Cycle
; User can poll WR bit, use NVMIF or Timer IRQ to determine erasure complete
```

### 6.2.2 ERASING A WORD OF DATA EEPROM

The NVMADRU and NVMADR registers must point to the block. Select WR a block of data Flash and set the WR and WREN bits in the NVMCON register. Setting the WR bit initiates the erase, as shown in Example 6-3.

**EXAMPLE 6-3: DATA EEPROM WORD ERASE**

```
; Select data EEPROM word, WR, WREN bits
    MOV     #0x4044,W0
    MOV     W0,NVMCON

; Start erase cycle by setting WR after writing key sequence
    DISI    #5                          ; Block all interrupts with priority <7 for
                                        ; next 5 instructions
    MOV     #0x55,W0                    ;
    MOV     W0,NVMKEY                   ; Write the 0x55 key
    MOV     #0xAA,W1                    ;
    MOV     W1,NVMKEY                   ; Write the 0xAA key
    BSET    NVMCON,#WR                  ; Initiate erase sequence
    NOP
    NOP
; Erase cycle will complete in 2mS. CPU is not stalled for the Data Erase Cycle
; User can poll WR bit, use NVMIF or Timer IRQ to determine erasure complete
```

## 8.2 Reset Sequence

A Reset is not a true exception because the interrupt controller is not involved in the Reset process. The processor initializes its registers in response to a Reset which forces the PC to zero. The processor then begins program execution at location 0x000000. A GOTO instruction is stored in the first program memory location immediately followed by the address target for the GOTO instruction. The processor executes the GOTO to the specified address and then begins operation at the specified target (start) address.

### 8.2.1 RESET SOURCES

In addition to external Reset and Power-on Reset (POR), there are six sources of error conditions which 'trap' to the Reset vector.

- Watchdog Time-out:
  The watchdog has timed out, indicating that the processor is no longer executing the correct flow of code.
- Uninitialized W Register Trap:
  An attempt to use an uninitialized W register as an Address Pointer causes a Reset.
- Illegal Instruction Trap:
  Attempted execution of any unused opcodes results in an illegal instruction trap. Note that a fetch of an illegal instruction does not result in an illegal instruction trap if that instruction is flushed prior to execution due to a flow change.
- Brown-out Reset (BOR):
  A momentary dip in the power supply to the device has been detected which may result in malfunction.
- Trap Lockout:
  Occurrence of multiple trap conditions simultaneously causes a Reset.

## 8.3 Traps

Traps can be considered as non-maskable interrupts indicating a software or hardware error, which adhere to a predefined priority as shown in Figure 8-1. They are intended to provide the user a means to correct erroneous operation during debug and when operating within the application.

| | |
|---|---|
| **Note:** | If the user does not intend to take corrective action in the event of a trap error condition, these vectors must be loaded with the address of a default handler that contains the RESET instruction. If, on the other hand, one of the vectors containing an invalid address is called, an address error trap is generated. |

Note that many of these trap conditions can only be detected when they occur. Consequently, the questionable instruction is allowed to complete prior to trap exception processing. If the user chooses to recover from the error, the result of the erroneous action that caused the trap may have to be corrected.

There are eight fixed priority levels for traps: Level 8 through Level 15, which implies that the IPL3 is always set during processing of a trap.

If the user is not currently executing a trap, and he sets the IPL<3:0> bits to a value of '0111' (Level 7), then all interrupts are disabled, but traps can still be processed.

### 8.3.1 TRAP SOURCES

The following traps are provided with increasing priority. However, since all traps can be nested, priority has little effect.

#### Math Error Trap:

The math error trap executes under the following four circumstances:

1. If an attempt is made to divide by zero, the divide operation is aborted on a cycle boundary and the trap is taken.
2. If enabled, a math error trap is taken when an arithmetic operation on either accumulator A or B causes an overflow from bit 31 and the accumulator guard bits are not utilized.
3. If enabled, a math error trap is taken when an arithmetic operation on either accumulator A or B causes a catastrophic overflow from bit 39 and all saturation is disabled.
4. If the shift amount specified in a shift instruction is greater than the maximum allowed shift amount, a trap occurs.

### 12.4.2 PWM PERIOD

The PWM period is specified by writing to the PRx register. The PWM period can be calculated using Equation 12-1.

**EQUATION 12-1:**

$$PWM\ period = [(PRx) + 1] \cdot 4 \cdot Tosc \cdot (TMRx\ prescale\ value)$$

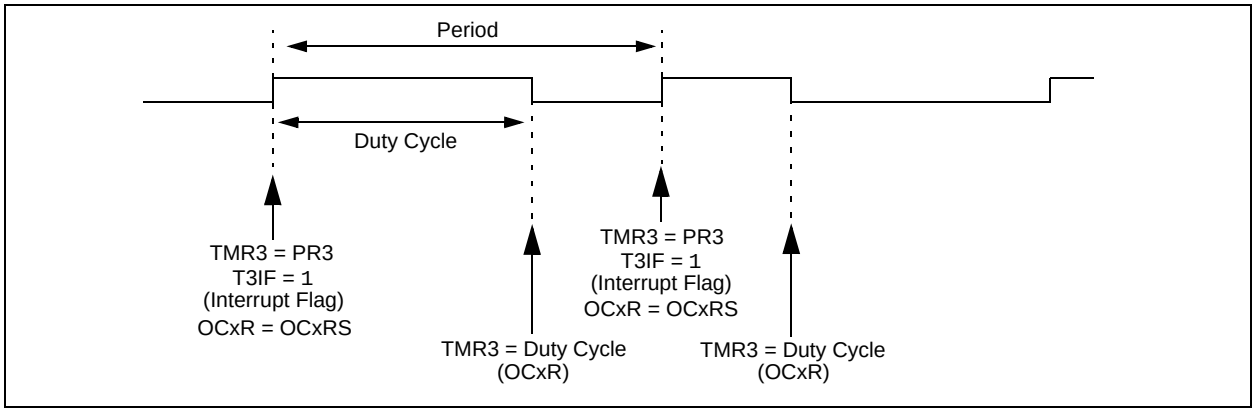
PWM frequency is defined as 1/[PWM period].

When the selected TMRx is equal to its respective period register, PRx, the following four events occur on the next increment cycle:

- TMRx is cleared.
- The OCx pin is set.
  - Exception 1: If PWM duty cycle is 0x0000, the OCx pin remains low.
  - Exception 2: If duty cycle is greater than PRx, the pin remains high.
- The PWM duty cycle is latched from OCxRS into OCxR.
- The corresponding timer interrupt flag is set.

See Figure 12-2 for key PWM period comparisons. Timer3 is referred to in Figure 12-2 for clarity.

**FIGURE 12-2: PWM OUTPUT TIMING**



## 16.13 Configuring Analog Port Pins

The use of the ADPCFG and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bit set (input). If the TRIS bit is cleared (output), the digital output level ($V_{OH}$ or $V_{OL}$) will be converted.

The A/D operation is independent of the state of the CH0SA<3:0>/CH0SB<3:0> bits and the TRIS bits.

When reading the PORT register, all pins configured as analog input channels will read as cleared.

Pins configured as digital inputs will not convert an analog input. Analog levels on any pin that is defined as a digital input (including the ANx pins) may cause the input buffer to consume current that exceeds the device specifications.

## 16.14 Connection Considerations

The analog inputs have diodes to $V_{DD}$ and $V_{SS}$ as ESD protection. This requires that the analog input be between $V_{DD}$ and $V_{SS}$. If the input voltage exceeds this range by greater than 0.3V (either direction), one of the diodes becomes forward biased and it may damage the device if the input current specification is exceeded.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the sampling time requirements are satisfied. Any external components connected (via high-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

**TABLE 16-2: A/D CONVERTER REGISTER MAP FOR dsPIC30F2011/3012**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADCBUF0 | 0280 | — | — | — | — | ADC Data Buffer 0 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF1 | 0282 | — | — | — | — | ADC Data Buffer 1 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF2 | 0284 | — | — | — | — | ADC Data Buffer 2 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF3 | 0286 | — | — | — | — | ADC Data Buffer 3 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF4 | 0288 | — | — | — | — | ADC Data Buffer 4 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF5 | 028A | — | — | — | — | ADC Data Buffer 5 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF6 | 028C | — | — | — | — | ADC Data Buffer 6 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF7 | 028E | — | — | — | — | ADC Data Buffer 7 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF8 | 0290 | — | — | — | — | ADC Data Buffer 8 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUF9 | 0292 | — | — | — | — | ADC Data Buffer 9 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUFA | 0294 | — | — | — | — | ADC Data Buffer 10 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUFB | 0296 | — | — | — | — | ADC Data Buffer 11 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUFC | 0298 | — | — | — | — | ADC Data Buffer 12 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUFD | 029A | — | — | — | — | ADC Data Buffer 13 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUFE | 029C | — | — | — | — | ADC Data Buffer 14 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCBUFF | 029E | — | — | — | — | ADC Data Buffer 15 | | | | | | | | | | | | 0000 uuuu uuuu uuuu |
| ADCON1 | 02A0 | ADON | — | ADSIDL | — | — | — | FORM<1:0> | | SSRC<2:0> | | | — | — | ASAM | SAMP | DONE | 0000 0000 0000 0000 |
| ADCON2 | 02A2 | VCFG<2:0> | | | — | — | CSCNA | — | — | BUFS | — | SMPI<3:0> | | | | BUFM | ALTS | 0000 0000 0000 0000 |
| ADCON3 | 02A4 | — | — | — | SAMC<4:0> | | | | | ADRC | — | ADCS<5:0> | | | | | | 0000 0000 0000 0000 |
| ADCHS | 02A6 | — | — | — | CH0NB | CH0SB<3:0> | | | | — | — | — | CH0NA | CH0SA<3:0> | | | | 0000 0000 0000 0000 |
| ADPCFG | 02A8 | — | — | — | — | — | — | — | — | PCFG7 | PCFG6 | PCFG5 | PCFG4 | PCFG3 | PCFG2 | PCFG1 | PCFG0 | 0000 0000 0000 0000 |
| ADCSSL | 02AA | — | — | — | — | — | — | — | — | CSSL7 | CSSL6 | CSSL5 | CSSL4 | CSSL3 | CSSL2 | CSSL1 | CSSL0 | 0000 0000 0000 0000 |

**Legend:** u = uninitialized bit; — = unimplemented bit, read as '0'

**Note:** Refer to the "*dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

**TABLE 17-1: OSCILLATOR OPERATING MODES**

| Oscillator Mode | Description |
|---|---|
| XTL | 200 kHz-4 MHz crystal on OSC1:OSC2. |
| XT | 4 MHz-10 MHz crystal on OSC1:OSC2. |
| XT w/PLL 4x | 4 MHz-10 MHz crystal on OSC1:OSC2, 4x PLL enabled. |
| XT w/PLL 8x | 4 MHz-10 MHz crystal on OSC1:OSC2, 8x PLL enabled. |
| XT w/PLL 16x | 4 MHz-7.5 MHz crystal on OSC1:OSC2, 16x PLL enabled(1). |
| LP | 32 kHz crystal on SOSCO:SOSCI(2). |
| HS | 10 MHz-25 MHz crystal. |
| HS/2 w/PLL 4x | 10 MHz-20 MHz crystal, divide by 2, 4x PLL enabled. |
| HS/2 w/PLL 8x | 10 MHz-20 MHz crystal, divide by 2, 8x PLL enabled. |
| HS/2 w/PLL 16x | 10 MHz-15 MHz crystal, divide by 2, 16x PLL enabled(1). |
| HS/3 w/PLL 4x | 12 MHz-25 MHz crystal, divide by 3, 4x PLL enabled. |
| HS/3 w/PLL 8x | 12 MHz-25 MHz crystal, divide by 3, 8x PLL enabled. |
| HS/3 w/PLL 16x | 12 MHz-22.5 MHz crystal, divide by 3, 16x PLL enabled(1). |
| EC | External clock input (0-40 MHz). |
| ECIO | External clock input (0-40 MHz), OSC2 pin is I/O. |
| EC w/PLL 4x | External clock input (4-10 MHz), OSC2 pin is I/O, 4x PLL enabled. |
| EC w/PLL 8x | External clock input (4-10 MHz), OSC2 pin is I/O, 8x PLL enabled. |
| EC w/PLL 16x | External clock input (4-7.5 MHz), OSC2 pin is I/O, 16x PLL enabled(1). |
| ERC | External RC oscillator, OSC2 pin is FOSC/4 output(3). |
| ERCIO | External RC oscillator, OSC2 pin is I/O(3). |
| FRC | 7.37 MHz internal RC oscillator. |
| FRC w/PLL 4x | 7.37 MHz Internal RC oscillator, 4x PLL enabled. |
| FRC w/PLL 8x | 7.37 MHz Internal RC oscillator, 8x PLL enabled. |
| FRC w/PLL 16x | 7.37 MHz Internal RC oscillator, 16x PLL enabled. |
| LPRC | 512 kHz internal RC oscillator. |

**Note 1:** dsPIC30F maximum operating frequency of 120 MHz must be met.

**2:** LP oscillator can be conveniently shared as system clock, as well as real-time clock for Timer1.

**3:** Requires external R and C. Frequency operation up to 4 MHz.

### 17.2.3 LP OSCILLATOR CONTROL

Enabling the LP oscillator is controlled with two elements:

- The current oscillator group bits COSC<2:0>.
- The LPOSCEN bit (OSCCON register).

The LP oscillator is on (even during Sleep mode) if LPOSCEN = 1. The LP oscillator is the device clock if:

- COSC<2:0> = 000 (LP selected as main osc.) and
- LPOSCEN = 1

Keeping the LP oscillator on at all times allows for a fast switch to the 32 kHz system clock for lower power operation. Returning to the faster main oscillator will still require a start-up time

### 17.2.4 PHASE LOCKED LOOP (PLL)

The PLL multiplies the clock which is generated by the primary oscillator or Fast RC oscillator. The PLL is selectable to have either gains of x4, x8, and x16. Input and output frequency ranges are summarized in Table 17-3.

**TABLE 17-3: PLL FREQUENCY RANGE**

| FIN | PLL Multiplier | FOUT |
|---|---|---|
| 4 MHz-10 MHz | x4 | 16 MHz-40 MHz |
| 4 MHz-10 MHz | x8 | 32 MHz-80 MHz |
| 4 MHz-7.5 MHz | x16 | 64 MHz-120 MHz |

The PLL features a lock output which is asserted when the PLL enters a phase locked state. Should the loop fall out of lock (e.g., due to noise), the lock signal will be rescinded. The state of this signal is reflected in the read-only LOCK bit in the OSCCON register.

### 17.2.5 FAST RC OSCILLATOR (FRC)

The FRC oscillator is a fast (7.37 MHz ±2% nominal) internal RC oscillator. This oscillator is intended to provide reasonable device operating speeds without the use of an external crystal, ceramic resonator, or RC network. The FRC oscillator can be used with the PLL to obtain higher clock frequencies.

The dsPIC30F operates from the FRC oscillator whenever the current oscillator selection control bits in the OSCCON register (OSCCON<14:12>) are set to '001'.

The four bit field specified by TUN<3:0> (OSCTUN <3:0>) allows the user to tune the internal fast RC oscillator (nominal 7.37 MHz). The user can tune the FRC oscillator within a range of +10.5% (840 kHz) and -12% (960 kHz) in steps of 1.50% around the factory calibrated setting, as shown in Table 17-4.

**Note:** OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested.

If OSCCON<14:12> are set to '111' and FPR<4:0> are set to '00001', '01010' or '00011', a PLL multiplier of 4, 8 or 16 (respectively) is applied.

**Note:** When a 16x PLL is used, the FRC frequency must not be tuned to a frequency greater than 7.5 MHz.

**TABLE 17-4: FRC TUNING**

| TUN<3:0> Bits | FRC Frequency |
|---|---|
| 0111 | + 10.5% |
| 0110 | + 9.0% |
| 0101 | + 7.5% |
| 0100 | + 6.0% |
| 0011 | + 4.5% |
| 0010 | + 3.0% |
| 0001 | + 1.5% |
| 0000 | Center Frequency (oscillator is running at calibrated frequency) |
| 1111 | - 1.5% |
| 1110 | - 3.0% |
| 1101 | - 4.5% |
| 1100 | - 6.0% |
| 1011 | - 7.5% |
| 1010 | - 9.0% |
| 1001 | - 10.5% |
| 1000 | - 12.0% |

### 17.2.6 LOW-POWER RC OSCILLATOR (LPRC)

The LPRC oscillator is a component of the Watchdog Timer (WDT) and oscillates at a nominal frequency of 512 kHz. The LPRC oscillator is the clock source for the Power-up Timer (PWRT) circuit, WDT and clock monitor circuits. It may also be used to provide a low-frequency clock source option for applications where power consumption is critical and timing accuracy is not required.

The LPRC oscillator is always enabled at a Power-on Reset because it is the clock source for the PWRT. After the PWRT expires, the LPRC oscillator will remain on if one of the following is true:

- The Fail-Safe Clock Monitor is enabled
- The WDT is enabled
- The LPRC oscillator is selected as the system clock via the COSC<2:0> control bits in the OSCCON register

If one of the above conditions is not true, the LPRC will shut-off after the PWRT expires.

**Note 1:** OSC2 pin function is determined by the Primary Oscillator mode selection (FPR<4:0>).

**2:** OSC1 pin cannot be used as an I/O pin even if the secondary oscillator or an internal clock source is selected at all times.

**TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|
| 9 | BTG | BTG f,#bit4 | Bit Toggle f | 1 | 1 | None |
| | | BTG Ws,#bit4 | Bit Toggle Ws | 1 | 1 | None |
| 10 | BTSC | BTSC f,#bit4 | Bit Test f, Skip if Clear | 1 | 1 (2 or 3) | None |
| | | BTSC Ws,#bit4 | Bit Test Ws, Skip if Clear | 1 | 1 (2 or 3) | None |
| 11 | BTSS | BTSS f,#bit4 | Bit Test f, Skip if Set | 1 | 1 (2 or 3) | None |
| | | BTSS Ws,#bit4 | Bit Test Ws, Skip if Set | 1 | 1 (2 or 3) | None |
| 12 | BTST | BTST f,#bit4 | Bit Test f | 1 | 1 | Z |
| | | BTST.C Ws,#bit4 | Bit Test Ws to C | 1 | 1 | C |
| | | BTST.Z Ws,#bit4 | Bit Test Ws to Z | 1 | 1 | Z |
| | | BTST.C Ws,Wb | Bit Test Ws<Wb> to C | 1 | 1 | C |
| | | BTST.Z Ws,Wb | Bit Test Ws<Wb> to Z | 1 | 1 | Z |
| 13 | BTSTS | BTSTS f,#bit4 | Bit Test then Set f | 1 | 1 | Z |
| | | BTSTS.C Ws,#bit4 | Bit Test Ws to C, then Set | 1 | 1 | C |
| | | BTSTS.Z Ws,#bit4 | Bit Test Ws to Z, then Set | 1 | 1 | Z |
| 14 | CALL | CALL lit23 | Call subroutine | 2 | 2 | None |
| | | CALL Wn | Call indirect subroutine | 1 | 2 | None |
| 15 | CLR | CLR f | f = 0x0000 | 1 | 1 | None |
| | | CLR WREG | WREG = 0x0000 | 1 | 1 | None |
| | | CLR Ws | Ws = 0x0000 | 1 | 1 | None |
| | | CLR Acc,Wx,Wxd,Wy,Wyd,AWB | Clear Accumulator | 1 | 1 | OA,OB,SA,SB |
| 16 | CLRWDT | CLRWDT | Clear Watchdog Timer | 1 | 1 | WDTO,Sleep |
| 17 | COM | COM f | f = $\overline{f}$ | 1 | 1 | N,Z |
| | | COM f,WREG | WREG = $\overline{f}$ | 1 | 1 | N,Z |
| | | COM Ws,Wd | Wd = $\overline{Ws}$ | 1 | 1 | N,Z |
| 18 | CP | CP f | Compare f with WREG | 1 | 1 | C,DC,N,OV,Z |
| | | CP Wb,#lit5 | Compare Wb with lit5 | 1 | 1 | C,DC,N,OV,Z |
| | | CP Wb,Ws | Compare Wb with Ws (Wb - Ws) | 1 | 1 | C,DC,N,OV,Z |
| 19 | CP0 | CP0 f | Compare f with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| | | CP0 Ws | Compare Ws with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| 20 | CPB | CPB f | Compare f with WREG, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB Wb,#lit5 | Compare Wb with lit5, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB Wb,Ws | Compare Wb with Ws, with Borrow (Wb - Ws - $\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 21 | CPSEQ | CPSEQ Wb, Wn | Compare Wb with Wn, skip if = | 1 | 1 (2 or 3) | None |
| 22 | CPSGT | CPSGT Wb, Wn | Compare Wb with Wn, skip if > | 1 | 1 (2 or 3) | None |
| 23 | CPSLT | CPSLT Wb, Wn | Compare Wb with Wn, skip if < | 1 | 1 (2 or 3) | None |
| 24 | CPSNE | CPSNE Wb, Wn | Compare Wb with Wn, skip if ≠ | 1 | 1 (2 or 3) | None |
| 25 | DAW | DAW Wn | Wn = decimal adjust Wn | 1 | 1 | C |
| 26 | DEC | DEC f | f = f -1 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC f,WREG | WREG = f -1 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC Ws,Wd | Wd = Ws - 1 | 1 | 1 | C,DC,N,OV,Z |
| 27 | DEC2 | DEC2 f | f = f -2 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 f,WREG | WREG = f -2 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 Ws,Wd | Wd = Ws - 2 | 1 | 1 | C,DC,N,OV,Z |
| 28 | DISI | DISI #lit14 | Disable Interrupts for k instruction cycles | 1 | 1 | None |

**TABLE 18-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|
| 48 | MPY | MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd | Multiply Wm by Wn to Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd | Square Wm to Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 49 | MPY.N | MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd | -(Multiply Wm by Wn) to Accumulator | 1 | 1 | None |
| 50 | MSC | MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd, AWB | Multiply and Subtract from Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 51 | MUL | MUL.SS Wb,Ws,Wnd | {Wnd+1, Wnd} = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,Ws,Wnd | {Wnd+1, Wnd} = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.US Wb,Ws,Wnd | {Wnd+1, Wnd} = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.UU Wb,Ws,Wnd | {Wnd+1, Wnd} = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Wnd | {Wnd+1, Wnd} = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Wnd | {Wnd+1, Wnd} = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL f | W3:W2 = f * WREG | 1 | 1 | None |
| 52 | NEG | NEG Acc | Negate Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | NEG f | f = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG f,WREG | WREG = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG Ws,Wd | Wd = $\overline{Ws}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| 53 | NOP | NOP | No Operation | 1 | 1 | None |
| | | NOPR | No Operation | 1 | 1 | None |
| 54 | POP | POP f | Pop f from top-of-stack (TOS) | 1 | 1 | None |
| | | POP Wdo | Pop from top-of-stack (TOS) to Wdo | 1 | 1 | None |
| | | POP.D Wnd | Pop from top-of-stack (TOS) to W(nd):W(nd+1) | 1 | 2 | None |
| | | POP.S | Pop Shadow Registers | 1 | 1 | All |
| 55 | PUSH | PUSH f | Push f to top-of-stack (TOS) | 1 | 1 | None |
| | | PUSH Wso | Push Wso to top-of-stack (TOS) | 1 | 1 | None |
| | | PUSH.D Wns | Push W(ns):W(ns+1) to top-of-stack (TOS) | 1 | 2 | None |
| | | PUSH.S | Push Shadow Registers | 1 | 1 | None |
| 56 | PWRSAV | PWRSAV #lit1 | Go into Sleep or Idle mode | 1 | 1 | WDTO,Sleep |
| 57 | RCALL | RCALL Expr | Relative Call | 1 | 2 | None |
| | | RCALL Wn | Computed Call | 1 | 2 | None |
| 58 | REPEAT | REPEAT #lit14 | Repeat Next Instruction lit14+1 times | 1 | 1 | None |
| | | REPEAT Wn | Repeat Next Instruction (Wn)+1 times | 1 | 1 | None |
| 59 | RESET | RESET | Software device Reset | 1 | 1 | None |
| 60 | RETFIE | RETFIE | Return from interrupt | 1 | 3 (2) | None |
| 61 | RETLW | RETLW #lit10,Wn | Return with literal in Wn | 1 | 3 (2) | None |
| 62 | RETURN | RETURN | Return from Subroutine | 1 | 3 (2) | None |
| 63 | RLC | RLC f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 64 | RLNC | RLNC f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 65 | RRC | RRC f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |

**FIGURE 20-2: BROWN-OUT RESET CHARACTERISTICS**

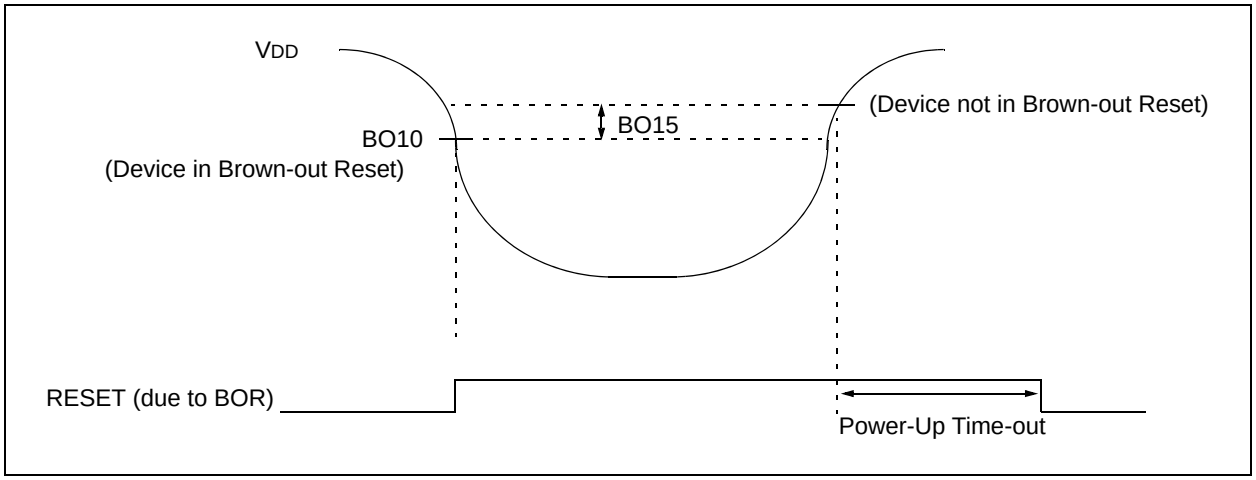



**TABLE 20-11: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Voltage(2) on VDD transition high to low | BORV = 11(3) | — | — | — | V | Not in operating range |
| | | | BORV = 10 | 2.6 | — | 2.71 | V | |
| | | | BORV = 01 | 4.1 | — | 4.4 | V | |
| | | | BORV = 00 | 4.58 | — | 4.73 | V | |
| BO15 | VBHYS | | | — | 5 | — | mV | |

**Note 1:** Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** These parameters are characterized but not tested in manufacturing.

**3:** 11 values not in usable operating range.

**TABLE 20-24: TYPE B TIMER (TIMER2 AND TIMER4) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TB10 | TtxH | TxCK High Time | Synchronous, no prescaler | 0.5 TCY + 20 | — | — | ns | Must also meet parameter TB15 |
| | | | Synchronous, with prescaler | 10 | — | — | ns | |
| TB11 | TtxL | TxCK Low Time | Synchronous, no prescaler | 0.5 TCY + 20 | — | — | ns | Must also meet parameter TB15 |
| | | | Synchronous, with prescaler | 10 | — | — | ns | |
| TB15 | TtxP | TxCK Input Period | Synchronous, no prescaler | TCY + 10 | — | — | ns | N = prescale value (1, 8, 64, 256) |
| | | | Synchronous, with prescaler | Greater of: 20 ns or (TCY + 40)/N | | | | |
| TB20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.5 TCY | — | 1.5 TCY | — | |

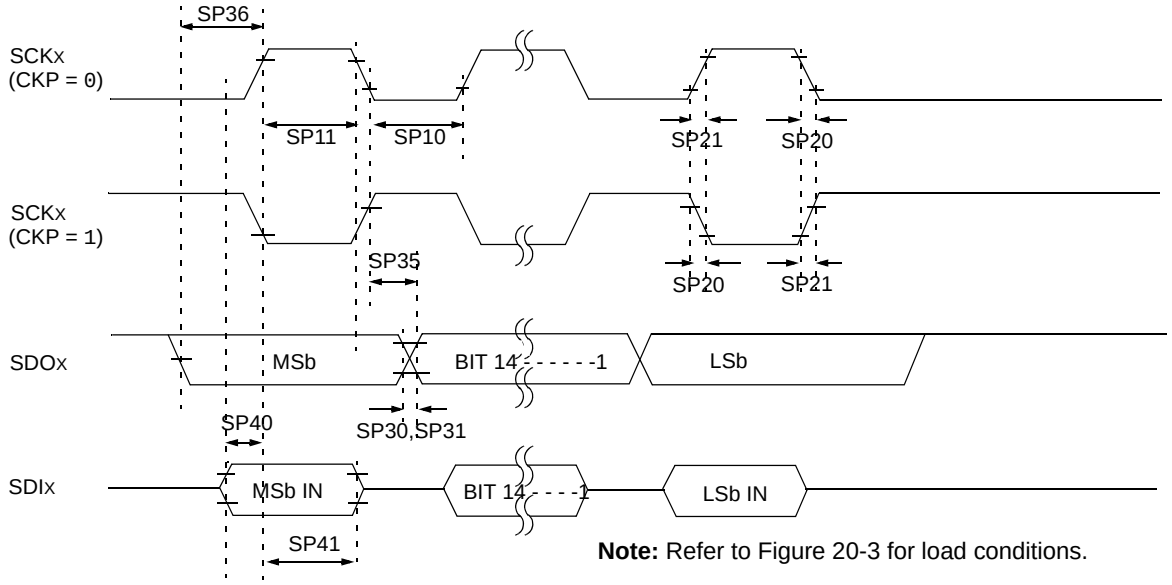
**Note:** Timer2 and Timer4 are Type B.

**TABLE 20-25: TYPE C TIMER (TIMER3 AND TIMER5) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| TC10 | TtxH | TxCK High Time | Synchronous | 0.5 TCY + 20 | — | — | ns | Must also meet parameter TC15 |
| TC11 | TtxL | TxCK Low Time | Synchronous | 0.5 TCY + 20 | — | — | ns | Must also meet parameter TC15 |
| TC15 | TtxP | TxCK Input Period | Synchronous, no prescaler | TCY + 10 | — | — | ns | N = prescale value (1, 8, 64, 256) |
| | | | Synchronous, with prescaler | Greater of: 20 ns or (TCY + 40)/N | | | | |
| TC20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.5 TCY | — | 1.5 TCY | — | |

**Note:** Timer3 and Timer5 are Type C.

**FIGURE 20-13: SPI MODULE MASTER MODE (CKE =1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 20-3 for load conditions.

**TABLE 20-30: SPI MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min** | **Typ(2)** | **Max** | **Units** | **Conditions** |
| SP10 | TscL | SCKx output low time(3) | TCY/2 | — | — | ns | — |
| SP11 | TscH | SCKx output high time(3) | TCY/2 | — | — | ns | — |
| SP20 | TscF | SCKx output fall time(4) | — | — | — | ns | See parameter DO32 |
| SP21 | TscR | SCKx output rise time(4) | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx data output fall time(4) | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx data output rise time(4) | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx data output valid after SCKx edge | — | — | 30 | ns | — |
| SP36 | TdoV2sc, TdoV2scL | SDOx data output setup to first SCKx edge | 30 | — | — | ns | — |
| SP40 | TdiV2scH, TdiV2scL | Setup time of SDIx data input to SCKx edge | 20 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold time of SDIx data input to SCKx edge | 20 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ” column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCK is 100 ns. Therefore, the clock generated in master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI pins.

**FIGURE 20-18: I²C™ BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

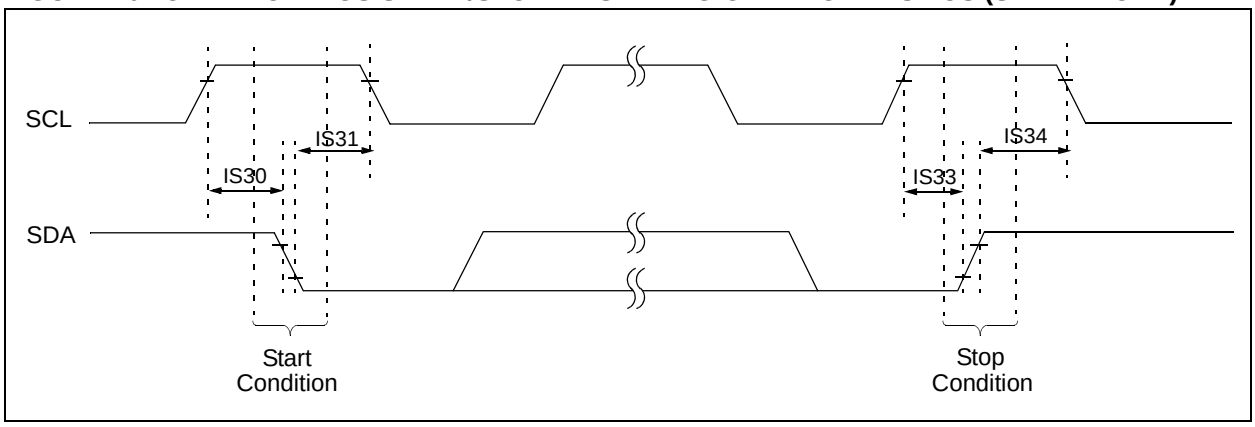



**FIGURE 20-19: I²C™ BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

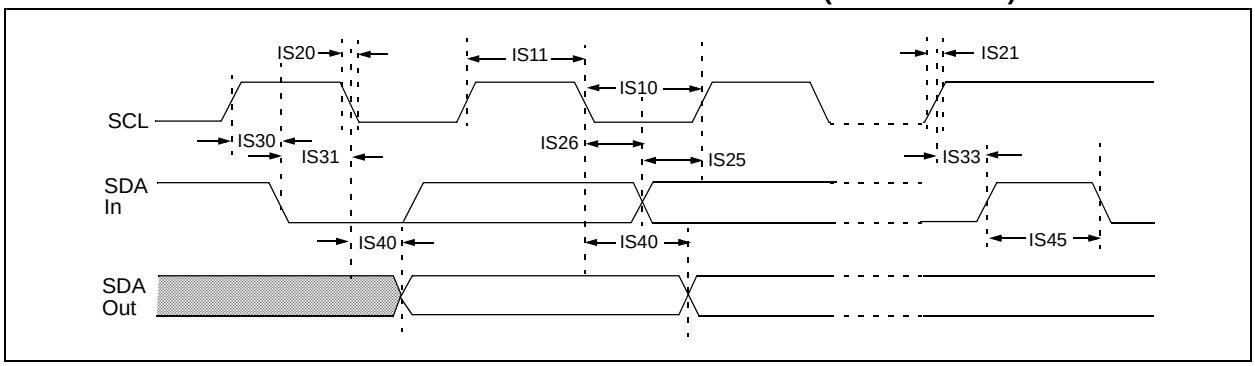



**TABLE 20-34: I²C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)**<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | | **Min** | **Max** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 1.3 | — | µs | Device must operate at a minimum of 10 MHz. |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Device must operate at a minimum of 10 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS20 | TF:SCL | SDA and SCL Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 100 | ns | |
| IS21 | TR:SCL | SDA and SCL Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 300 | ns | |

**Note 1:** Maximum pin capacitance = 10 pF for all I²C™ pins (for 1 MHz mode only).

**TABLE 20-36: 12-BIT ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD | Module VDD Supply | Greater of VDD - 0.3 or 2.7 | — | Lesser of VDD + 0.3 or 5.5 | V | |
| AD02 | AVSS | Module VSS Supply | VSS - 0.3 | — | VSS + 0.3 | V | |
| **Reference Inputs** | | | | | | | |
| AD05 | VREFH | Reference Voltage High | AVSS + 2.7 | — | AVDD | V | |
| AD06 | VREFL | Reference Voltage Low | AVSS | — | AVDD - 2.7 | V | |
| AD07 | VREF | Absolute Reference Voltage | AVSS - 0.3 | — | AVDD + 0.3 | V | |
| AD08 | IREF | Current Drain | — | 200<br>.001 | 300<br>2 | µA<br>µA | A/D operating<br>A/D off |
| **Analog Input** | | | | | | | |
| AD10 | VINH-VINL | Full-Scale Input Span | VREFL | — | VREFH | V | **See Note 1** |
| AD11 | VIN | Absolute Input Voltage | AVSS - 0.3 | — | AVDD + 0.3 | V | — |
| AD12 | — | Leakage Current | — | ±0.001 | ±0.610 | µA | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V Source Impedance = 2.5 kΩ |
| AD13 | — | Leakage Current | — | ±0.001 | ±0.610 | µA | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V Source Impedance = 2.5 kΩ |
| AD15 | RSS | Switch Resistance | — | 3.2K | — | Ω | |
| AD16 | CSAMPLE | Sample Capacitor | — | 18 | | pF | |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | — | — | 2.5K | Ω | |
| **DC Accuracy(2)** | | | | | | | |
| AD20 | Nr | Resolution | 12 data bits | | | bits | |
| AD21 | INL | Integral Nonlinearity | — | — | <±1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V |
| AD21A | INL | Integral Nonlinearity | — | — | <±1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V |
| AD22 | DNL | Differential Nonlinearity | — | — | <±1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V |
| AD22A | DNL | Differential Nonlinearity | — | — | <±1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V |
| AD23 | GERR | Gain Error | +1.25 | +1.5 | +3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V |
| AD23A | GERR | Gain Error | +1.25 | +1.5 | +3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V |

**Note 1:** The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

**2:** Measurements taken with external VREF+ and VREF- used as the ADC voltage references.

**TABLE 20-36: 12-BIT ADC MODULE SPECIFICATIONS (CONTINUED)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤TA ≤+85°C for Industrial<br>-40°C ≤TA ≤+125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ** | **Max.** | **Units** | **Conditions** |
| AD24 | EOFF | Offset Error | -2 | -1.5 | -1.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5V |
| AD24A | EOFF | Offset Error | -2 | -1.5 | -1.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V |
| AD25 | — | Monotonicity(1) | — | — | — | — | Guaranteed |
| **Dynamic Performance** | | | | | | | |
| AD30 | THD | Total Harmonic Distortion | — | -71 | — | dB | |
| AD31 | SINAD | Signal to Noise and Distortion | — | 68 | — | dB | |
| AD32 | SFDR | Spurious Free Dynamic Range | — | 83 | — | dB | |
| AD33 | FNYQ | Input Signal Bandwidth | — | — | 100 | kHz | |
| AD34 | ENOB | Effective Number of Bits | 10.95 | 11.1 | — | bits | |

**Note 1:** The A/D conversion result never decreases with an increase in the input voltage, and has no missing codes.

**2:** Measurements taken with external VREF+ and VREF- used as the ADC voltage references.

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