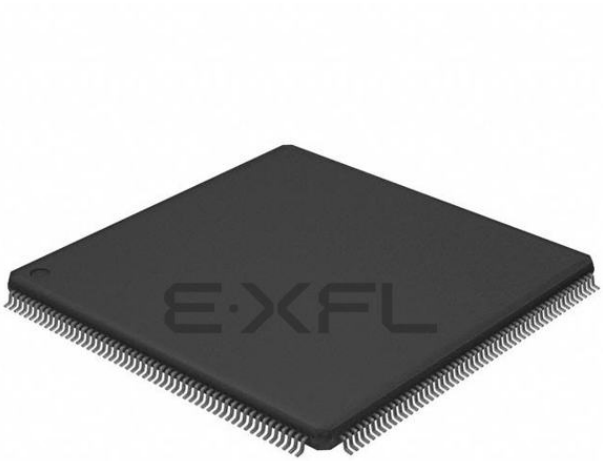

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	142
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	154K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc43s67jbd208e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC43S67JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC43S67JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm	SOT459-1
LPC43S67JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm	SOT926-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	PWM	QEI	ADC channels	Temperature range[1]	GPIO
LPC43S67JET256	1 MB	512 kB	512 kB	154 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC43S67JBD208	1 MB	512 kB	512 kB	154 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC43S67JET100	1 MB	512 kB	512 kB	154 kB	no	yes	yes	yes/no	yes	yes	4	J	49

[1] J = -40 °C to +105 °C

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P1_16	M7	H9	90	[2]	N; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
						I	**U2_RXD —** Receiver input for USART2.
						I/O	**SGPIO3 —** General purpose digital input/output pin.
						I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
						O	**T0_MAT0 —** Match output 0 of timer 0.
						-	**R —** Function reserved.
						I/O	**EMC_D9 —** External memory data line 9.
						I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
P1_17	M8	H10	93	[3]	N; PU	I/O	**GPIO0[12] —** General purpose digital input/output pin.
						I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
						-	**R —** Function reserved.
						I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
						I	**T0_CAP3 —** Capture input 3 of timer 0.
						O	**CAN1_TD —** CAN1 transmitter output.
						I/O	**SGPIO11 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
P1_18	N12	J10	95	[2]	N; PU	I/O	**GPIO0[13] —** General purpose digital input/output pin.
						I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
						-	**R —** Function reserved.
						O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
						O	**T0_MAT3 —** Match output 3 of timer 0.
						I	**CAN1_RD —** CAN1 receiver input.
						I/O	**SGPIO12 —** General purpose digital input/output pin.
						I/O	**EMC_D10 —** External memory data line 10.
P1_19	M11	K9	96	[2]	N; PU	I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
						I/O	**SSP1_SCK —** Serial clock for SSP1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**CLKOUT —** Clock output pin.
						-	**R —** Function reserved.
						O	**I2S0_RX_MCLK —** I2S receive master clock.
						I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P5_4	P9	-	80	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
						O	**MCOB0 —** Motor control PWM channel 0, output B.
						I/O	**EMC_D8 —** External memory data line 8.
						-	**R —** Function reserved.
						I	**U1_CTS —** Clear to Send input for UART 1.
						O	**T1_MAT0 —** Match output 0 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_5	P10	-	81	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
						O	**MCOA1 —** Motor control PWM channel 1, output A.
						I/O	**EMC_D9 —** External memory data line 9.
						-	**R —** Function reserved.
						I	**U1_DCD —** Data Carrier Detect input for UART 1.
						O	**T1_MAT1 —** Match output 1 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_6	T13	-	89	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
						O	**MCOB1 —** Motor control PWM channel 1, output B.
						I/O	**EMC_D10 —** External memory data line 10.
						-	**R —** Function reserved.
						O	**U1_TXD —** Transmitter output for UART 1.
						O	**T1_MAT2 —** Match output 2 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P5_7	R12	-	91	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
						O	**MCOA2 —** Motor control PWM channel 2, output A.
						I/O	**EMC_D11 —** External memory data line 11.
						-	**R —** Function reserved.
						I	**U1_RXD —** Receiver input for UART 1.
						O	**T1_MAT3 —** Match output 3 of timer 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P6_7	J13	-	123	[2]	N; PU	-	**R —** Function reserved.
						I/O	**EMC_A15 —** External memory address line 15.
						I/O	**SGPIO6 —** General purpose digital input/output pin.
						O	**USB0_IND1 —** USB0 port indicator LED control output 1.
						I/O	**GPIO5[15] —** General purpose digital input/output pin.
						O	**T2_MAT0 —** Match output 0 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_8	H13	-	125	[2]	N; PU	-	**R —** Function reserved.
						I/O	**EMC_A14 —** External memory address line 14.
						I/O	**SGPIO7 —** General purpose digital input/output pin.
						O	**USB0_IND0 —** USB0 port indicator LED control output 0.
						I/O	**GPIO5[16] —** General purpose digital input/output pin.
						O	**T2_MAT1 —** Match output 1 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_9	J15	F8	139	[2]	N; PU	I/O	**GPIO3[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**$\overline{\text{EMC\_DYCS0}}$ —** SDRAM chip select 0.
						-	**R —** Function reserved.
						O	**T2_MAT2 —** Match output 2 of timer 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P6_10	H15	-	142	[2]	N; PU	I/O	**GPIO3[6] —** General purpose digital input/output pin.
						O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
						-	**R —** Function reserved.
						O	**EMC_DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PC_6	H6	-	22	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
						-	**R —** Function reserved.
						I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
						I/O	**GPIO6[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						I	**T3_CAP3 —** Capture input 3 of timer 3.
						I/O	**SD_DAT2 —** SD/MMC data bus line 2.
PC_7	G5	-	-	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
						-	**R —** Function reserved.
						I	**ENET_RXD3 —** Ethernet receive data 3 (MII interface).
						I/O	**GPIO6[6] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT0 —** Match output 0 of timer 3.
						I/O	**SD_DAT3 —** SD/MMC data bus line 3.
PC_8	N4	-	-	[2]	N; PU	-	**R —** Function reserved.
						I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
						-	**R —** Function reserved.
						I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
						I/O	**GPIO6[7] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT1 —** Match output 1 of timer 3.
						I	**SD_CD —** SD/MMC card detect input.
PC_9	K2	-	-	[2]	N; PU	-	**R —** Function reserved.
						I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
						-	**R —** Function reserved.
						I	**ENET_RX_ER —** Ethernet receive error (MII interface).
						I/O	**GPIO6[8] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT2 —** Match output 2 of timer 3.
						O	**SD_POW —** SD/MMC power monitor output.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PC_10	M5	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
						I	**U1_DSR —** Data Set Ready input for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[9] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						O	**T3_MAT3 —** Match output 3 of timer 3.
						I/O	**SD_CMD —** SD/MMC command signal.
PC_11	L5	-	-	[2]	N; PU	-	**R —** Function reserved.
						I	**USB1_ULPI_DIR —** ULPI link DIR signal. Controls the ULPI data line direction.
						I	**U1_DCD —** Data Carrier Detect input for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[10] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SD_DAT4 —** SD/MMC data bus line 4.
PC_12	L6	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[11] —** General purpose digital input/output pin.
						I/O	**SGPIO11 —** General purpose digital input/output pin.
						I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
						I/O	**SD_DAT5 —** SD/MMC data bus line 5.
PC_13	M1	-	-	[2]	N; PU	-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**U1_TXD —** Transmitter output for UART 1.
						-	**R —** Function reserved.
						I/O	**GPIO6[12] —** General purpose digital input/output pin.
						I/O	**SGPIO12 —** General purpose digital input/output pin.
						I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						I/O	**SD_DAT6 —** SD/MMC data bus line 6.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PE_10	E14	-	154	[2]	N; PU	-	**R —** Function reserved.
						I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
						O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						I/O	**EMC_D29 —** External memory data line 29.
						I/O	**GPIO7[10] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_11	D16	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
						O	**U1_TXD —** Transmitter output for UART 1.
						I/O	**EMC_D30 —** External memory data line 30.
						I/O	**GPIO7[11] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_12	D15	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
						I	**U1_RXD —** Receiver input for UART 1.
						I/O	**EMC_D31 —** External memory data line 31.
						I/O	**GPIO7[12] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_13	G14	-	-	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
						I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
						O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
						I/O	**GPIO7[13] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.17.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Events control outputs, interrupts, and DMA requests.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states
  - Match register 0 to 5 support a fractional component for the dither engine

7.17.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.17.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.

7.18.5.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.18.6 High-speed USB Host/Device/OTG interface (USB0)

The USB OTG module allows the LPC43S6x to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.18.6.1 Features

- Contains UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.

- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.7 High-speed USB Host/Device interface with ULPI (USB1)

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.18.7.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.8 LCD controller

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.18.8.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.

- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.18.9 Ethernet

7.18.9.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.19 Digital serial peripherals

7.19.1 UART1

Remark: The LPC43S6x contain one UART with standard transmit and receive data lines.

UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.19.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.

7.20.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.20.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

7.21 Analog peripherals

7.21.1 Analog-to-Digital Converter (ADC0/1)

Remark: The LPC43S6x contain two 10-bit ADCs.

7.21.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0. See Table 5

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.24 Serial Wire Debug/JTAG

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

Remark: Serial Wire Debug is supported for the ARM Cortex-M4 only,

The ARM Cortex-M0 coprocessors support JTAG debug. A standard ARM Cortex-compliant debugger can debug the ARM Cortex-M4 and the ARM Cortex-M0 cores separately or both cores simultaneously.

Remark: In order to debug the ARM Cortex-M0, release the M0 reset by software in the RGU block.

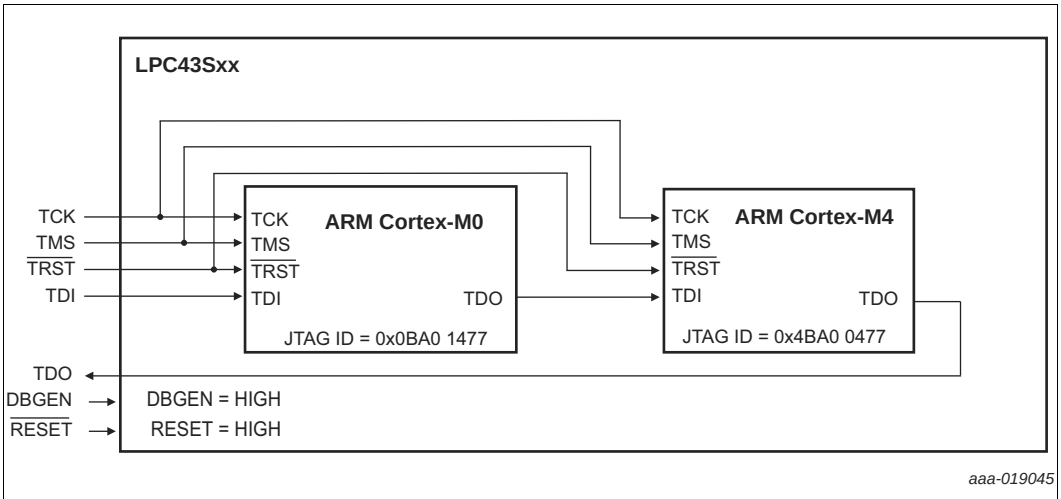
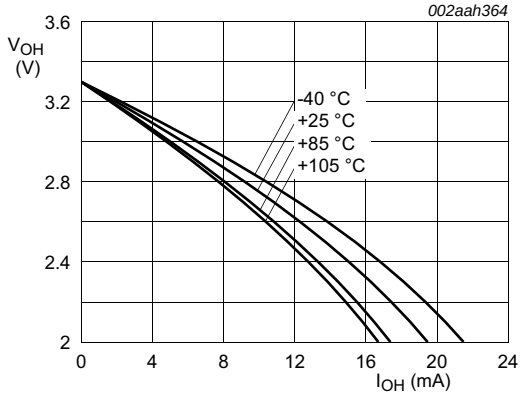
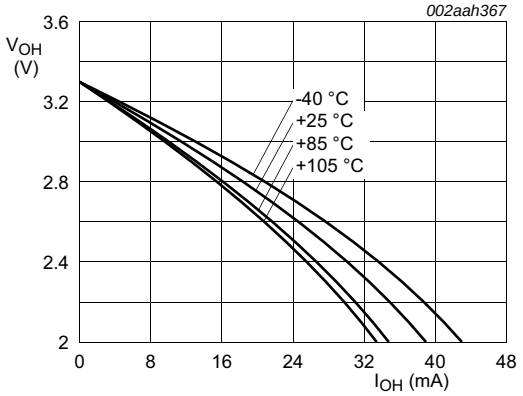


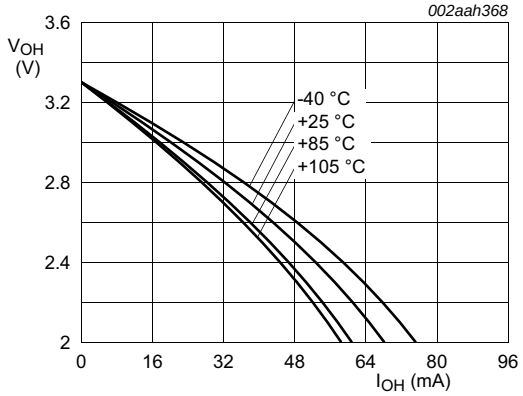
Fig 9. Dual-core debug configuration



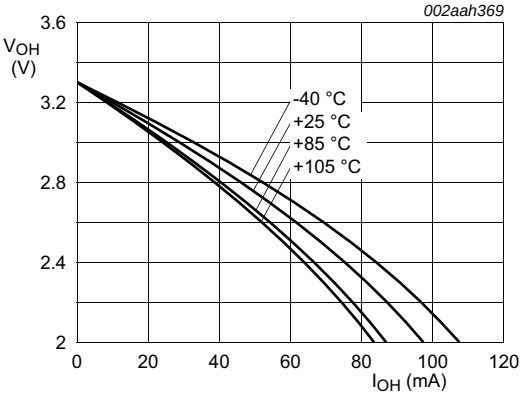
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.

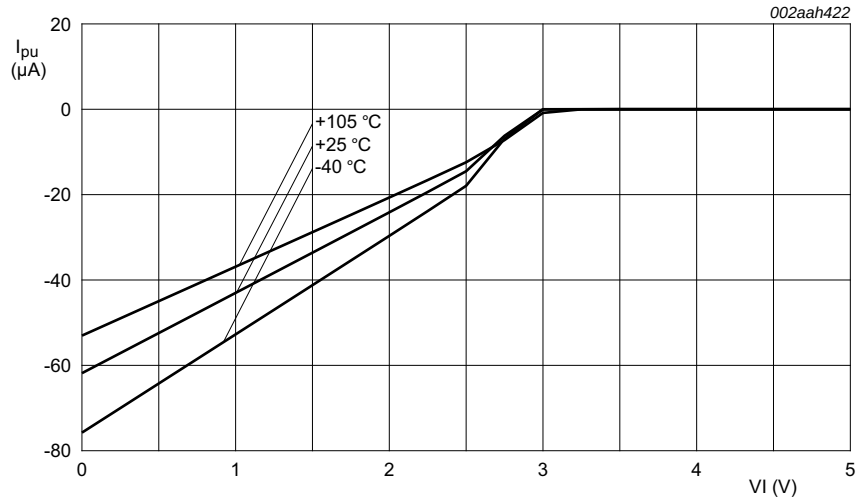


Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.



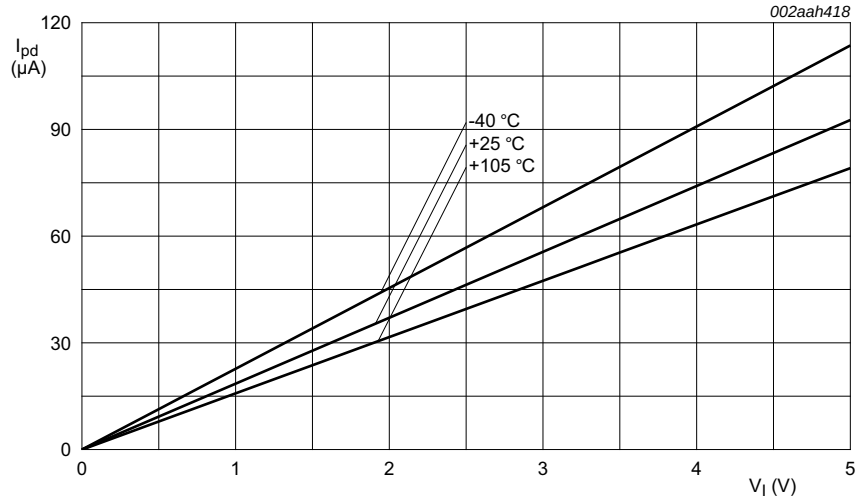
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 22. High-drive pins; typical HIGH level output voltage V_{OH} versus HGH level output current I_{OH}



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

Fig 23. Pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(IO)}$ = 3.3 V. Simulated data over process and temperature.

Fig 24. Pull-down current I_{pd} versus input voltage V_I

11.2 Wake-up times

Table 17. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes

T_{amb} = −40 °C to +105 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from Sleep mode	[2]	$3 \times T_{cy(clk)}$	$5 \times T_{cy(clk)}$	-	ns
		from Deep-sleep and Power-down mode		12	51	-	µs
		from Deep power-down mode		-	200	-	µs
		after reset		-	200	-	µs

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

11.3 External clock for oscillator in slave mode

Remark: The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

Table 18. Dynamic characteristic: external clock

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges.[1]

Symbol	Parameter	Conditions		Min	Max	Unit
f_{osc}	oscillator frequency			1	25	MHz
$T_{cy(clk)}$	clock cycle time			40	1000	ns
t_{CHCX}	clock HIGH time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns
t_{CLCX}	clock LOW time			$T_{cy(clk)} \times 0.4$	$T_{cy(clk)} \times 0.6$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

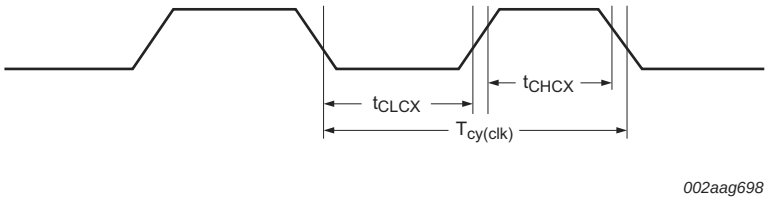


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.12 SSP interface

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		12.2	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.6	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.7	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.7	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		microwire frame format		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

11.13 SPI interface

Table 28. Dynamic characteristics: SPI

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			5			ns
$T_{cy(clk)}$	clock cycle time		[1]	40	-	-	ns
Master							
t_{DS}	data set-up time			7.2	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	3.7	ns
$t_{h(Q)}$	data output hold time			-	-	1.2	ns
Slave							
t_{DS}	data set-up time			1.2	-	-	ns
t_{DH}	data hold time			3 x $T_{cy(PCLK)}$ + 0.54	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	3 x $T_{cy(PCLK)}$ + 9.7	ns
$t_{h(Q)}$	data output hold time			-	-	2 x $T_{cy(PCLK)}$ + 7.1	ns

[1] $T_{cy(clk)}$ = 8/BASE_SPI_CLK. Tcy(PCLK) = 1/BASE_SPI_CLK.

Table 32. Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for EMC_DYCSn, EMC_RAS, EMC_CAS, EMC_WE, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ =3.3 V ± 10 %; RD = 1 (see LPC43xx/LPC43Sxx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	dynamic chip select valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DYCS)}$	dynamic chip select hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	4.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	0.5 + 0.5 × $T_{cy(clk)}$	1.1 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	2.9 + 0.5 × $T_{cy(clk)}$	4.6 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	write enable valid delay time	-	3.2 + 0.5 × $T_{cy(clk)}$	5.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(WE)}$	write enable hold time	1.3 + 0.5 × $T_{cy(clk)}$	1.4 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	DQMOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.0 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	DQMOUT hold time	0.2 + 0.5 × $T_{cy(clk)}$	0.8 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.3 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	CKEOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	CKEOUT hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	2.2	0.8	-	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.2 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns

Table 33. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 105 °C; $V_{DD(IO)}$ =3.3 V ± 10 %; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	delay value	[1]				
		CLKn_DELAY = 0		0.0	0.0	0.0	ns
		CLKn_DELAY = 1	[1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2	[1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3	[1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4	[1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5	[1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6	[1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7	[1]	2.5	3.6	5.8	ns

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC43xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.

13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{RTCX1} and C_{RTCX2} need to be connected externally. Typical capacitance values for C_{RTCX1} and C_{RTCX2} are $C_{RTCX1/2}$ = 20 (typical) $\pm$ 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

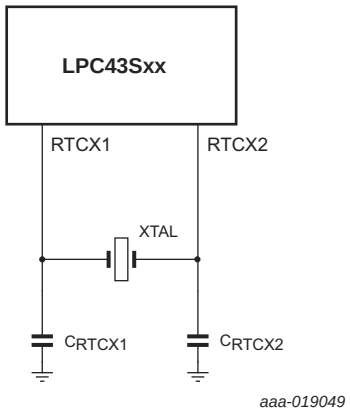


Fig 44. RTC 32 kHz oscillator circuit

13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. Also connect the external components to the ground plain. To keep the noise coupled in via the PCB as small as possible, make loops and parasitics as small as possible. Choose smaller values of C_{X1} and C_{X2} if parasitics increase in the PCB layout.

Ensure that no high-speed or high-drive signals are near the RTCX1/2 signals.

13.5 Standard I/O pin configuration

Figure 45 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input buffer enabled/disabled
- Analog input

The default configuration for standard I/O pins is input buffer disabled and pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.