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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, QEI, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	154K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 16x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc43s67jet100e

- System tick timer.

- Cortex-M0 Processor core
  - ARM Cortex-M0 co-processor (version r0p0) capable of off-loading the main ARM Cortex-M4 application processor.
  - Running at frequencies of up to 204 MHz.
  - JTAG
  - Built-in NVIC.
- Cortex-M0 subsystem
  - ARM Cortex-M0 coprocessor controlling the SPI and SGPIO residing on a separate AHB multilayer matrix. Includes 2 kB + 16 kB of SRAM.
  - Running at frequencies of up to 204 MHz.
  - Connected via a core-to-core bridge to the main AHB multilayer matrix and the main ARM Cortex-M4 processor.
  - JTAG and built-in NVIC.
- On-chip memory
  - Up to 1 MB on-chip dual bank flash memory with flash accelerator.
  - 16 kB on-chip EEPROM data memory.
  - 154 kB SRAM for code and data use.
  - Multiple SRAM blocks with separate bus access. Two SRAM blocks can be powered down individually.
  - 64-bit of One-Time Programmable (OTP) memory for general-purpose use.
  - Two banks (256-bit total) of One-Time Programmable (OTP) memory for AES key storage. One bank can store an encrypted key for decoding the boot image.
- AES engine for encryption and decryption of the boot image and data with DMA support and programmable via a ROM-based API.
- Configurable digital peripherals
  - Serial GPIO (SGPIO) interface.
  - SCTimer/PWM subsystem on AHB.
  - Global Input Multiplexer Array (GIMA) allows to cross-connect multiple inputs and outputs to event driven peripherals like the timers, SCTimer/PWM, and ADC0/1.
- Serial interfaces
  - Quad SPI Flash Interface (SPIFI) with four lanes and up to 52 MB per second.
  - 10/100T Ethernet MAC with RMII and MII interfaces and DMA support for high throughput at low CPU load. Support for IEEE 1588 time stamping/advanced time stamping (IEEE 1588-2008 v2).
  - One High-speed USB 2.0 Host/Device/OTG interface with DMA support and on-chip high-speed PHY.
  - One High-speed USB 2.0 Host/Device interface with DMA support, on-chip full-speed PHY and ULPI interface to external high-speed PHY.
  - USB interface electrical test software included in ROM USB stack.
  - One 550 UART with DMA support and full modem interface.
  - Three 550 USARTs with DMA and synchronous mode support and a smart card interface conforming to ISO7816 specification. One USART with IrDA interface.
  - Up to two C_CAN 2.0B controllers with one channel each.
  - Two SSP controllers with FIFO and multi-protocol support. Both SSPs with DMA support.

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Table 3. Pin description

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
Multiplexed digital pins							
P0_0	L3	G2	47	[2]	N; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
						I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
						I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
						I/O	**SGPIO0 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
						I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P0_1	M2	G1	50	[2]	N; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
						I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
						I	**ENET_COL —** Ethernet Collision detect (MII interface).
						I/O	**SGPIO1 —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
							ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
						I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P1_0	P2	H1	54	[2]	N; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
						I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
						I/O	**EMC_A5 —** External memory address line 5.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SSP0_SSEL —** Slave Select for SSP0.
						I/O	**SGPIO7 —** General purpose digital input/output pin.
						I/O	**EMC_D12 —** External memory data line 12.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P2_9	H16	B10	144	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. Boot pin (see Table 5).
						O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
						I/O	**U3_BAUD —** Baud pin for USART3.
						I/O	**EMC_A0 —** External memory address line 0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P2_10	G16	E8	146	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
						O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
						O	**U2_TXD —** Transmitter output for USART2.
						I/O	**EMC_A1 —** External memory address line 1.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P2_11	F16	A9	148	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
						O	**CTOUT_5 —** SCT output 5. Match output 3 of timer 3.
						I	**U2_RXD —** Receiver input for USART2.
						I/O	**EMC_A2 —** External memory address line 2.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P2_12	E15	B9	153	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
						O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
						-	**R —** Function reserved.
						I/O	**EMC_A3 —** External memory address line 3.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P3_5	C12	B7	173	[2]	N; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
						I	**U1_RXD —** Receiver input for UART 1.
						I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
						I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
						O	**LCD_VD12 —** LCD data.
P3_6	B13	C7	174	[2]	N; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
						I/O	**SPI_MISO —** Master In Slave Out for SPI.
						I/O	**SSP0_SSEL —** Slave Select for SSP0.
						I/O	**SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1.
						-	**R —** Function reserved.
						I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P3_7	C11	D7	176	[2]	N; PU	-	**R —** Function reserved.
						I/O	**SPI_MOSI —** Master Out Slave In for SPI.
						I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
						I/O	**SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0.
						I/O	**GPIO5[10] —** General purpose digital input/output pin.
						I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
P3_8	C10	E7	179	[2]	N; PU	-	**R —** Function reserved.
						I	**SPI_SSEL —** Slave Select for SPI. Note that this pin in an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode.
						I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
						I/O	**SPIFI_CS —** SPIFI serial flash chip select.
						I/O	**GPIO5[11] —** General purpose digital input/output pin.
						I/O	**SSP0_SSEL —** Slave Select for SSP0.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P4_0	D5	-	1	[2]	N; PU	I/O	**GPIO2[0] —** General purpose digital input/output pin.
						O	**MCOA0 —** Motor control PWM channel 0, output A.
						I	**NMI —** External interrupt input to NMI.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**LCD_VD13 —** LCD data.
						I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
						-	**R —** Function reserved.
P4_1	A1	-	3	[5]	N; PU	I/O	**GPIO2[1] —** General purpose digital input/output pin.
						O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
						O	**LCD_VD0 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**LCD_VD19 —** LCD data.
						O	**U3_TXD —** Transmitter output for USART3.
						I	**ENET_COL —** Ethernet Collision detect (MII interface).
						AI	**ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_2	D3	-	12	[2]	N; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
						O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
						O	**LCD_VD3 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**LCD_VD12 —** LCD data.
						I	**U3_RXD —** Receiver input for USART3.
						I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	-	10	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
						O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
						O	**LCD_VD2 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**LCD_VD21 —** LCD data.
						I/O	**U3_BAUD —** Baud pin for USART3.
						I/O	**SGPIO9 —** General purpose digital input/output pin.
						AI	**ADC0_0 —** DAC, ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
P4_4	B1	-	14	[5]	N; PU	I/O	**GPIO2[4] —** General purpose digital input/output pin.
						O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
						O	**LCD_VD1 —** LCD data.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						O	**LCD_VD20 —** LCD data.
						I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
						I/O	**SGPIO10 —** General purpose digital input/output pin.
						O	**DAC —** DAC output. Configure the pin as GPIO input and use the analog function select register in the SCU to select the DAC.
P4_5	D2	-	15	[2]	N; PU	I/O	**GPIO2[5] —** General purpose digital input/output pin.
						O	**CTOUT_5 —** SCT output 5. Match output 3 of timer 3.
						O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO11 —** General purpose digital input/output pin.
P4_6	C1	-	17	[2]	N; PU	I/O	**GPIO2[6] —** General purpose digital input/output pin.
						O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
						O	**LCD_ENAB/LCDM —** STN AC bias drive or TFT data enable input.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						I/O	**SGPIO12 —** General purpose digital input/output pin.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
PE_2	M14	-	115	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
						I	**CAN0_RD —** CAN receiver input.
						-	**R —** Function reserved.
						I/O	**EMC_A20 —** External memory address line 20.
						I/O	**GPIO7[2] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_3	K12	-	118	[2]	N; PU	-	**R —** Function reserved.
						O	**CAN0_TD —** CAN transmitter output.
						I	**ADCTRIG1 —** ADC trigger input 1.
						I/O	**EMC_A21 —** External memory address line 21.
						I/O	**GPIO7[3] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_4	K13	-	120	[2]	N; PU	-	**R —** Function reserved.
						I	**NMI —** External interrupt input to NMI.
						-	**R —** Function reserved.
						I/O	**EMC_A22 —** External memory address line 22.
						I/O	**GPIO7[4] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
PE_5	N16	-	122	[2]	N; PU	-	**R —** Function reserved.
						O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
						O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
						I/O	**EMC_D24 —** External memory data line 24.
						I/O	**GPIO7[5] —** General purpose digital input/output pin.
						-	**R —** Function reserved.
						-	**R —** Function reserved.
						-	**R —** Function reserved.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208		Reset state [1]	Type	Description
XTAL2	E1	C1	19	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins							
USB0_VDDA3V3_DRIVER	F3	D1	24		-	-	Separate analog 3.3 V power supply for driver.
USB0_VDDA3V3	G3	D2	25		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA_TERM	H3	D3	27		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA_REF	G1	F2	31		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	B2	198		-	-	Analog power supply and ADC reference voltage.
VBAT	B10	C5	184		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	E4, E5, F4	135, 188, 195, 82, 33			-	Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VPP	E8	-	-	[12]	-	-	OTP programming voltage.
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	F10, K5	6, 52, 57, 102, 110, 155, 160, 202	[12]	-	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VSS	G9, H7, J10, J11, K8	C8, D4, D5, G8, J3, J6	-	[13]	-	-	Ground.
VSSIO	C4, D13, G6, G7, G8, H8, H9, J8, J9, K9, K10, M13, P7, P13	-	5, 56, 109, 157	[13]	-	-	Ground.
VSSA	B2	C2	196		-	-	Analog ground.

[1] N = neutral, input buffer disabled; no extra VDDIO current consumption if the input is driven midway between supplies; set the EZI bit in the SFS register to enable the input buffer; I = input, OL = output driving LOW; OH = output driving HIGH; AI/O = analog input/output; IA = inactive; PU = pull-up enabled (weak pull-up resistor pulls up pin to VDDIO; F = floating. Reset state reflects the pin state at reset without boot code operation.

[2] 5 V tolerant pad with 15 ns glitch filter (5 V tolerant if VDDIO present; if VDDIO not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength.

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- WWDT, BOD interrupts
- C_CAN0/1 and QEI interrupts
- Ethernet, USB0, USB1 signals
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3)

Remark: Any interrupt can wake up the ARM Cortex-M4 from sleep mode if enabled in the NVIC.

7.9 Global Input Multiplexer Array (GIMA)

The GIMA allows to route signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.

7.9.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.10 On-chip static RAM

The LPC43S6x support up to 154 kB SRAM with separate bus master access for higher throughput and individual power control for low power operation.

7.11 On-chip flash memory

The LPC43S6x contain up to 1 MB of dual-bank flash program memory. With dual-bank flash memory, the user code can write or erase one flash bank while reading the other flash bank without interruption. A two-port flash accelerator maximizes the flash performance.

In-System Programming (ISP) and In-Application Programming (IAP) routines for programming the flash memory are provided in the Boot ROM.

7.12 EEPROM

The LPC43S6x contain 16 kB of on-chip byte-erasable and byte-programmable EEPROM memory.

The EEPROM memory is divided into 128 pages. The user can access pages 1 through 127. Page 128 is protected.

7.13 Boot ROM

The internal ROM memory is used to store the boot code of the LPC43S6x. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.

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- Compliant with SPI specification
- Synchronous, serial, full duplex communication
- Combined SPI master and slave
- Maximum data bit rate of one eighth of the input clock rate
- 8 bits to 16 bits per transfer

7.19.4 SSP serial I/O controller

Remark: The LPC43S6x contain two SSP controllers.

The SSP controller can operate on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bit to 16 bit of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.19.4.1 Features

- Maximum SSP speed in full-duplex mode of 25 Mbit/s; for transmit only 50 Mbit/s (master) and 15 Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

7.19.5 I^2C-bus interface

Remark: The LPC43S6x each contain two I^2C-bus interfaces.

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.19.5.1 Features

- I^2C0 is a standard I^2C compliant bus interface with open-drain pins. I^2C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I^2C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I^2C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.

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7.20.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.20.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.20.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.20.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.20.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

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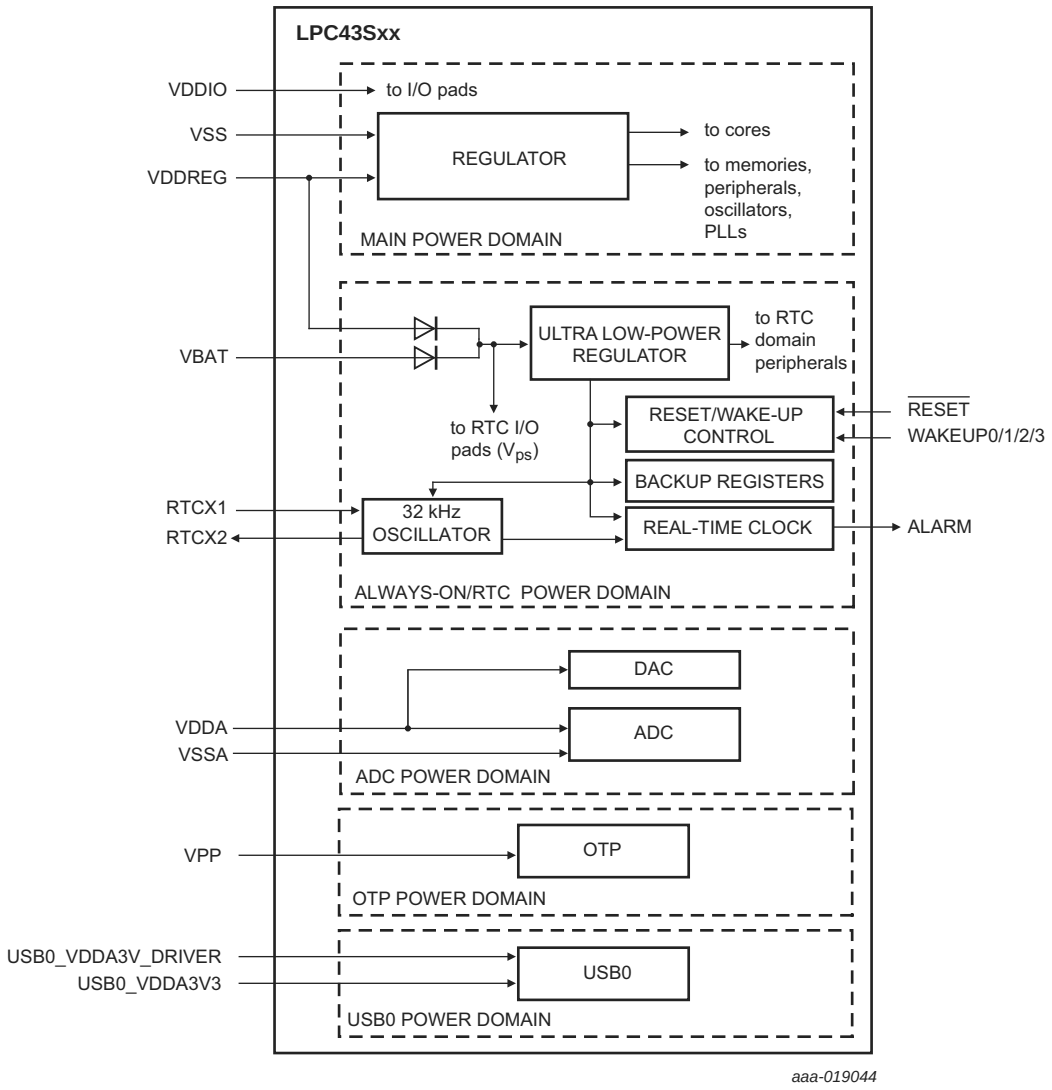

Fig 8. Power domains

7.23.11 Code security (Code Read Protection - CRP)

CRP enables different levels of security so that access to the on-chip flash and use of the JTAG and ISP can be restricted. CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by CRP.

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.

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10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage		[17]	2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; ARM Cortex-M0 core in reset; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
		CCLK = 204 MHz	[4]	-	83	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled; ARM Cortex-M0 core in reset					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-		0.1	nA

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{BAT}	battery supply current	$V_{DD(REG)(3V3)}$ = 3.3 V; V_{BAT} = 3.6 V	[8]				
		deep-sleep mode		-	1.5	-	µA
		power-down mode	[8]	-	1.5	-	µA
		deep power-down mode	[8]	-	1.5	-	µA
I_{BAT}	battery supply current	Deep power-down mode; RTC running; $V_{DD(REG)}$ = VDDA = VDDIO = 0 V; V_{BAT} = 3.3 V		-	3.0	-	µA
		$V_{DD(REG)(3V3)}$ = V_{BAT} = 3.3 V		-	1.5	-	µA
$I_{DD(IO)}$	I/O supply current	deep sleep mode		-	< 0.1	-	µA
		power-down mode		-	< 0.1	-	µA
		deep power-down mode		-	< 0.1	-	µA
I_{DDA}	Analog supply current	on pin VDDA;	[10]	-	0.4	-	
		deep sleep mode					µA
		power-down mode	[10]	-	0.4	-	µA
		deep power-down mode	[10]	-	0.007	-	µA
$\overline{\text{RESET}}$ pin							
V_{IH}	HIGH-level input voltage		[9]	0.8 × (V_{ps} − 0.35)	-	5.5	V
V_{IL}	LOW-level input voltage		[9]	−0.5	-	0.3 × (V_{ps} − 0.1)	V
V_{hys}	hysteresis voltage		[9]	0.05 × (V_{ps} − 0.35)	-	-	V
Standard I/O pins - normal drive strength							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	V_I = $V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.5	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	40	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;		0	-	5.5	V
		$V_{DD(IO)}$ ≥ 2.4 V					
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[13] [14] [15]	-	62	-	µA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq$ 5 V		-	10	-	µA
I/O pins - high drive strength: standard drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	65	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.7	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	70	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	63	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	113	mA

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76	mA
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[13] [14] [15]	-	62	-	µA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq 5$ V		-	0	-	µA
Open-drain I²C0-bus pins							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			−0.5	0.14	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[12]	-	4.5	-	µA
		V_I = 5 V		-	-	10	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	-	1.2	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	-	1.2	V
C_{io}	input/output capacitance		[16]	-	-	0.8	pF
USB0 pins[17]							
V_I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		$V_{DD(IO)} \geq 2.4$ V		0	-	5.25	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
R_{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ
V_{IC}	common-mode input voltage	high-speed mode		−50	200	500	mV
		full-speed/low-speed mode		800	-	2500	mV
		chirp mode		−50	-	600	mV
$V_{i(dif)}$	differential input voltage			100	400	1100	mV
USB1 pins (USB1_DP/USB1_DM)[17]							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[17]	-	-	±10	µA

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11.4 Crystal oscillator

Table 19. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[5]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3][4]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps
High-frequency mode (20 - 25 MHz)[6]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3][4]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] PLL-induced jitter is not included.

[5] Select HF = 0 in the XTAL_OSC_CTRL register.

[6] Select HF = 1 in the XTAL_OSC_CTRL register.

11.5 IRC oscillator

Table 20. Dynamic characteristic: IRC oscillator

2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-40 °C ≤ T_{amb} < 0 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz
		0 °C ≤ T_{amb} ≤ 85 °C	12.0 - 1.5 %	12.0	12.0 + 1.5 %	MHz
		85 °C < T_{amb} < 105 °C	12.0 - 3 %	12.0	12.0 + 3 %	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.6 RTC oscillator

See Section 13.3 for connecting the RTC oscillator to an external clock source.

Table 21. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V or 2.4 V ≤ V_{BAT} ≤ 3.6 V[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz
$I_{CC(osc)}$	oscillator supply current				280	800	nA

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

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11.17 External memory interface

Table 31. Dynamic characteristics: Static asynchronous external memory interface

C_L = 22 pF for EMC_Dn C_L = 20 pF for all others; T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted which results in multiple memory accesses.

Symbol	Parameter[1]	Conditions		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		[2]	−0.6 + $T_{cy(clk)}$ × WAITOEN	-	1.3 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		[2]	−0.6 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time			-	-	−16 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	ns
$t_{h(D)}$	data input hold time			−16	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		−0.4	-	1.9	ns
t_{CSHOEH}	CS HIGH to $\overline{OE}$ HIGH time			−0.4	-	1.4	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid	PB = 1		−2.0	-	2.6	ns
t_{CSHEOR}	$\overline{CS}$ HIGH to end of read time		[3]	−2.0	-	0	ns
t_{CSLSOR}	$\overline{CS}$ LOW to start of read time		[4]	0	-	1.8	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time			−3.1	-	1.6	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time			−3.1	-	1.5	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	PB = 1		−1.5 + (WAITWEN + 1) × $T_{cy(clk)}$	-	0.2 + (WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	PB = 1		−0.7	-	1.8	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	PB = 1	[2]	−0.6 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	−0.4 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	PB = 1	[2]	−0.9 + $T_{cy(clk)}$	-	2.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	PB = 1	[2] [5]	−0.4 + $T_{cy(clk)}$	-	−0.3 + $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	PB = 0		−0.7 + (WAITWEN + 1) × $T_{cy(clk)}$	-	1.8 + (WAITWEN + 1) × $T_{cy(clk)}$	ns

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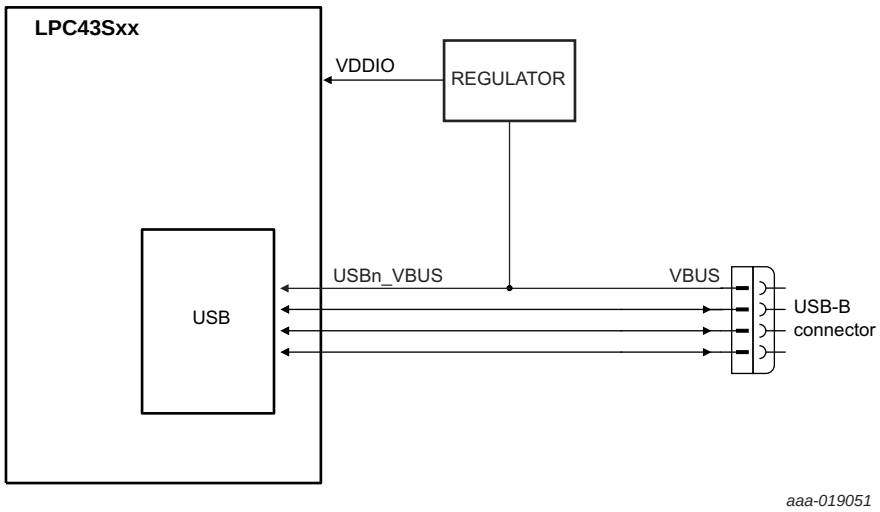

Fig 48. USB interface on a bus-powered device

Remark: If the VBUS function of the USB1 interface is not connected, configure the pin function for GPIO using the function control bits in the SYSCON block.

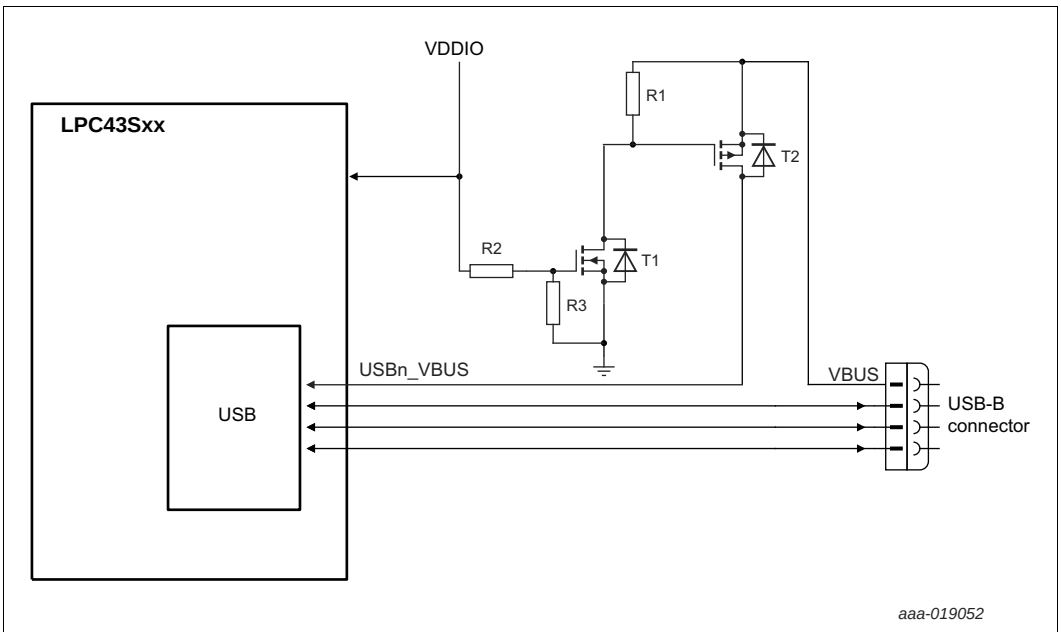

Fig 49. USB interface for USB operating in OTG mode

Remark: In OTG mode, it is important to be able to detect the VBUS level and to charge and discharge VBUS. This requires adding active devices that disconnect the link when VDDIO is not present.

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Table 46. Abbreviations *…continued*

Acronym	Description
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB2.0 Transceiver Macrocell Interface

17. References

[1] LPC43xx/LPC43Sxx User manual UM10503: http://www.nxp.com/documents/user_manual/UM10503.pdf

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