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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Ethernet, I²C, TDM, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	448kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8112tmp2400v

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Table 1. MSC8112 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
H21	V_{DDH}	K15	V_{DD}
H22	A31	K16	TT2/$\overline{CS5}$
J2	HA18	K17	ALE
J3	HA26	K18	$\overline{CS2}$
J4	V_{DD}	K19	GND
J5	HA13	K20	A26
J6	GND	K21	A29
J7	PSDAMUX/PGPL5	K22	A28
J8	BADDR27	L2	HA12
J9	V_{DD}	L3	HA14
J10	CLKIN	L4	HA11
J11	BM2/TC2/BNKSEL2	L5	V_{DDH}
J12	$\overline{DBG}$	L6	V_{DDH}
J13	V_{DD}	L7	BADDR28
J14	GND	L8	$\overline{IRQ5}$/BADDR29
J15	V_{DD}	L9	GND
J16	TT3/$\overline{CS6}$	L10	GND
J17	PSDA10/PGPL0	L14	GND
J18	$\overline{BCTL1}$/$\overline{CS5}$	L15	V_{DDH}
J19	GPIO23/TDM0TDAT/$\overline{IRQ13}$	L16	GND
J20	GND	L17	GND
J21	GPIO25/TDM0RCLK/$\overline{IRQ15}$	L18	$\overline{CS3}$
J22	A30	L19	V_{DDH}
K2	HA15	L20	A27
K3	HA21	L21	A25
K4	HA16	L22	A22
K5	$\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$	M2	HD28
K6	$\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$	M3	HD31
K7	$\overline{POE}$/$\overline{PSDRAS}$/PGPL2	M4	V_{DDH}
K8	$\overline{IRQ2}$/BADDR30	M5	GND
K9	Reserved	M6	GND
K10	GND	M7	GND
K11	GND	M8	V_{DD}
K12	GND	M9	V_{DDH}
K13	GND	M10	GND
K14	CLKOUT	M14	GND

Table 1. MSC8112 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

Table 1. MSC8112 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T6	HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7	U21	A12
T7	HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	TBST	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	IRQ5/DP5/DACK4/EXT_BG3	V10	D10
T17	IRQ4/DP4/DACK3/EXT_DBG3	V11	D12
T18	IRQ1/DP1/DACK1/EXT_BG2	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core and PLL supply voltage:	V_{DD} V_{CCSYN}	1.07 to 1.13	V
I/O supply voltage	V_{DDH}	3.135 to 3.465	V
Input voltage	V_{IN}	–0.2 to V_{DDH}+0.2	V
Operating temperature range:	T_J	–40 to 105	°C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8112 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8112

Characteristic	Symbol	FC-PBGA 20 × 20 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	26	21	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	19	15	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	9		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.9		°C/W
Junction-to-package-top[6]	Ψ_{JT}	1		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.5, *Thermal Considerations* provides a detailed explanation of these characteristics.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8112. The measurements in **Table 5** assume the following system conditions:

- T_A = 25 °C
- V_{DD} = 1.1 V nominal = 1.07–1.13 V_{DC}
- V_{DDH} = 3.3 V ± 5% V_{DC}
- GND = 0 V_{DC}

Note: The leakage current is measured for nominal V_{DDH} and V_{DD}.

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

Table 6. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8112 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

Note: See **Section 3.1** for start-up sequencing recommendations and **Section 3.2** for power supply design recommendations.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 7** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

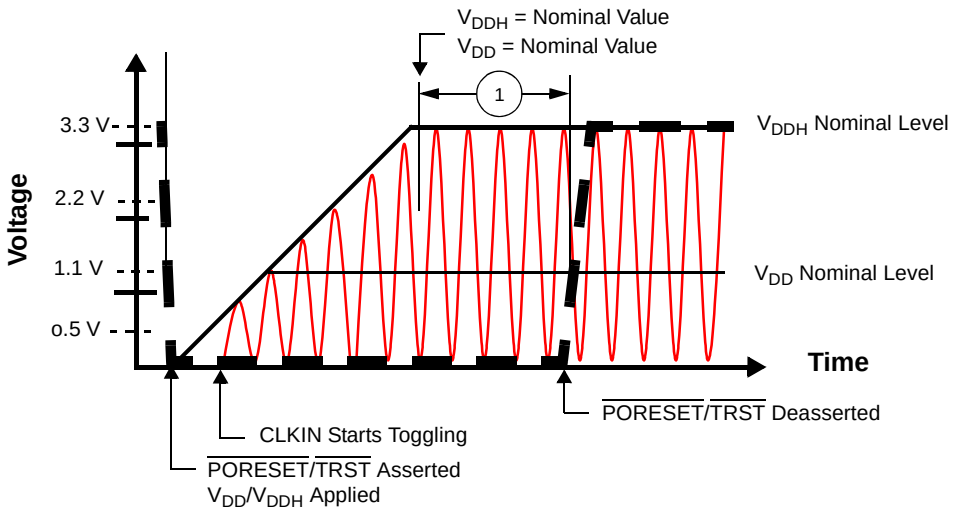


Figure 6. Start-Up Sequence: V_{DD} and V_{DDH} Raised Together

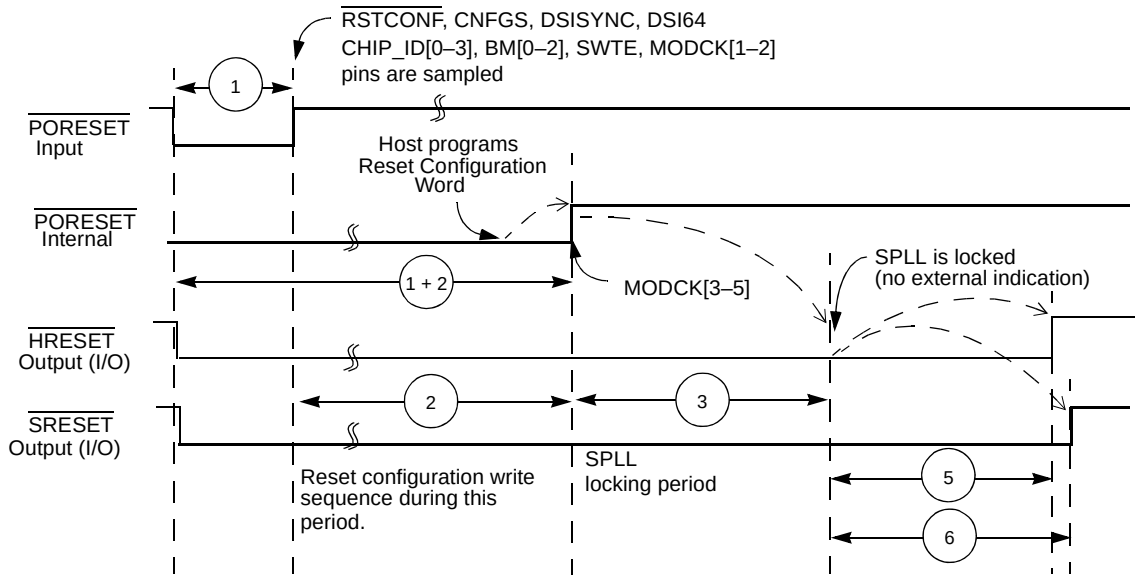


Figure 9. Timing Diagram for a Reset Configuration Write

2.5.5 System Bus Access Timing

2.5.5.1 Core Data Transfers

Generally, all MSC8112 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 13** shows.

Table 13. Tick Spacing for Memory Controller Signals

BCLK/SC140 clock	Tick Spacing (T1 Occurs at the Rising Edge of REFCLK)		
	T2	T3	T4
1:4, 1:6, 1:8, 1:10	1/4 REFCLK	1/2 REFCLK	3/4 REFCLK
1:3	1/6 REFCLK	1/2 REFCLK	4/6 REFCLK
1:5	2/10 REFCLK	1/2 REFCLK	7/10 REFCLK

Figure 10 is a graphical representation of **Table 13**.

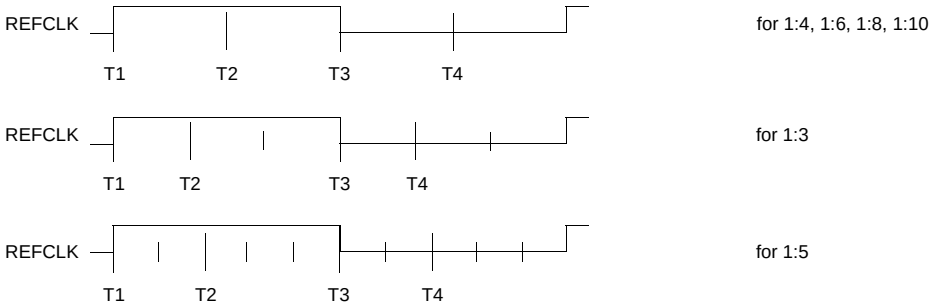


Figure 10. Internal Tick Spacing for Memory Controller Signals

2.5.5.2 CLKIN to CLKOUT Skew

Table 17 describes the CLKOUT-to-CLKIN skew timing.

Table 16. CLKOUT Skew

No.	Characteristic	Min[1]	Max[1]	Units
20	Rise-to-rise skew	0.0	0.95	ns
21	Fall-to-fall skew	–1.5	1.0	ns
24	CLKOUT phase (1.1 V, 100 MHz) • Phase high • Phase low	 3.3 3.3	 — —	 ns ns

Notes:
1. A positive number indicates that CLKOUT precedes CLKIN, A negative number indicates that CLKOUT follows CLKIN.
2. Skews are measured in clock mode 29, with a CLKIN:CLKOUT ratio of 1:1. The same skew is valid for all clock modes.
3. CLKOUT skews are measured using a load of 10 pF.
4. CLKOUT skews and phase are not measured for 500/166 Mhz parts because these parts only use CLKIN mode.

For designs that use the CLKOUT synchronization mode, use the skew values listed in **Table 16** to adjust the rise-to-fall timing values specified for CLKIN synchronization. **Figure 12** shows the relationship between the CLKOUT and CLKIN timings.

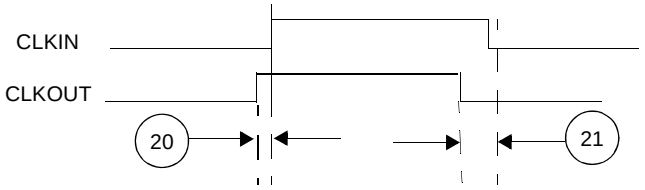


Figure 12. CLKOUT and CLKIN Signals.

2.5.5.3 DMA Data Transfers

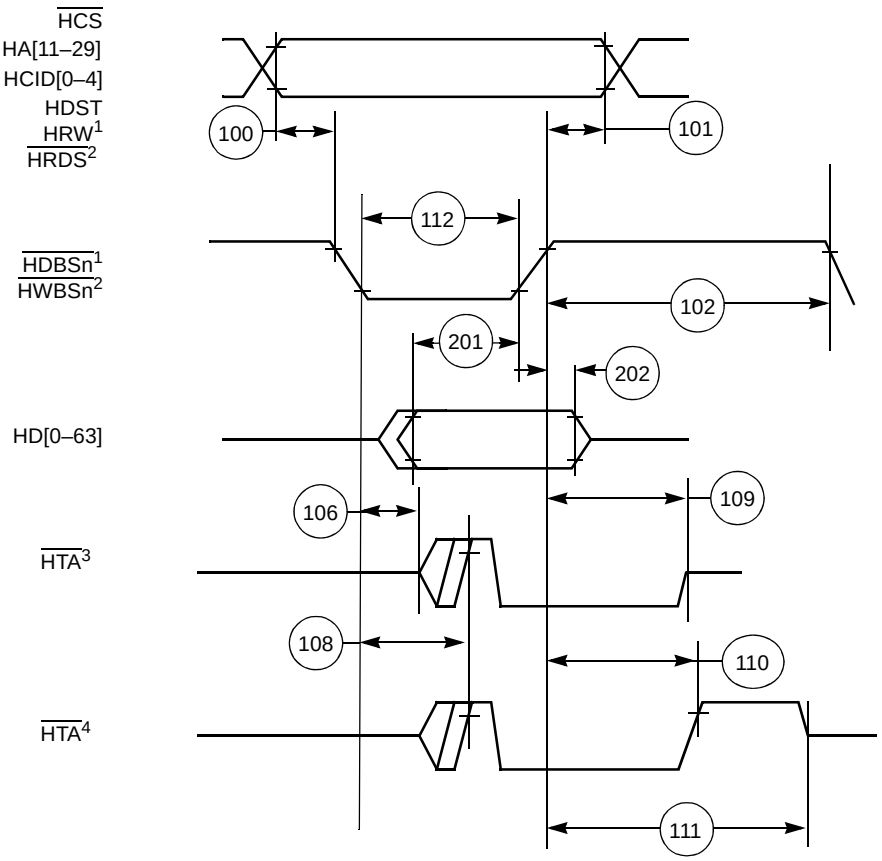
Table 17 describes the DMA signal timing.

Table 17. DMA Signals

No.	Characteristic	Ref = CLKIN		Units
		Min	Max	
37	DREQ set-up time before the 50% level of the falling edge of REFCLK	5.0	—	ns
38	DREQ hold time after the 50% level of the falling edge of REFCLK	0.5	—	ns
39	DONE set-up time before the 50% level of the rising edge of REFCLK	5.0	—	ns
40	DONE hold time after the 50% level of the rising edge of REFCLK	0.5	—	ns
41	DACK/DRACK/DONE delay after the 50% level of the REFCLK rising edge	0.5	7.5	ns

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 17**. **Figure 13** shows synchronous peripheral interaction.

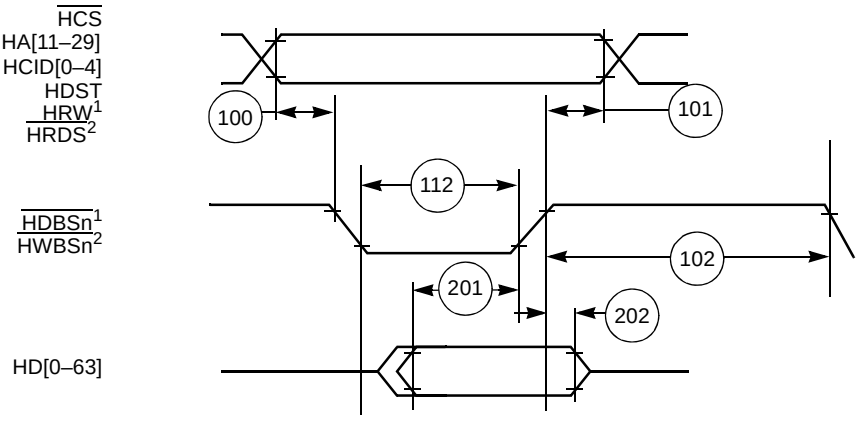
Figure 15 shows DSI asynchronous write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 15. Asynchronous Single- and Dual-Strobe Modes Write Timing Diagram

Figure 16 shows DSI asynchronous broadcast write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 16. Asynchronous Broadcast Write Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs in Synchronous Mode

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
120	HCLKIN cycle time[1,2]	HTC	10.0	55.6	ns
121	HCLKIN high pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
122	HCLKIN low pulse width	(0.5 ± 0.1) × HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.6	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes: 1. Values are based on a frequency range of 18–70 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

Table 20. DSI Outputs in Synchronous Mode

No.	Characteristic	1.1 V Core		Units
		Min	Max	
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	7.6	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	8.3	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.2	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	7.4	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	7.5	ns

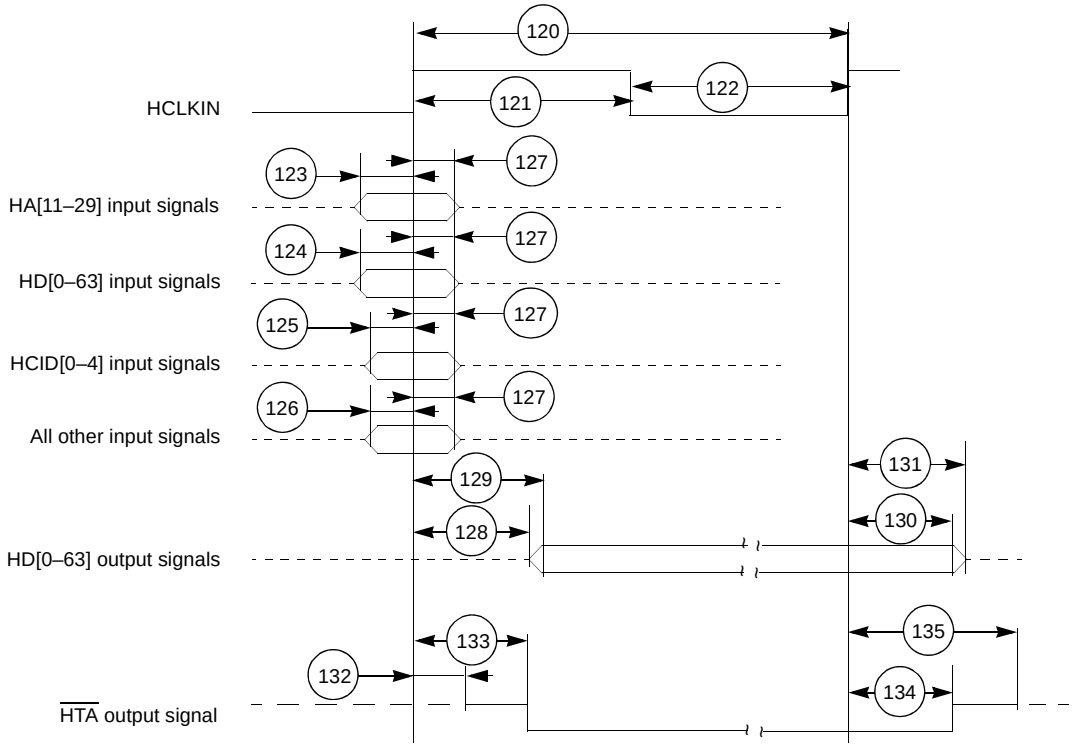


Figure 17. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 21. TDM Timing

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
300	TDMxRCLK/TDMxTCLK	TC[1]	16	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ± 0.1) × TC	7	—	ns
302	TDMxRCLK/TDMxTCLK low pulse width	(0.5 ± 0.1) × TC	7	—	ns
303	TDM receive all input set-up time		1.3	—	ns
304	TDM receive all input hold time		1.0	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		2.8	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output		—	10.0	ns
307	All output hold time[4]		2.5	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	10.7	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	9.7	ns
310	TDMxTSYN output hold time[4]		2.5	—	ns

Notes:
1. Devices operating at 300 MHz are limited to a maximum TDMxRCLK/TDMxTCLK frequency of 50 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8112 Reference Manual* for details.
4. Values are based on 10 pF capacitive load.

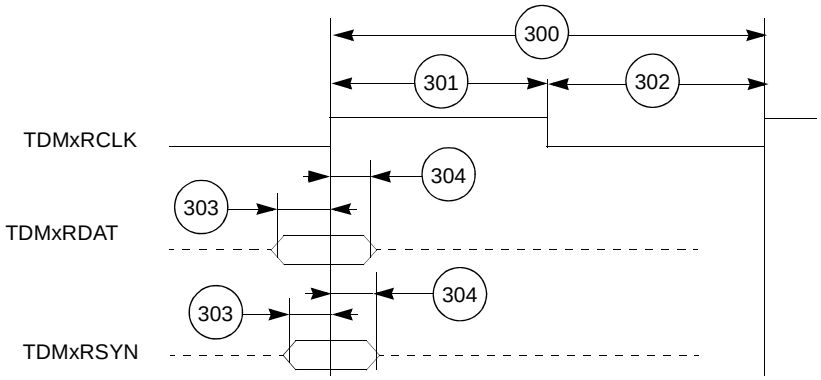


Figure 18. TDM Inputs Signals

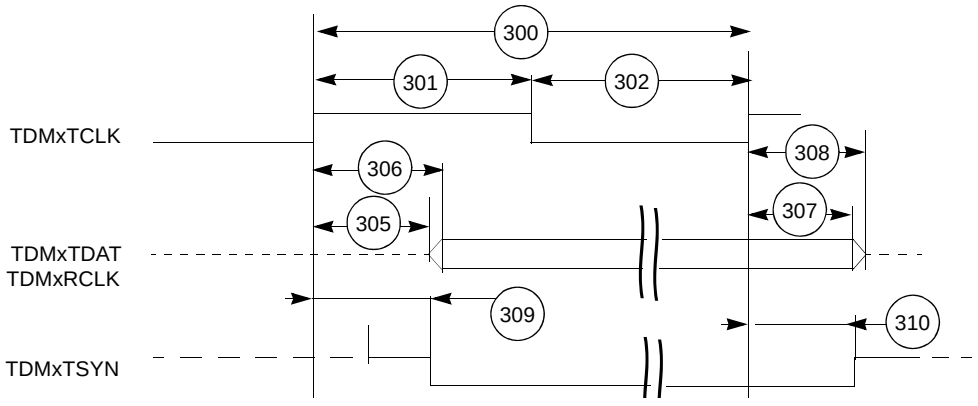


Figure 19. TDM Output Signals

2.5.10 Ethernet Timing

2.5.10.1 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

No.	Characteristics	Min	Max	Unit
801	ETHMDIO to ETHMDC rising edge set-up time	10	—	ns
802	ETHMDC rising edge to ETHMDIO hold time	10	—	ns

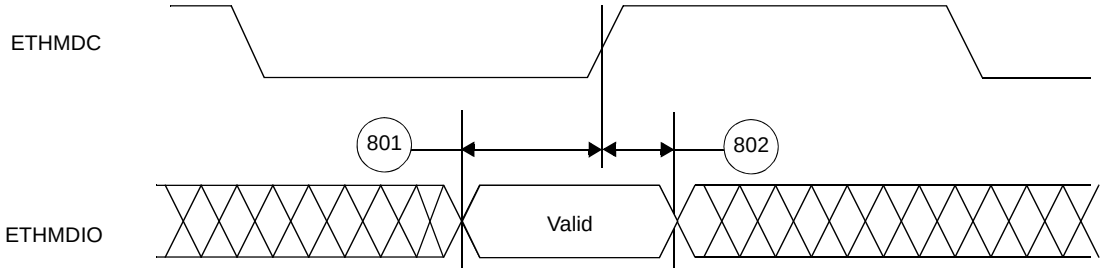


Figure 23. MDIO Timing Relationship to MDC

2.5.10.2 MII Mode Timing

Table 25. MII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
803	ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time	3.5	—	ns
804	ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time	3.5	—	ns
805	ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay	1	14.6	ns

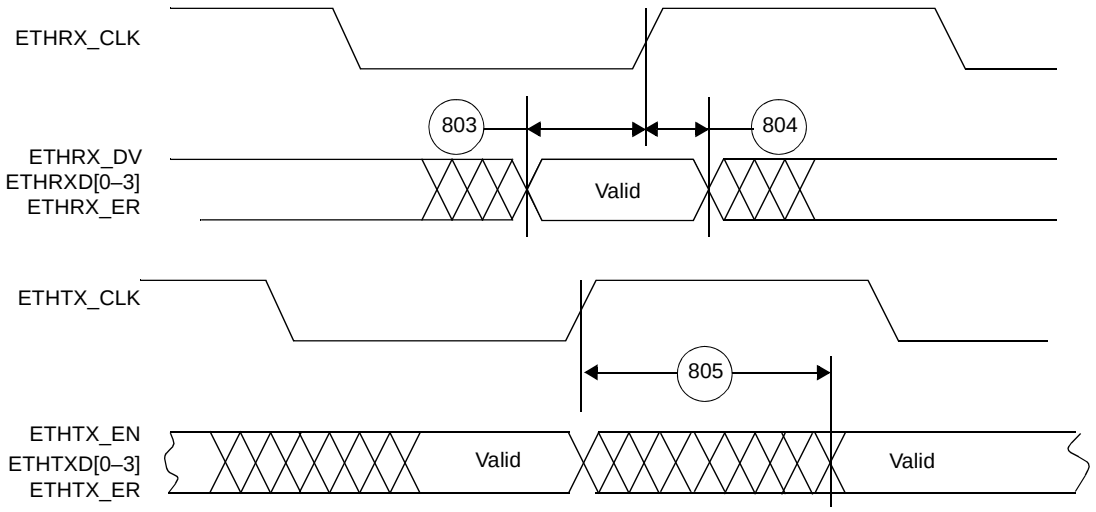


Figure 24. MII Mode Signal Timing

2.5.10.3 RMII Mode

Table 26. RMII Mode Signal Timing

No.	Characteristics	1.1 V Core		Unit
		Min	Max	
806	ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time	1.6	—	ns
807	ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time	1.6	—	ns
811	ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay.	3	12.5	ns

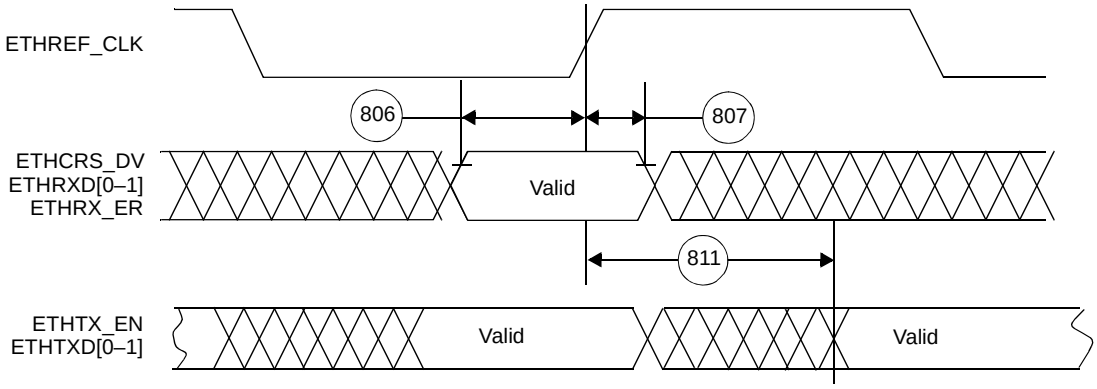


Figure 25. RMII Mode Signal Timing

2.5.10.4 SMII Mode

Table 27. SMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	—	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	1.5[1]	6.0[2]	ns

Notes: **1.** Measured using a 5 pF load.
2. Measured using a 15 pF load.

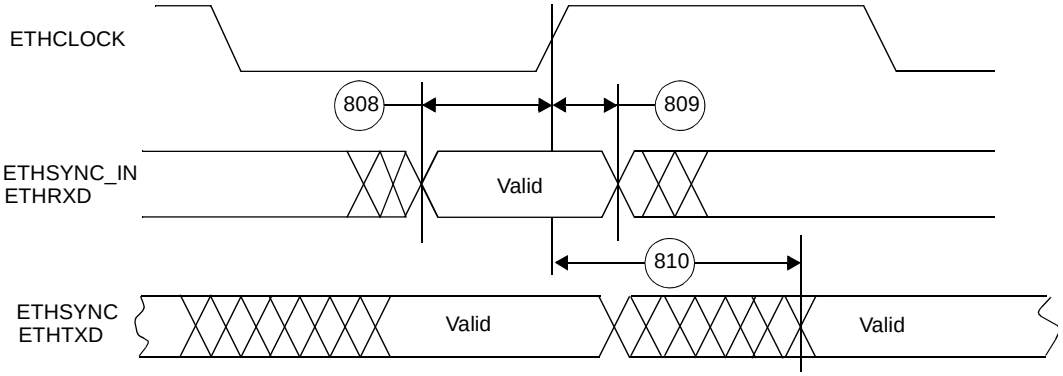


Figure 26. SMII Mode Signal Timing

2.5.13 JTAG Signals

Table 30. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 4$); maximum 25 MHz)	0.0	25	MHz
701	TCK cycle time	40.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V • High • Low	 20.0 16.0	 — —	 ns ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	20.0	—	ns
706	TCK low to output data valid	0.0	30.0	ns
707	TCK low to output high impedance	0.0	30.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	20.0	—	ns
710	TCK low to TDO data valid	0.0	20.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
713	$\overline{\text{TRST}}$ set-up time to TCK low	30.0	—	ns
Note:	All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.			

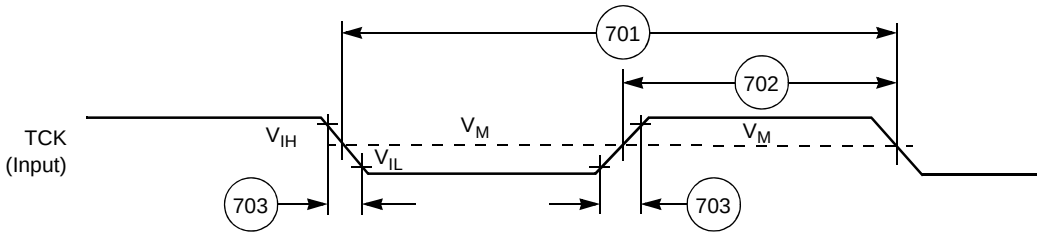


Figure 29. Test Clock Input Timing Diagram

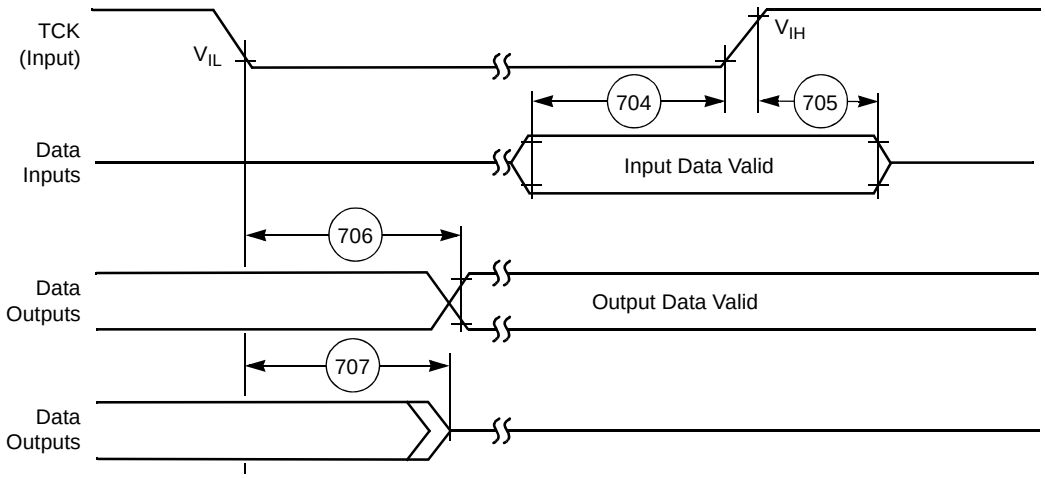


Figure 30. Boundary Scan (JTAG) Timing Diagram

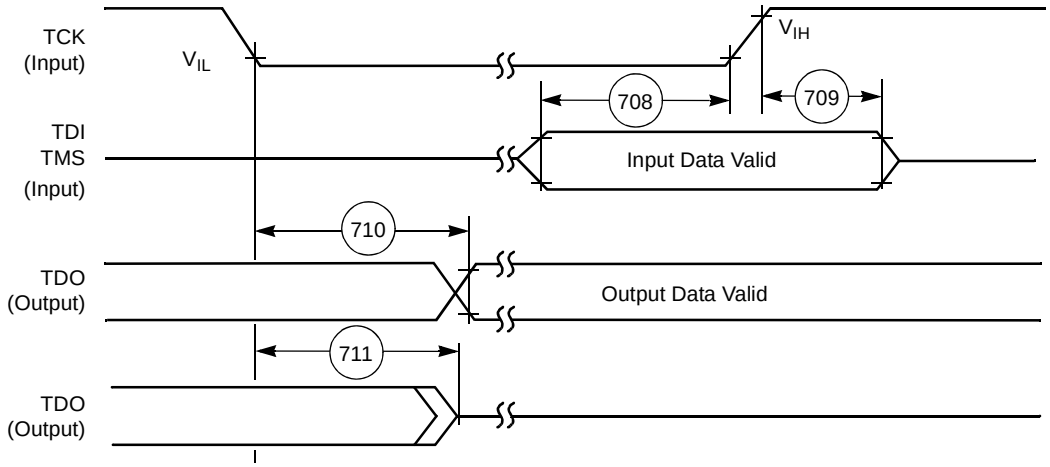


Figure 31. Test Access Port Timing Diagram

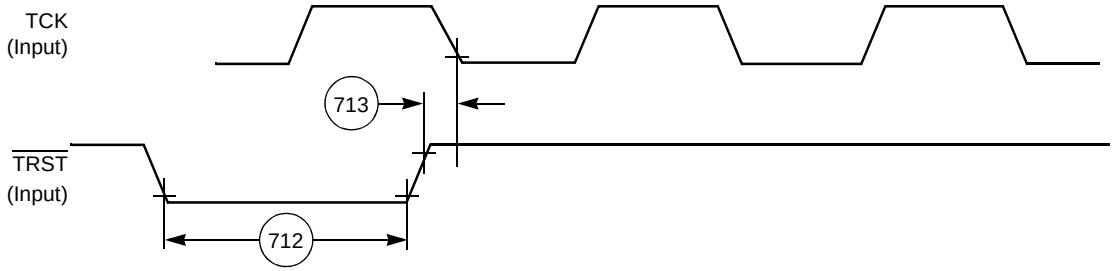


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8112 device is designed into a system.

3.1 Start-up Sequencing Recommendations

Use the following guidelines for start-up and power-down sequences:

- Assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ before applying power and keep the signals driven low until the power reaches the required minimum power levels. This can be implemented via weak pull-down resistors.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{\text{PORESET}}$ and after both power supplies have reached nominal voltage levels.
- If possible, bring up V_{DD}/V_{CCSYN} and V_{DDH} together. If it is not possible, raise V_{DD}/V_{CCSYN} first and then bring up V_{DDH}. V_{DDH} should not exceed V_{DD}/V_{CCSYN} until V_{DD}/V_{CCSYN} reaches its nominal voltage level. Similarly, bring both voltage levels down together. If that is not possible reverse the power-up sequence, with V_{DDH} going down first and then V_{DD}/V_{CCSYN}.

Note: This recommended power sequencing for the MSC8112 is different from the MSC8102. See **Section 2.5.2** for start-up timing specifications.

External voltage applied to any input line must not exceed the I/O supply V_{DDH} by more than 0.8 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule. However, each such input can draw up to 80 mA per input pin per device in the system during start-up.

During the power-up sequence, if V_{DD} rises before V_{DDH} (see **Figure 6**), current can pass from the V_{DD} supply through the device ESD protection circuits to the V_{DDH} supply. The ESD protection diode can allow this to occur when V_{DD} exceeds V_{DDH} by more than 0.8 V. Design the power supply to prevent or minimize this effect using one of the following optional methods:

- Never allow V_{DD} to exceed V_{DDH} + 0.8V.
- Design the V_{DDH} supply to prevent reverse current flow by adding a minimum 10 Ω resistor to GND to limit the current. Such a design yields an initial V_{DDH} level of V_{DD} – 0.8 V before it is enabled.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

3.2 Power Supply Design Considerations

When implementing a new design, use the guidelines described in the *MSC8112 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information. See **Section 2.5.2** for start-up timing specifications.

Figure 33 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.1 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8112 device.

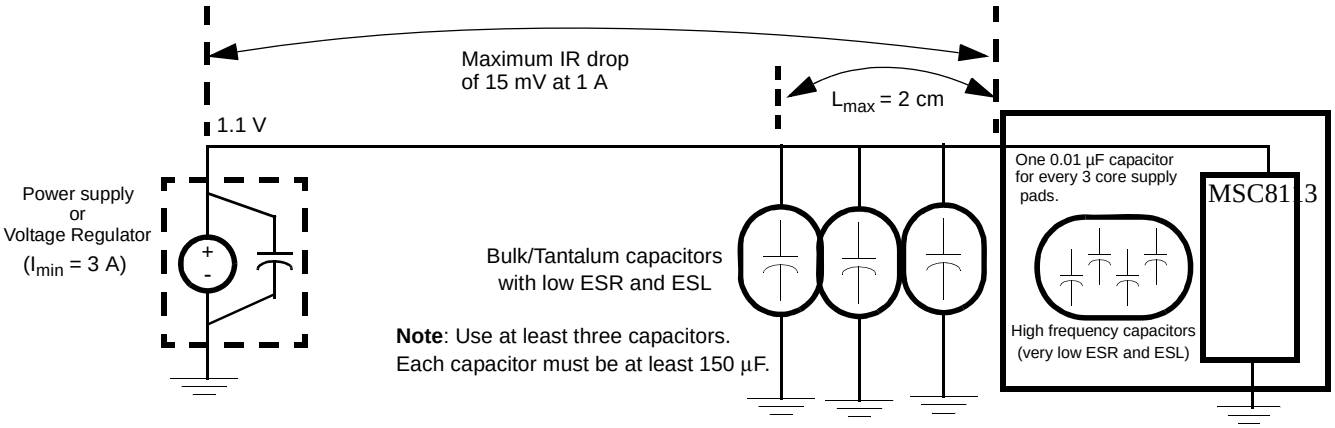


Figure 33. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8112 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8112 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Note: The MSC8112 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8112 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.

Note: See the Clock chapter in the *MSC8113 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8112 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or V_{DDH} or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

Note: For details on configuration, see the *MSC8112 User's Guide* and *MSC8112 Reference Manual*. For additional information, refer to the *MSC8113 Design Checklist* (ANxxxx).

3.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 133 MHz operation, you may have to use 133 or 166 MHz SDRAM. Always perform a detailed timing analysis using the MSC8112 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.

3.5 Thermal Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8112 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8112 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D) \quad \textit{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

Note: See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number	
					Lead-Free	Lead-Bearing
MSC8112	Flip Chip Plastic Ball Grid Array (FC-PBGA)	1.1 V	–40° to 105°C	300	MSC8112TVT2400V	MSC8112TMP2400V

6 Product Documentation

- *MSC8112 Technical Data Sheet* (MSC8112). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8112 device.
- *MSC8112 Reference Manual* (MSC8112RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8112 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.

7 Revision History

Table 31 provides a revision history for this data sheet.

Table 31. Document Revision History

Revision	Date	Description
0	5/2008	• Initial release.
1	12/2008	• Clarified the wording of note 2 in **Table 15** on p. 23.

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