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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC140 Core
Interface	Ethernet, I²C, TDM, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	448kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8112tmp2400v

1 Pin Assignments

This section includes diagrams of the MSC8112 package ball grid array layouts and pinout allocation tables.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.

Top View

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
B		V_{DD}	GND	GND	$\overline{\text{NMI OUT}}$	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GPIO0	V_{DD}	V_{DD}	GND
C	GND	V_{DD}	TDO	$\overline{\text{SRESET}}$	GPIO28	HCID1	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	GND	GPIO30	GPIO2	GPIO1	GPIO7	GPIO3	GPIO5	GPIO6
D	TDI	EE0	EE1	GND	V_{DDH}	HCID2	HCID3	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	GPIO31	GPIO29	V_{DDH}	GPIO4	V_{DDH}	GND	GPIO8
E	TCK	$\overline{\text{TRST}}$	TMS	$\overline{\text{HRESET}}$	GPIO27	HCID0	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	GND	V_{DD}	GND	GND	GPIO9	GPIO13	GPIO10	GPIO12
F	$\overline{\text{PORESET}}$	$\overline{\text{RSTCONF}}$	$\overline{\text{NMI}}$	HA29	HA22	GND	V_{DD}	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	ETHRX CLK	ETHTX CLK	GPIO20	GPIO18	GPIO16	GPIO11	GPIO14	GPIO19
G	HA24	HA27	HA25	HA23	HA17	$\overline{\text{PWE0}}$	V_{DD}	V_{DD}	BADDR 31	BM0	$\overline{\text{ABB}}$	V_{DD}	$\overline{\text{INT OUT}}$	ETHCRS	V_{DD}	$\overline{\text{CS1}}$	$\overline{\text{BCTL0}}$	GPIO15	GND	GPIO17	GPIO22
H	HA20	HA28	V_{DD}	HA19	TEST	$\overline{\text{PSDCAS}}$	$\overline{\text{PGTA}}$	V_{DD}	BM1	$\overline{\text{ARTRY}}$	$\overline{\text{AACK}}$	$\overline{\text{DBB}}$	$\overline{\text{HTA}}$	V_{DD}	TT4	$\overline{\text{CS4}}$	GPIO24	GPIO21	V_{DD}	V_{DDH}	A31
J	HA18	HA26	V_{DD}	HA13	GND	PSDA MUX	BADDR 27	V_{DD}	CLKIN	BM2	$\overline{\text{DBG}}$	V_{DD}	GND	V_{DD}	TT3	PSDA10	BCTL1	GPIO23	GND	GPIO25	A30
K	HA15	HA21	HA16	$\overline{\text{PWE3}}$	$\overline{\text{PWE1}}$	$\overline{\text{POE}}$	BADDR 30	Res.	GND	GND	GND	GND	CLKOUT	V_{DD}	TT2	ALE	$\overline{\text{CS2}}$	GND	A26	A29	A28
L	HA12	HA14	HA11	V_{DDH}	V_{DDH}	BADDR 28	BADDR 29	GND	GND	MSC8112			GND	V_{DDH}	GND	GND	$\overline{\text{CS3}}$	V_{DDH}	A27	A25	A22
M	HD28	HD31	V_{DDH}	GND	GND	GND	V_{DD}	V_{DDH}	GND				GND	V_{DDH}	$\overline{\text{HBRST}}$	V_{DDH}	V_{DDH}	GND	V_{DDH}	A24	A21
N	HD26	HD30	HD29	HD24	$\overline{\text{PWE2}}$	V_{DDH}	$\overline{\text{HWBS0}}$	$\overline{\text{HBCS}}$	GND				GND	$\overline{\text{HRDS}}$	$\overline{\text{BG}}$	$\overline{\text{HCS}}$	$\overline{\text{CS0}}$	$\overline{\text{PSDWE}}$	GPIO26	A23	A20
P	HD20	HD27	HD25	HD23	$\overline{\text{HWBS3}}$	$\overline{\text{HWBS2}}$	$\overline{\text{HWBS1}}$	HCLKIN	GND	GND_{SYN}	V_{CCSYN}	GND	GND	$\overline{\text{TA}}$	$\overline{\text{BR}}$	$\overline{\text{TEA}}$	$\overline{\text{PSDVAL}}$	DP0	V_{DDH}	GND	A19
R	HD18	V_{DDH}	GND	HD22	$\overline{\text{HWBS6}}$	$\overline{\text{HWBS4}}$	TSZ1	TSZ3	$\overline{\text{GBL}}$	V_{DD}	V_{DD}	V_{DD}	TT0	DP7	DP6	DP3	$\overline{\text{TS}}$	DP2	A17	A18	A16
T	HD17	HD21	HD1	HD0	$\overline{\text{HWBS7}}$	$\overline{\text{HWBS5}}$	TSZ0	TSZ2	$\overline{\text{TBST}}$	V_{DD}	D16	TT1	D21	D23	DP5	DP4	DP1	D30	GND	A15	A14
U	HD16	HD19	HD2	D2	D3	D6	D8	D9	D11	D14	D15	D17	D19	D22	D25	D26	D28	D31	V_{DDH}	A12	A13
V	HD3	V_{DDH}	GND	D0	D1	D4	D5	D7	D10	D12	D13	D18	D20	GND	D24	D27	D29	A8	A9	A10	A11
W	HD6	HD5	HD4	GND	GND	V_{DDH}	V_{DDH}	GND	HDST1	HDST0	V_{DDH}	GND	HD40	V_{DDH}	HD33	V_{DDH}	HD32	GND	GND	A7	A6
Y	HD7	HD15	V_{DDH}	HD9	V_{DD}	HD60	HD58	GND	V_{DDH}	HD51	GND	V_{DDH}	HD43	GND	V_{DDH}	GND	HD37	HD34	V_{DDH}	A4	A5
AA	V_{DD}	HD14	HD12	HD10	HD63	HD59	GND	V_{DDH}	HD54	HD52	V_{DDH}	GND	V_{DDH}	HD46	GND	HD42	HD38	HD35	A0	A2	A3
AB	GND	HD13	HD11	HD8	HD62	HD61	HD57	HD56	HD55	HD53	HD50	HD49	HD48	HD47	HD45	HD44	HD41	HD39	HD36	A1	V_{DD}

Figure 3. MSC8112 Package, Top View

Bottom View

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2
B	GND	V_{DD}	V_{DD}	GPIO0	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	NMI OUT	GND	GND	V_{DD}	
C	GPIO6	GPIO5	GPIO3	GPIO7	GPIO1	GPIO2	GPIO30	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID1	GPIO28	S RESET	TDO	V_{DD}	GND
D	GPIO8	GND	V_{DDH}	GPIO4	V_{DDH}	GPIO29	GPIO31	V_{DD}	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID3	HCID2	V_{DDH}	GND	EE1	EE0	TDI
E	GPIO12	GPIO10	GPIO13	GPIO9	GND	GND	V_{DD}	GND	GND	V_{DD}	GND	V_{DD}	GND	V_{DD}	GND	HCID0	GPIO27	HRESET	TMS	TRST	TCK
F	GPIO19	GPIO14	GPIO11	GPIO16	GPIO18	GPIO20	ETHTX_CLK	ETHRX_CLK	V_{DD}	GND	V_{DD}	GND	V_{DD}	V_{DD}	V_{DD}	GND	HA22	HA29	NMI	RST CONF	PO RESET
G	GPIO22	GPIO17	GND	GPIO15	BCTL0	CS1	V_{DD}	ETHCRS	INT OUT	V_{DD}	ABB	BM0	BADDR31	V_{DD}	V_{DD}	PWE0	HA17	HA23	HA25	HA27	HA24
H	A31	V_{DDH}	V_{DD}	GPIO21	GPIO24	CS4	TT4	V_{DD}	HTA	DBB	AACK	ARTRY	BM1	V_{DD}	PGTA	PSD CAS	TEST	HA19	V_{DD}	HA28	HA20
J	A30	GPIO25	GND	GPIO23	BCTL1	PSDA10	TT3	V_{DD}	GND	V_{DD}	DBG	BM2	CLKIN	V_{DD}	BADDR27	PSDA MUX	GND	HA13	V_{DD}	HA26	HA18
K	A28	A29	A26	GND	CS2	ALE	TT2	V_{DD}	CLKOUT	GND	GND	GND	GND	Res.	BADDR30	POE	PWE1	PWE3	HA16	HA21	HA15
L	A22	A25	A27	V_{DDH}	CS3	GND	GND	V_{DDH}	GND				GND	GND	BADDR29	BADDR28	V_{DDH}	V_{DDH}	HA11	HA14	HA12
M	A21	A24	V_{DDH}	GND	V_{DDH}	V_{DDH}	HB RST	V_{DDH}	GND		MSC8112		GND	V_{DDH}	V_{DD}	GND	GND	GND	V_{DDH}	HD31	HD28
N	A20	A23	GPIO26	PSDWE	CS0	HCS	BG	HRDS	GND				GND	HBCS	HWBS0	V_{DDH}	PWE2	HD24	HD29	HD30	HD26
P	A19	GND	V_{DDH}	DP0	PSD VAL	TEA	BR	TA	GND	GND	V_{CCSYN}	GND_{SYN}	GND	HCLKIN	HWBS1	HWBS2	HWBS3	HD23	HD25	HD27	HD20
R	A16	A18	A17	DP2	TS	DP3	DP6	DP7	TT0	V_{DD}	V_{DD}	V_{DD}	GBL	TSZ3	TSZ1	HWBS4	HWBS6	HD22	GND	V_{DDH}	HD18
T	A14	A15	GND	D30	DP1	DP4	DP5	D23	D21	TT1	D16	V_{DD}	TBST	TSZ2	TSZ0	HWBS5	HWBS7	HD0	HD1	HD21	HD17
U	A13	A12	V_{DDH}	D31	D28	D26	D25	D22	D19	D17	D15	D14	D11	D9	D8	D6	D3	D2	HD2	HD19	HD16
V	A11	A10	A9	A8	D29	D27	D24	GND	D20	D18	D13	D12	D10	D7	D5	D4	D1	D0	GND	V_{DDH}	HD3
W	A6	A7	GND	GND	HD32	V_{DDH}	HD33	V_{DDH}	HD40	GND	V_{DDH}	HDST0	HDST1	GND	V_{DDH}	V_{DDH}	GND	GND	HD4	HD5	HD6
Y	A5	A4	V_{DDH}	HD34	HD37	GND	V_{DDH}	GND	HD43	V_{DDH}	GND	HD51	V_{DDH}	GND	HD58	HD60	V_{DD}	HD9	V_{DDH}	HD15	HD7
AA	A3	A2	A0	HD35	HD38	HD42	GND	HD46	V_{DDH}	GND	V_{DDH}	HD52	HD54	V_{DDH}	GND	HD59	HD63	HD10	HD12	HD14	V_{DD}
AB	V_{DD}	A1	HD36	HD39	HD41	HD44	HD45	HD47	HD48	HD49	HD50	HD53	HD55	HD56	HD57	HD61	HD62	HD8	HD11	HD13	GND

Figure 4. MSC8112 Package, Bottom View

Table 1. MSC8112 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
M15	V_{DDH}	P12	V_{CCSYN}
M16	$\overline{\text{HBRST}}$	P13	GND
M17	V_{DDH}	P14	GND
M18	V_{DDH}	P15	$\overline{\text{TA}}$
M19	GND	P16	$\overline{\text{BR}}$
M20	V_{DDH}	P17	$\overline{\text{TEA}}$
M21	A24	P18	$\overline{\text{PSDVAL}}$
M22	A21	P19	DP0/DREQ1/$\overline{\text{EXT\_BR2}}$
N2	HD26	P20	V_{DDH}
N3	HD30	P21	GND
N4	HD29	P22	A19
N5	HD24	R2	HD18
N6	$\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$	R3	V_{DDH}
N7	V_{DDH}	R4	GND
N8	$\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$	R5	HD22
N9	$\overline{\text{HBCS}}$	R6	$\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$
N10	GND	R7	$\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$
N14	GND	R8	TSZ1
N15	$\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$	R9	TSZ3
N16	$\overline{\text{BG}}$	R10	$\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$
N17	$\overline{\text{HCS}}$	R11	V_{DD}
N18	$\overline{\text{CS0}}$	R12	V_{DD}
N19	$\overline{\text{PSDWE}}$/PGPL1	R13	V_{DD}
N20	GPIO26/TDM0RDAT	R14	TT0/HA7
N21	A23	R15	$\overline{\text{IRQ7}}$/DP7/DREQ4
N22	A20	R16	$\overline{\text{IRQ6}}$/DP6/DREQ3
P2	HD20	R17	$\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$
P3	HD27	R18	$\overline{\text{TS}}$
P4	HD25	R19	$\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$
P5	HD23	R20	A17
P6	$\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$	R21	A18
P7	$\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$	R22	A16
P8	$\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$	T2	HD17
P9	HCLKIN	T3	HD21
P10	GND	T4	HD1/DSISYNC
P11	GND_{SYN}	T5	HD0/SWTE

Table 1. MSC8112 Signal Listing by Ball Designator (continued)

Des.	Signal Name	Des.	Signal Name
T6	$\overline{\text{HWBS7}}$/$\overline{\text{HDBS7}}$/$\overline{\text{HWBE7}}$/$\overline{\text{HDBE7}}$/$\overline{\text{PWE7}}$/$\overline{\text{PSDDQM7}}$/$\overline{\text{PBS7}}$	U21	A12
T7	$\overline{\text{HWBS5}}$/$\overline{\text{HDBS5}}$/$\overline{\text{HWBE5}}$/$\overline{\text{HDBE5}}$/$\overline{\text{PWE5}}$/$\overline{\text{PSDDQM5}}$/$\overline{\text{PBS5}}$	U22	A13
T8	TSZ0	V2	HD3/MODCK1
T9	TSZ2	V3	V_{DDH}
T10	$\overline{\text{TBST}}$	V4	GND
T11	V_{DD}	V5	D0
T12	D16	V6	D1
T13	TT1	V7	D4
T14	D21	V8	D5
T15	D23	V9	D7
T16	$\overline{\text{IRQ5}}$/DP5/$\overline{\text{DACK4}}$/$\overline{\text{EXT\_BG3}}$	V10	D10
T17	$\overline{\text{IRQ4}}$/DP4/$\overline{\text{DACK3}}$/$\overline{\text{EXT\_DBG3}}$	V11	D12
T18	$\overline{\text{IRQ1}}$/DP1/$\overline{\text{DACK1}}$/$\overline{\text{EXT\_BG2}}$	V12	D13
T19	D30	V13	D18
T20	GND	V14	D20
T21	A15	V15	GND
T22	A14	V16	D24
U2	HD16	V17	D27
U3	HD19	V18	D29
U4	HD2/DSI64	V19	A8
U5	D2	V20	A9
U6	D3	V21	A10
U7	D6	V22	A11
U8	D8	W2	HD6
U9	D9	W3	HD5/CNFGS
U10	D11	W4	HD4/MODCK2
U11	D14	W5	GND
U12	D15	W6	GND
U13	D17	W7	V_{DDH}
U14	D19	W8	V_{DDH}
U15	D22	W9	GND
U16	D25	W10	HDST1/HA10
U17	D26	W11	HDST0/HA9
U18	D28	W12	V_{DDH}
U19	D31	W13	GND
U20	V_{DDH}	W14	HD40/D40/ETHRXD0

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8112 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8112.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core and PLL supply voltage	V_{DD}	–0.2 to 1.6	V
I/O supply voltage	V_{DDH}	–0.2 to 4.0	V
Input voltage	V_{IN}	–0.2 to 4.0	V
Maximum operating temperature:	T_J	105	°C
Minimum operating temperature	T_J	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature (T_J).

Table 5. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Input high voltage[1], all inputs except CLKIN	V_{IH}	2.0	—	3.465	V
Input low voltage[1]	V_{IL}	GND	0	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.0	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0	0.8	V
Input leakage current, $V_{IN} = V_{DDH}$	I_{IN}	–1.0	0.09	1	µA
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, V_{IL} = 0.8 V[2]	I_L	–1.0	0.09	1	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–1.0	0.09	1	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0	0.4	V
V_{CCSYN} PLL supply current	I_{VCCSYN}	—	2	4	mA
Internal supply current: • Wait mode • Stop mode	 I_{DDW} I_{DDS}	 — —	 375[3] 290[3]	 — —	 mA mA
Typical power 300 MHz at 1.1 V[4]	P	—	554	—	mW

Notes:
1. See **Figure 5** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.1 V core at 25°C junction temperature.
4. The typical power values were calculated using a power calculator configured for two cores performing an EFR code with the device running at the specified operating frequency and a junction temperature of 25°C. No peripherals were included. The calculator was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Section 3** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

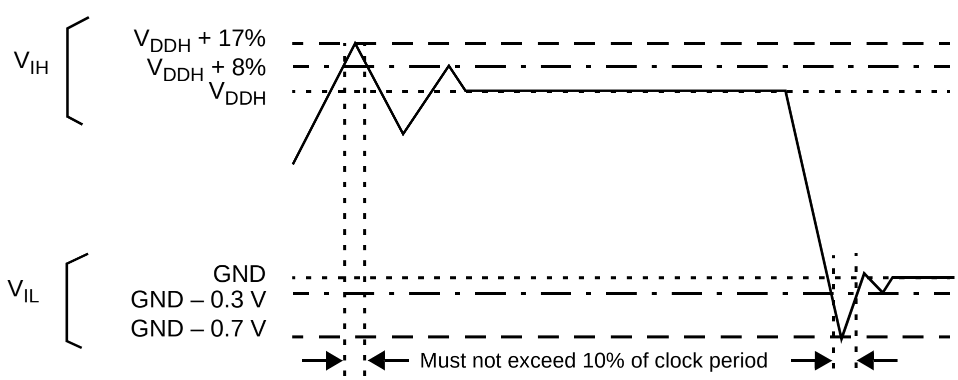


Figure 5. Overshoot/Undershoot Voltage for V_{IH} and V_{IL}

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

Table 6. Output Buffer Impedances

Output Buffers	Typical Impedance (Ω)
System bus	50
Memory controller	50
Parallel I/O	50
Note: These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature.	

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8112 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the V_{DD} and V_{DDH} levels together. For designs with separate power supplies, bring up the V_{DD} levels and then the V_{DDH} levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after V_{DDH} reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during V_{DDH} power-up. CLKIN can toggle during this period.

Note: See **Section 3.1** for start-up sequencing recommendations and **Section 3.2** for power supply design recommendations.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which V_{DD} and V_{DDH} are raised together. **Figure 7** shows a sequence in which V_{DDH} is raised after V_{DD} and CLKIN begins to toggle as V_{DDH} rises.

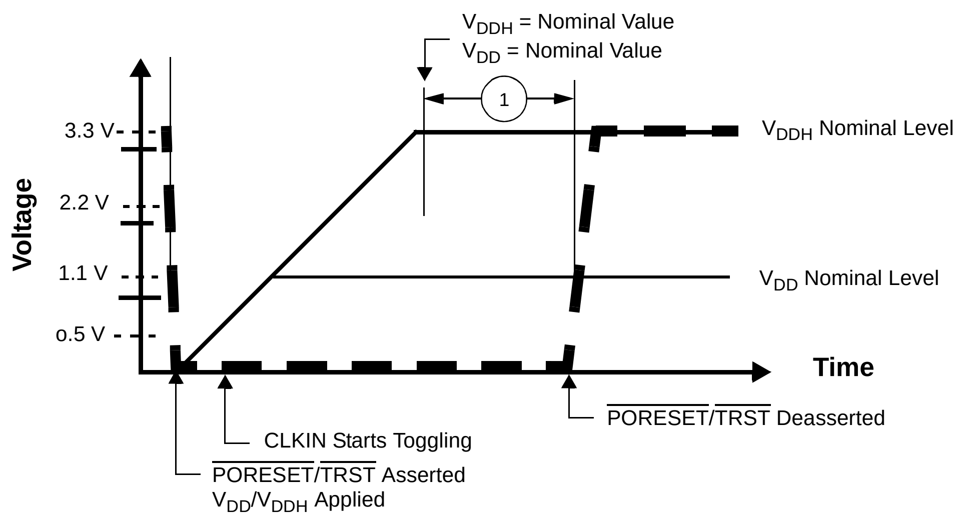


Figure 6. Start-Up Sequence: V_{DD} and V_{DDH} Raised Together

2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz
Core frequency	300
Reference frequency (REFCLK)	100
Internal bus frequency (BLCK)	100
DSI clock frequency (HCLKIN)	HCLKIN ≤ (min{70 MHz, CLKOUT})
External clock frequency (CLKIN or CLKOUT)	100

Table 8. Clock Frequencies

Characteristics	Symbol	Min	Max
CLKIN frequency	F_{CLKIN}	20	100
BCLK frequency	F_{BCLK}	40	100
Reference clock (REFCLK) frequency	F_{REFCLK}	40	100
Output clock (CLKOUT) frequency	F_{CLKOUT}	40	100
SC140 core clock frequency	F_{CORE}	200	300
Note: The rise and fall time of external clocks should be 3 ns maximum			

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
Phase jitter between BCLK and CLKIN	—	0.3	ns
CLKIN frequency	20	see **Table 8**	MHz
CLKIN slope	—	3	ns
CLKIN period jitter[1]	—	150	ps
CLKIN jitter spectrum	150	—	KHz
PLL input clock (after predivider)	20	100	MHz
PLL output frequency (VCO output)	800	1200	MHz
CLKOUT frequency jitter[1]	—	200	ps
CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps.	—	500	ps
Notes: **1.** Peak-to-peak. **2.** Not tested. Guaranteed by design.			

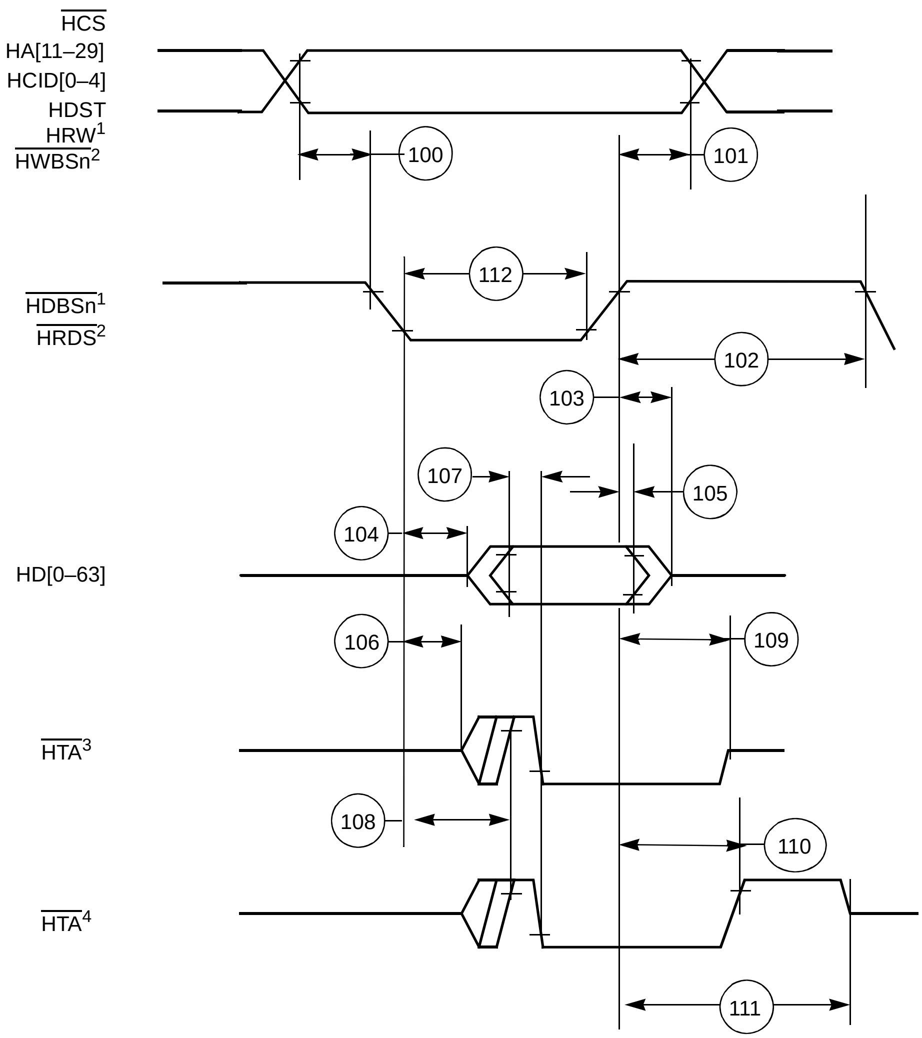
2.5.4 Reset Timing

The MSC8112 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8112 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

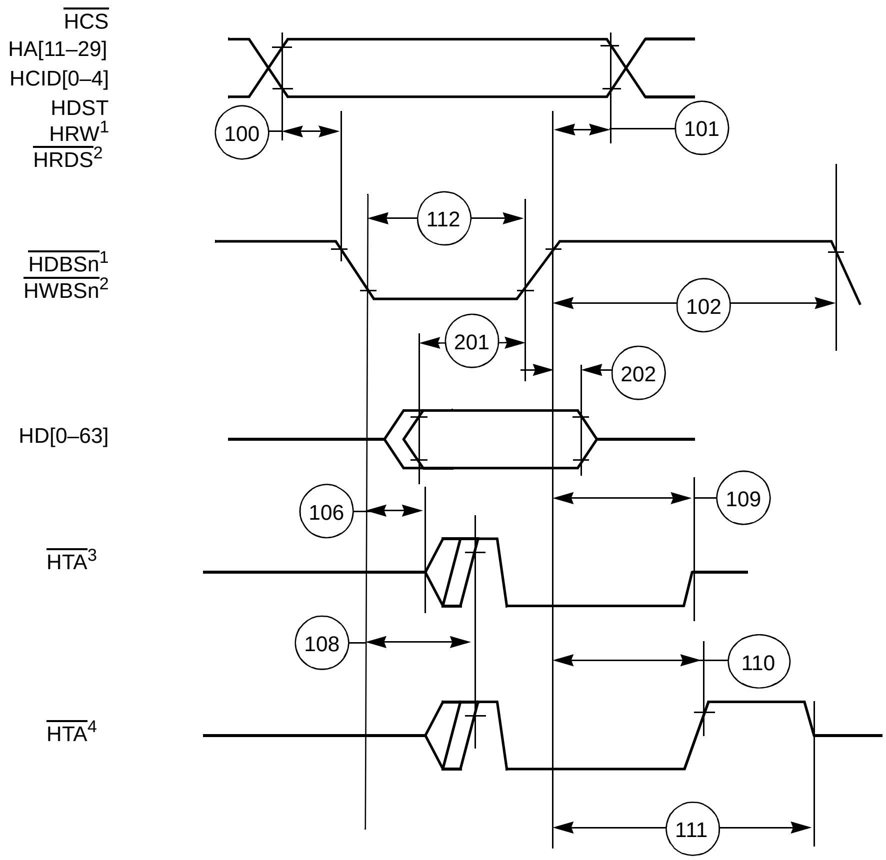
Figure 14 shows DSI asynchronous read signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram

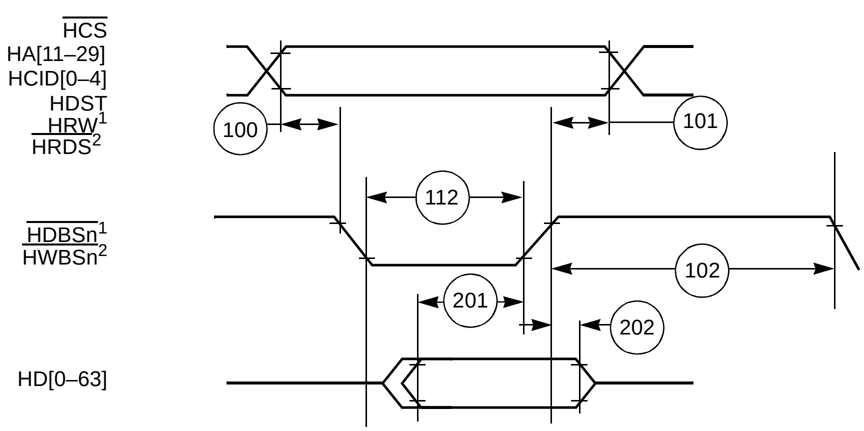
Figure 15 shows DSI asynchronous write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 15. Asynchronous Single- and Dual-Strobe Modes Write Timing Diagram

Figure 16 shows DSI asynchronous broadcast write signals timing.



Notes:
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 16. Asynchronous Broadcast Write Timing Diagram

2.5.6.2 DSI Synchronous Mode

Table 19. DSI Inputs in Synchronous Mode

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
120	HCLKIN cycle time[1,2]	HTC	10.0	55.6	ns
121	HCLKIN high pulse width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
122	HCLKIN low pulse width	$(0.5 \pm 0.1) \times$ HTC	4.0	33.3	ns
123	HA[11–29] inputs set-up time	—	1.2	—	ns
124	HD[0–63] inputs set-up time	—	0.6	—	ns
125	HCID[0–4] inputs set-up time	—	1.3	—	ns
126	All other inputs set-up time	—	1.2	—	ns
127	All inputs hold time	—	1.5	—	ns

Notes:
1. Values are based on a frequency range of 18–70 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

Table 20. DSI Outputs in Synchronous Mode

No.	Characteristic	1.1 V Core		Units
		Min	Max	
128	HCLKIN high to HD[0–63] output active	2.0	—	ns
129	HCLKIN high to HD[0–63] output valid	—	7.6	ns
130	HD[0–63] output hold time	1.7	—	ns
131	HCLKIN high to HD[0–63] output high impedance	—	8.3	ns
132	HCLKIN high to $\overline{\text{HTA}}$ output active	2.2	—	ns
133	HCLKIN high to $\overline{\text{HTA}}$ output valid	—	7.4	ns
134	$\overline{\text{HTA}}$ output hold time	1.7	—	ns
135	HCLKIN high to $\overline{\text{HTA}}$ high impedance	—	7.5	ns

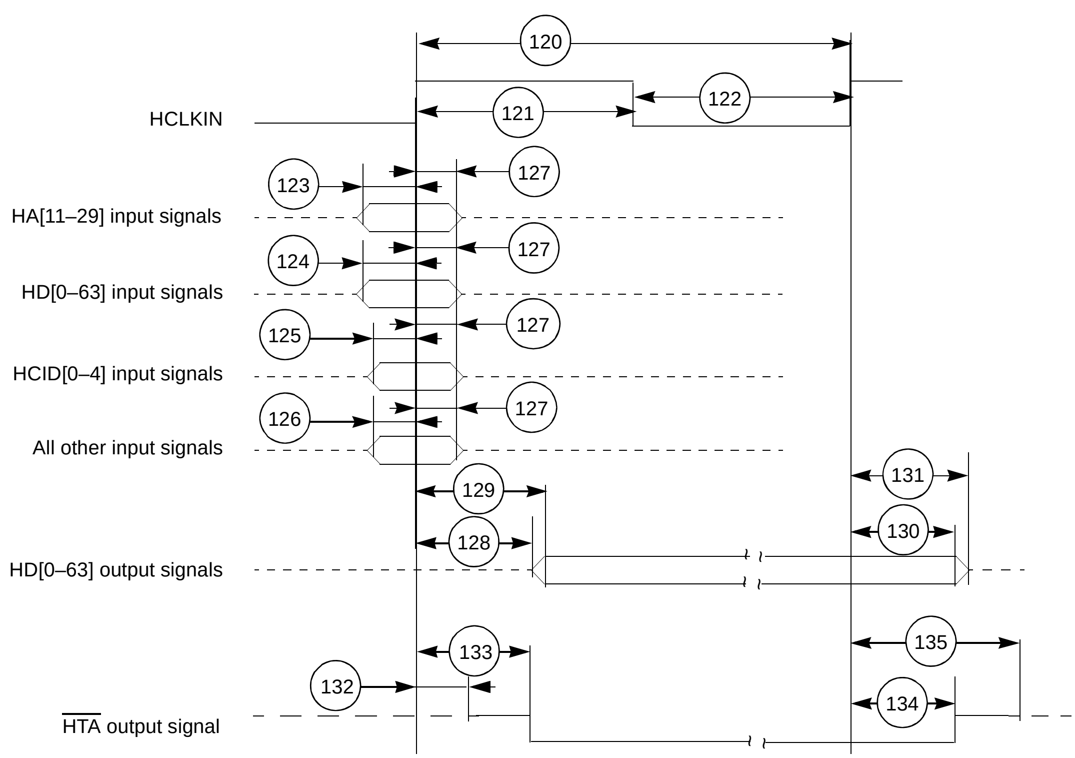


Figure 17. DSI Synchronous Mode Signals Timing Diagram

2.5.7 TDM Timing

Table 21. TDM Timing

No.	Characteristic	Expression	1.1 V Core		Units
			Min	Max	
300	TDMxRCLK/TDMxTCLK	TC[1]	16	—	ns
301	TDMxRCLK/TDMxTCLK high pulse width	(0.5 ± 0.1) × TC	7	—	ns
302	TDMxRCLK/TDMxTCLK low pulse width	(0.5 ± 0.1) × TC	7	—	ns
303	TDM receive all input set-up time		1.3	—	ns
304	TDM receive all input hold time		1.0	—	ns
305	TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3]		2.8	—	ns
306	TDMxTCLK high to TDMxTDAT/TDMxRCLK output		—	10.0	ns
307	All output hold time[4]		2.5	—	ns
308	TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3]		—	10.7	ns
309	TDMxTCLK high to TDMXTSYN output valid[2]		—	9.7	ns
310	TDMxTSYN output hold time[4]		2.5	—	ns

Notes:
1. Devices operating at 300 MHz are limited to a maximum TDMxRCLK/TDMxTCLK frequency of 50 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8112 Reference Manual* for details.
4. Values are based on 10 pF capacitive load.

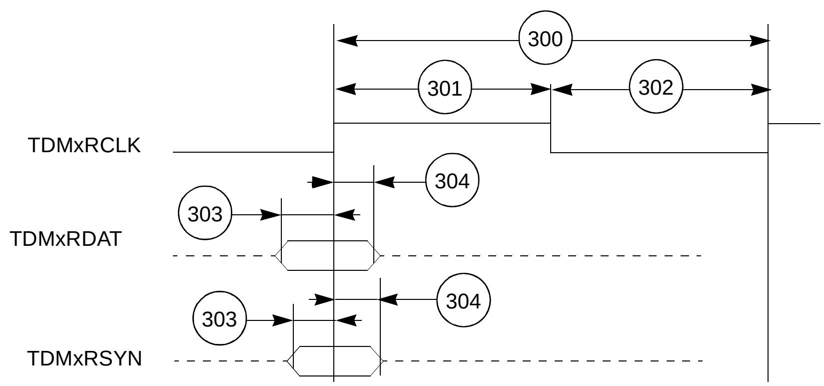


Figure 18. TDM Inputs Signals

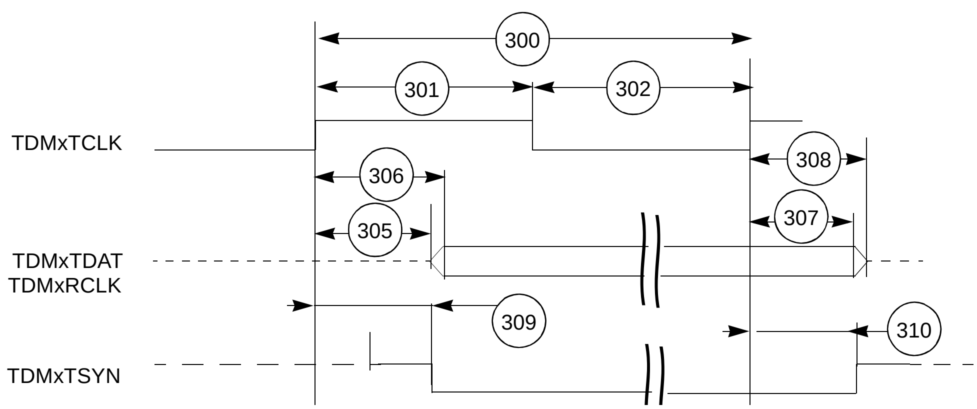


Figure 19. TDM Output Signals

2.5.8 UART Timing

Table 22. UART Timing

No.	Characteristics	Expression	Min	Max	Unit
400	URXD and UTXD inputs high/low duration	$16 \times T_{REFCLK}$	160.0	—	ns
401	URXD and UTXD inputs rise/fall time			10	ns
402	UTXD output rise/fall time			10	ns

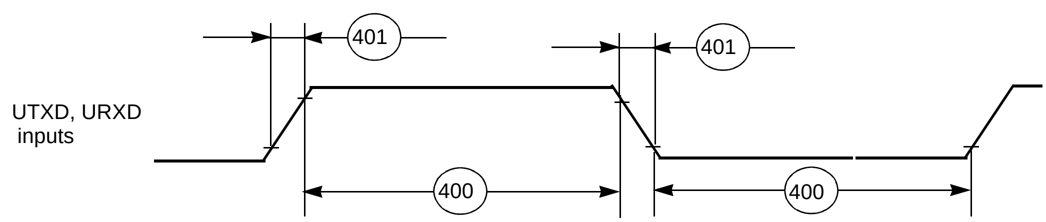


Figure 20. UART Input Timing

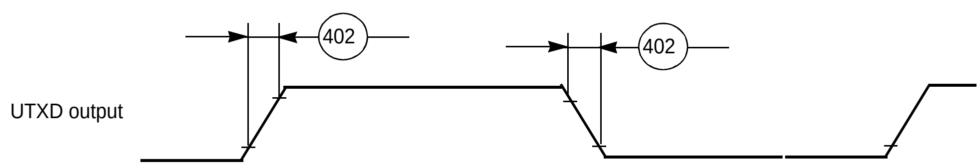


Figure 21. UART Output Timing

2.5.9 Timer Timing

Table 23. Timer Timing

No.	Characteristics	Ref = CLKIN		Unit
		Min	Max	
500	TIMERx frequency	10.0	—	ns
501	TIMERx Input high period	4.0	—	ns
502	TIMERx Output low period	4.0	—	ns
503	TIMERx Propagations delay from its clock input	3.1	9.5	ns

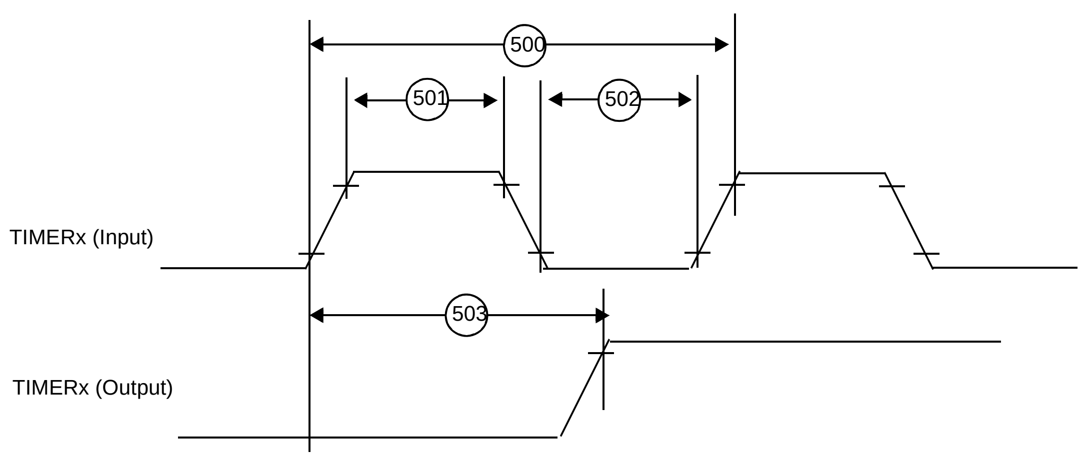


Figure 22. Timer Timing

2.5.10.3 RMII Mode

Table 26. RMII Mode Signal Timing

No.	Characteristics	1.1 V Core		Unit
		Min	Max	
806	ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time	1.6	—	ns
807	ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time	1.6	—	ns
811	ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay.	3	12.5	ns

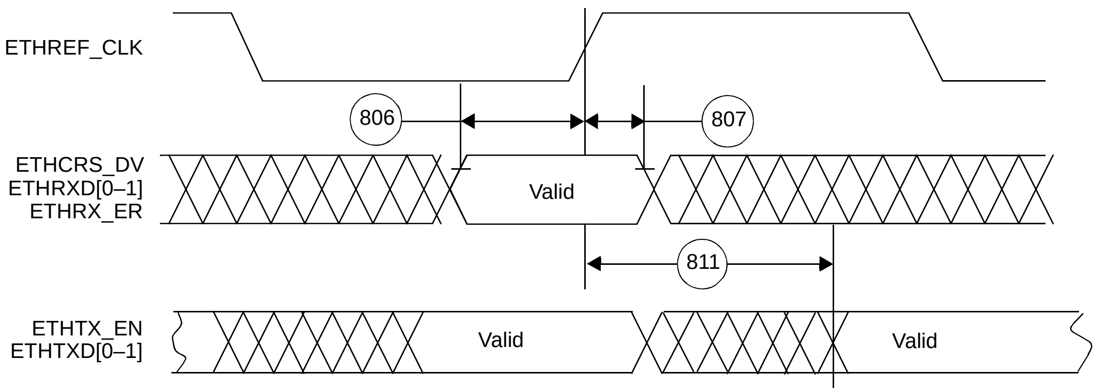


Figure 25. RMII Mode Signal Timing

2.5.10.4 SMII Mode

Table 27. SMII Mode Signal Timing

No.	Characteristics	Min	Max	Unit
808	ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time	1.0	—	ns
809	ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	1.0	—	ns
810	ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	1.5[1]	6.0[2]	ns

Notes:
1. Measured using a 5 pF load.
2. Measured using a 15 pF load.

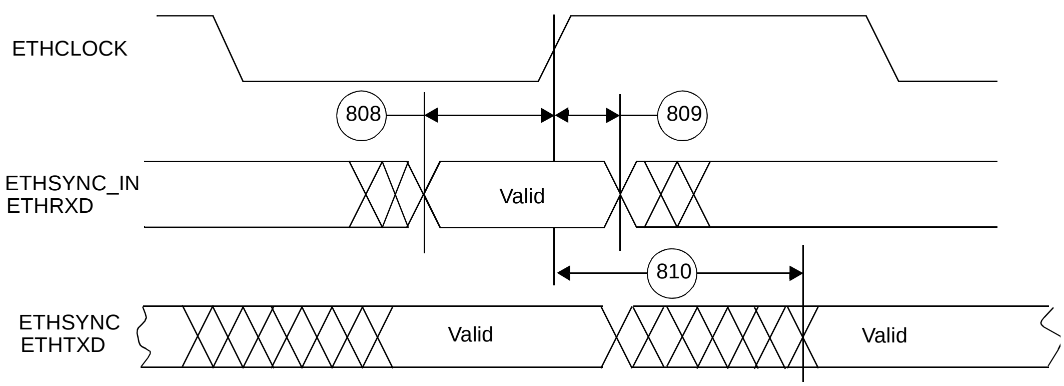


Figure 26. SMII Mode Signal Timing

2.5.13 JTAG Signals

Table 30. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/(T_C × 4); maximum 25 MHz)	0.0	25	MHz
701	TCK cycle time	40.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V • High • Low	 20.0 16.0	 — —	 ns ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	20.0	—	ns
706	TCK low to output data valid	0.0	30.0	ns
707	TCK low to output high impedance	0.0	30.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	20.0	—	ns
710	TCK low to TDO data valid	0.0	20.0	ns
711	TCK low to TDO high impedance	0.0	20.0	ns
712	$\overline{TRST}$ assert time	100.0	—	ns
713	$\overline{TRST}$ set-up time to TCK low	30.0	—	ns
Note:	All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.			

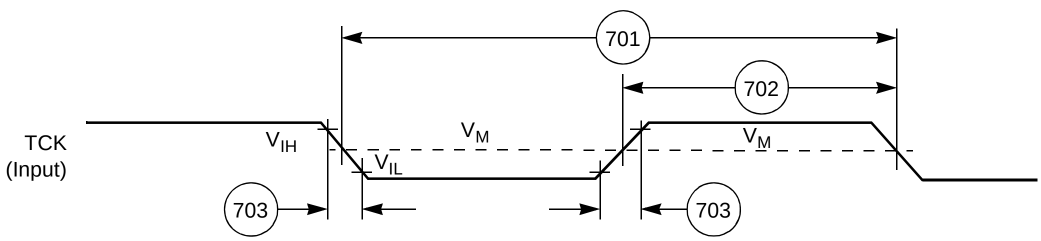


Figure 29. Test Clock Input Timing Diagram

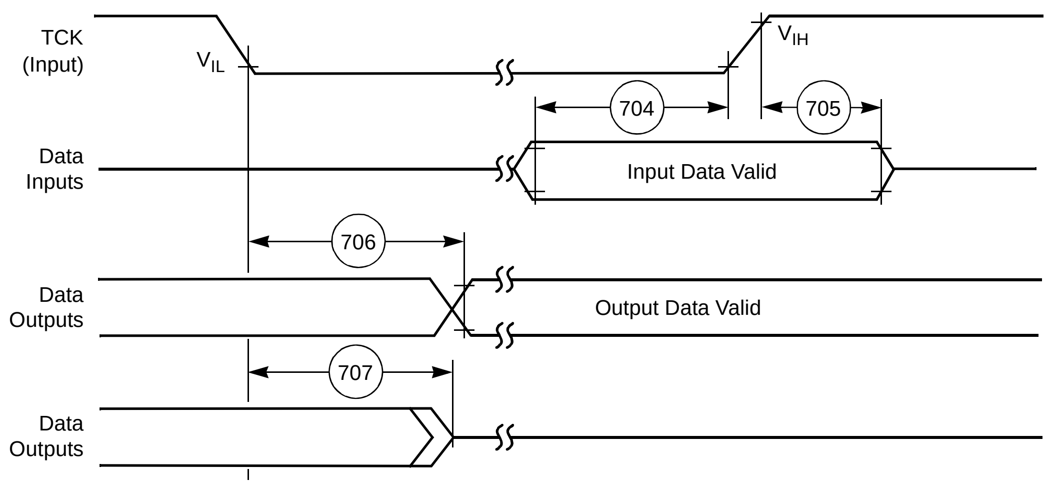


Figure 30. Boundary Scan (JTAG) Timing Diagram

During the power-up sequence, if V_{DD} rises before V_{DDH} (see **Figure 6**), current can pass from the V_{DD} supply through the device ESD protection circuits to the V_{DDH} supply. The ESD protection diode can allow this to occur when V_{DD} exceeds V_{DDH} by more than 0.8 V. Design the power supply to prevent or minimize this effect using one of the following optional methods:

- Never allow V_{DD} to exceed V_{DDH} + 0.8V.
- Design the V_{DDH} supply to prevent reverse current flow by adding a minimum 10 Ω resistor to GND to limit the current. Such a design yields an initial V_{DDH} level of V_{DD} – 0.8 V before it is enabled.

After power-up, V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 2.6 V.

3.2 Power Supply Design Considerations

When implementing a new design, use the guidelines described in the *MSC8112 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information. See **Section 2.5.2** for start-up timing specifications.

Figure 33 shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.1 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8112 device.

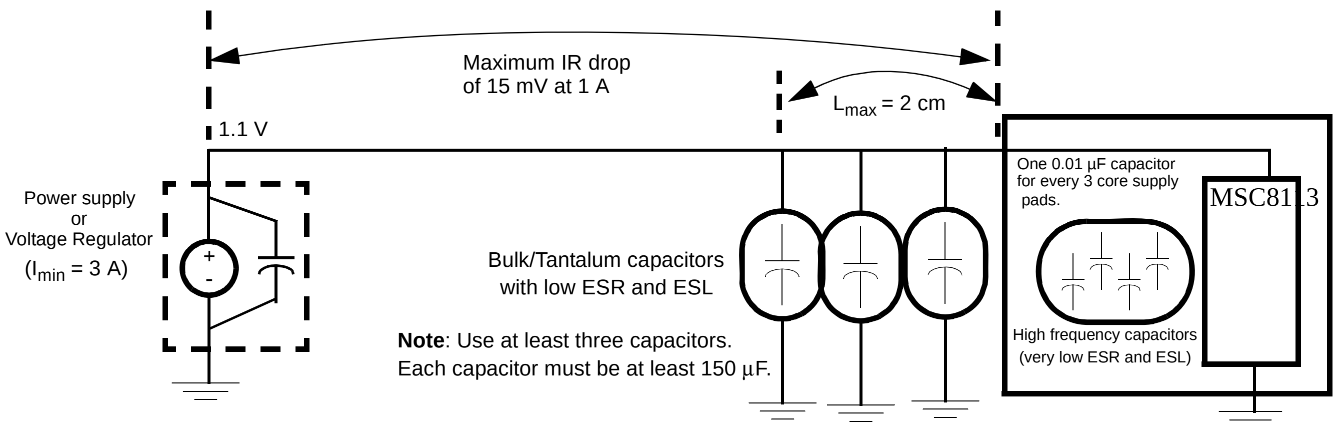


Figure 33. Core Power Supply Decoupling

Each V_{CC} and V_{DD} pin on the MSC8112 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The V_{CC} power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC}, V_{DD}, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MSC8112 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC}, V_{DD}, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: V_{CCSYN}-GND_{SYN}. To ensure internal clock stability, filter the power to the V_{CCSYN} input with a circuit similar to the one in **Figure 34**. For optimal noise filtering, place the circuit as close as possible to V_{CCSYN}. The 0.01-µF capacitor should be closest to V_{CCSYN}, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to V_{DD}. These traces should be kept short and direct. Provide an extremely low impedance path to the ground plane for GND_{SYN}. Bypass GND_{SYN} to V_{CCSYN} by a 0.01-µF capacitor located as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8112 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

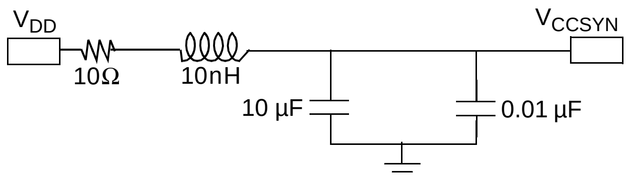


Figure 34. V_{CCSYN} Bypass

3.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to V_{DDH} or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), $\overline{HCS}$ and $\overline{HBCS}$ must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, $\overline{HTA}$ must be pulled up. In asynchronous mode, $\overline{HTA}$ should be pulled either up or down, depending on design requirements.
- $\overline{HDST}$ can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up $\overline{HWBS[1–3]}$/$\overline{HDBS[1–3]}$/$\overline{HWBE[1–3]}$/$\overline{HDBE[1–3]}$ and $\overline{HWBS[4–7]}$/$\overline{HDBS[4–7]}$/$\overline{HWBE[4–7]}$/$\overline{HDBE[4–7]}$/$\overline{PWE[4–7]}$/$\overline{PSDDQM[4–7]}$/$\overline{PBS[4–7]}$.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{HWBS[1–3]}$/$\overline{HDBS[1–3]}$/$\overline{HWBE[1–3]}$/$\overline{HDBE[1–3]}$ must be pulled up.
- When the DSI is in asynchronous mode, $\overline{HBRST}$ and HCLKIN should either be disconnected or pulled up.
- When the DSI uses sliding window address mode (DCR[SLDWA] = 1), the external HA[11–13] signals must be connected (tied) to the correct voltage levels so that the host can perform the first access to the DCR. After reset, the DSI expects full address mode (DCR[SLDWA] = 0). The DCR address in the DSI memory map is 0x1BE000, which requires the following connections:
  - — HA11 must be pulled high (1)
  - — HA12 must be pulled high (1)
  - — HA13 must be pulled low (0)
- The following signals must be pulled up: $\overline{HRESET}$, $\overline{SRESET}$, $\overline{ARTRY}$, $\overline{TA}$, $\overline{TEA}$, $\overline{PSDVAL}$, and $\overline{AACK}$.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - — $\overline{BG}$, $\overline{DBG}$, and $\overline{TS}$ can be left unconnected.
  - — $\overline{EXT\_BG[2–3]}$, $\overline{EXT\_DBG[2–3]}$, and $\overline{GBL}$ can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - — $\overline{BR}$ must be pulled up.
  - — $\overline{EXT\_BR[2–3]}$ must be pulled up if multiplexed to the system bus functionality.
- If there is an external bus master (BCR[EBM] = 1):
  - — $\overline{BR}$, $\overline{BG}$, $\overline{DBG}$, and $\overline{TS}$ must be pulled up.
  - — $\overline{EXT\_BR[2–3]}$, $\overline{EXT\_BG[2–3]}$, and $\overline{EXT\_DBG[2–3]}$ must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, $\overline{ABB}$ and $\overline{DBB}$ can be selected as $\overline{IRQ}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

3.5 Thermal Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8112 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8112 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine T_J:

$$T_J = T_T + (\theta_{JA} \times P_D) \qquad \text{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)
θ_{JA} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

Note: See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number	
					Lead-Free	Lead-Bearing
MSC8112	Flip Chip Plastic Ball Grid Array (FC-PBGA)	1.1 V	–40° to 105°C	300	MSC8112TVT2400V	MSC8112TMP2400V

6 Product Documentation

- *MSC8112 Technical Data Sheet* (MSC8112). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8112 device.
- *MSC8112 Reference Manual* (MSC8112RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8112 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.

7 Revision History

Table 31 provides a revision history for this data sheet.

Table 31. Document Revision History

Revision	Date	Description
0	5/2008	• Initial release.
1	12/2008	• Clarified the wording of note 2 in **Table 15** on p. 23.