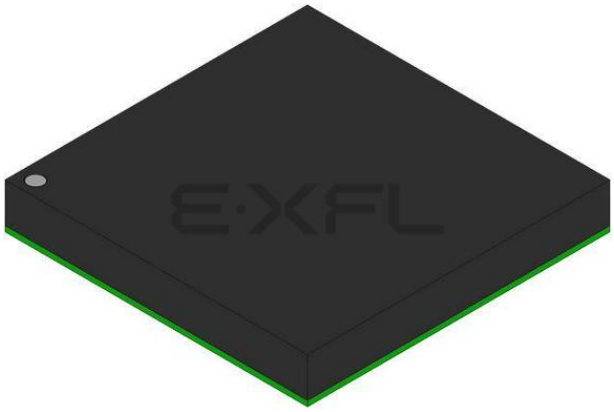

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	SC140 Core
Interface	Ethernet, I²C, TDM, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	448kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8112tvt2400v

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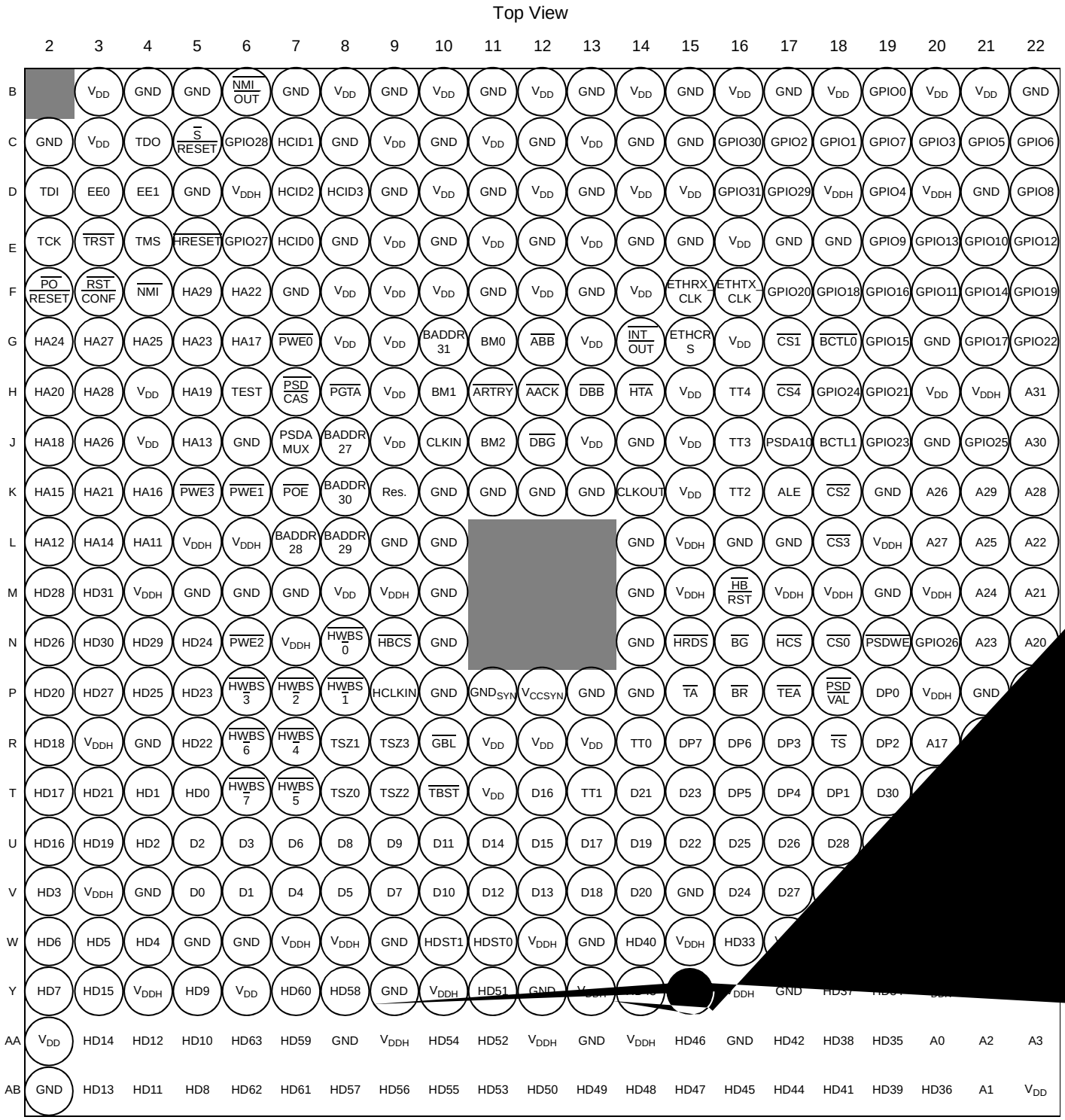

Figure 3. MSC8112 Package, Top View

2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

2.5.1 Output Buffer Impedances

2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. Section 2.5.3 describes the clocking characteristics. Section 2.5.4 describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8112 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See Table 2-11 for timing.
- If possible, bring up the V_{DD} and V_{DDH}

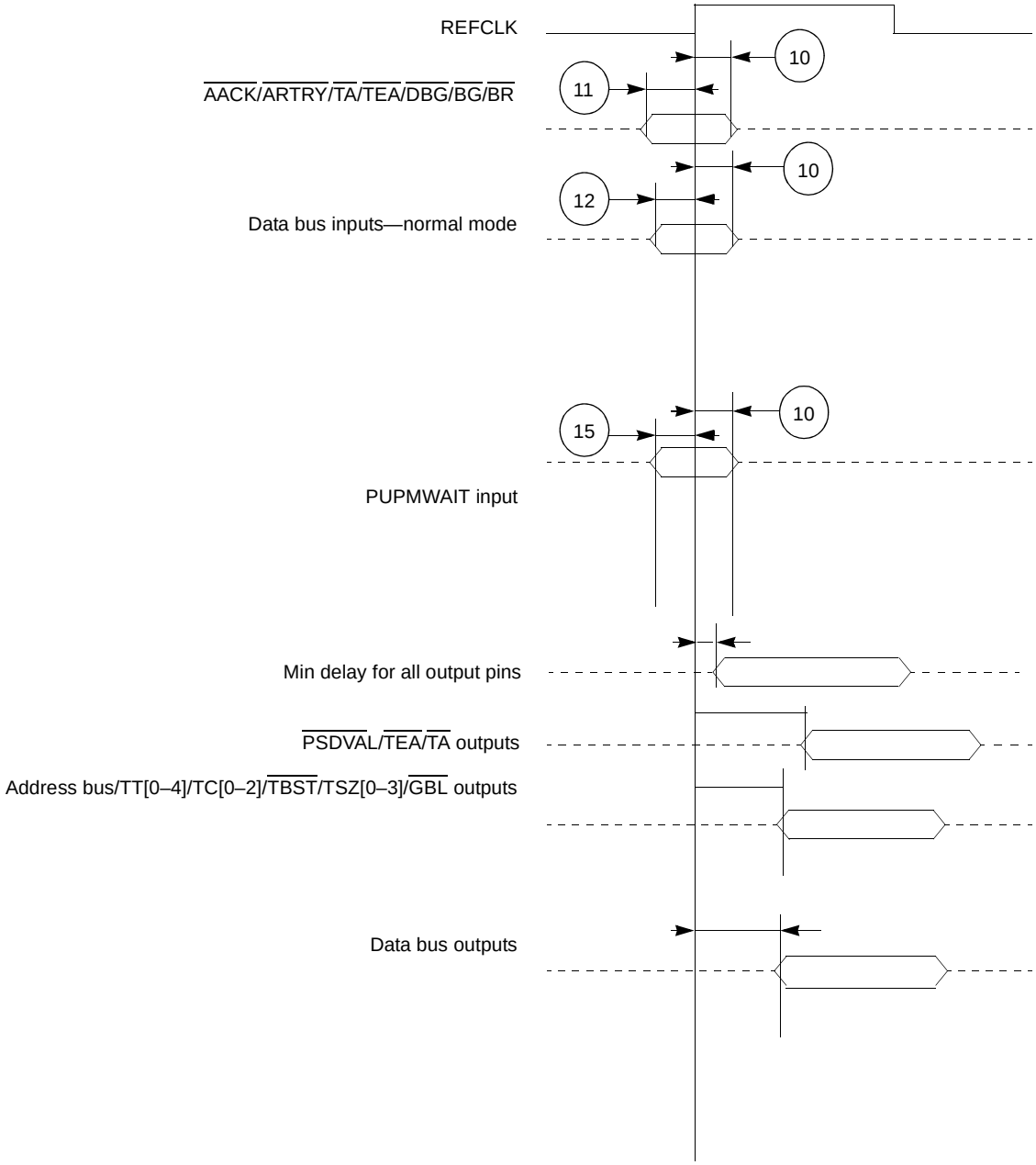

Figure 11. SIU Timing Diagram

Figure 14 shows DSI asynchronous read signals timing.

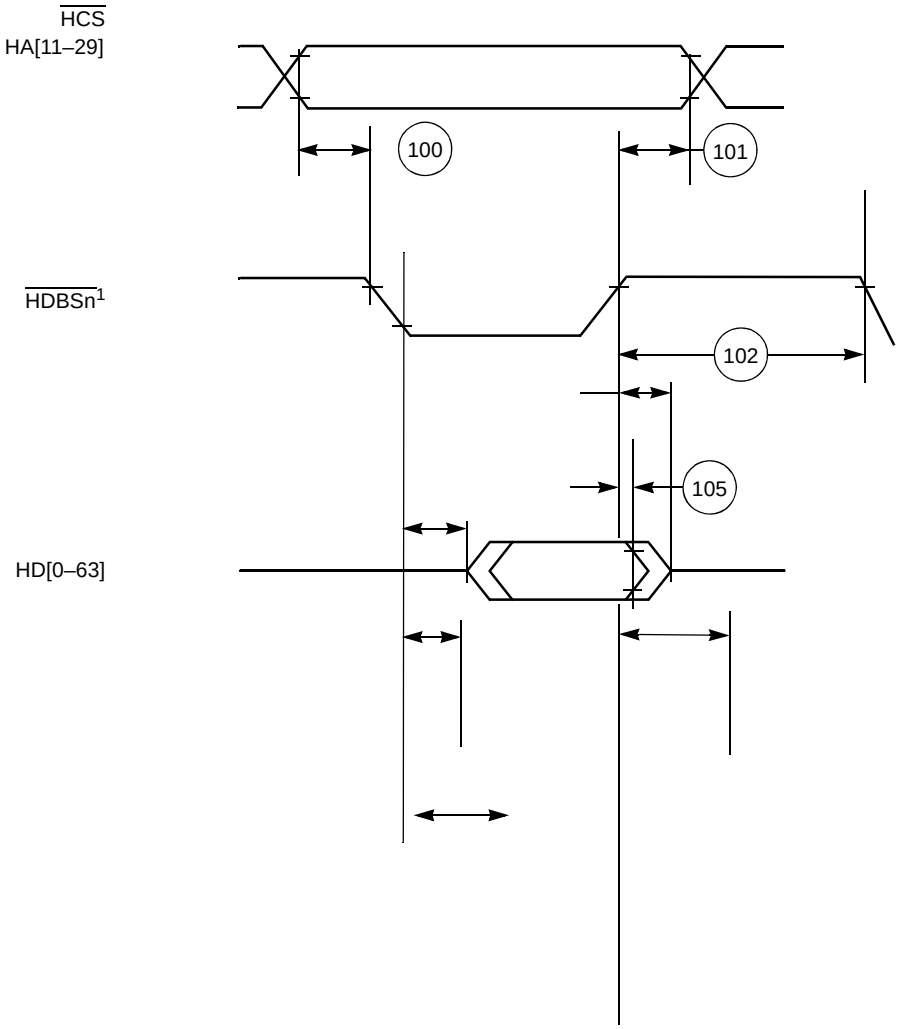

Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram