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### **Understanding Embedded - DSP (Digital Signal Processors)**

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

### **Applications of Embedded - DSP (Digital Signal Processors)**

#### **Details**

Product Status	Active
Type	SC140 Core
Interface	Ethernet, I <sup>2</sup> C, TDM, UART
Clock Rate	300MHz
Non-Volatile Memory	External
On-Chip RAM	448kB
Voltage - I/O	3.30V
Voltage - Core	1.10V
Operating Temperature	-40°C ~ 105°C
Mounting Type	Surface Mount
Package / Case	431-BFBGA, FCBGA
Supplier Device Package	431-FCPBGA (20x20)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=msc8112tvt2400v">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=msc8112tvt2400v</a>

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Top View

	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22			
B	V <sub>DD</sub>	GND	GND	NMI OUT	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GPI00	V <sub>DD</sub>	V <sub>DD</sub>	GND		
C	GND	V <sub>DD</sub>	TDO	S RESET	GPI028	HCID1	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	GND	GPI030	GPI02	GPI01	GPI07	GPI03	GPI05	GPI06			
D	TDI	EE0	EE1	GND	V <sub>DDH</sub>	HCID2	HCID3	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	V <sub>DD</sub>	GPI031	GPI029	V <sub>DDH</sub>	GPI04	V <sub>DDH</sub>	GND	GPI08			
E	TCK	TRST	TMS	HRESET	GPI027	HCID0	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	GND	V <sub>DD</sub>	GND	GND	GPI09	GPI013	GPI010	GPI012			
F	PO RESET	RST CONF	NMI	HA29	HA22	GND	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	GND	V <sub>DD</sub>	GND	V <sub>DD</sub>	ETHRX CLK	ETHTX CLK	GPI020	GPI018	GPI016	GPI011	GPI014	GPI019			
G	HA24	HA27	HA25	HA23	HA17	PWE0	V <sub>DD</sub>	V <sub>DD</sub>	BADDR 31	BM0	ABB	V <sub>DD</sub>	INT OUT	ETHCR S	V <sub>DD</sub>	CS1	BCTL0	GPI015	GND	GPI017	GPI022			
H	HA20	HA28	V <sub>DD</sub>	HA19	TEST	PSD CAS	PGTA	V <sub>DD</sub>	BM1	ARTRY	AACK	DBB	HTA	V <sub>DD</sub>	TT4	CS4	GPI024	GPI021	V <sub>DD</sub>	V <sub>DDH</sub>	A31			
J	HA18	HA26	V <sub>DD</sub>	HA13	GND	PSDA MUX	BADDR 27	V <sub>DD</sub>	CLKIN	BM2	DBG	V <sub>DD</sub>	GND	V <sub>DD</sub>	TT3	PSDA10	BCTL1	GPI023	GND	GPI025	A30			
K	HA15	HA21	HA16	PWE3	PWE1	POE	BADDR 30	Res.	GND	GND	GND	GND	CLKOUT	V <sub>DD</sub>	TT2	ALE	CS2	GND	A26	A29	A28			
L	HA12	HA14	HA11	V <sub>DDH</sub>	V <sub>DDH</sub>	BADDR 28	BADDR 29	GND	GND					GND	V <sub>DDH</sub>	GND	GND	CS3	V <sub>DDH</sub>	A27	A25	A22		
M	HD28	HD31	V <sub>DDH</sub>	GND	GND	GND	V <sub>DD</sub>	V <sub>DDH</sub>	GND					GND	V <sub>DDH</sub>	H RST	V <sub>DDH</sub>	V <sub>DDH</sub>	GND	V <sub>DDH</sub>	A24	A21		
N	HD26	HD30	HD29	HD24	PWE2	V <sub>DDH</sub>	HWBS 0	HBCS	GND					GND	HRDS	BG	HCS	CS0	PSDWE	GPI026	A23	A20		
P	HD20	HD27	HD25	HD23	HWBS 3	HWBS 2	HWBS 1	HCLKIN	GND	GND <sub>SYN</sub>	V <sub>CCSYN</sub>	GND	GND	GND	TA	BR	TEA	PSD VAL	DP0	V <sub>DDH</sub>	GND			
R	HD18	V <sub>DDH</sub>	GND	HD22	HWBS 6	HWBS 4	TSZ1	TSZ3	GBL	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>DD</sub>	TT0	DP7	DP6	DP3	TS	DP2	A17					
T	HD17	HD21	HD1	HD0	HWBS 7	HWBS 5	TSZ0	TSZ2	TBST	V <sub>DD</sub>	D16	TT1	D21	D23	DP5	DP4	DP1	D30						
U	HD16	HD19	HD2	D2	D3	D6	D8	D9	D11	D14	D15	D17	D19	D22	D25	D26	D28							
V	HD3	V <sub>DDH</sub>	GND	D0	D1	D4	D5	D7	D10	D12	D13	D18	D20	GND	D24	D27								
W	HD6	HD5	HD4	GND	GND	V <sub>DDH</sub>	V <sub>DDH</sub>	GND	HDST1	HDST0	V <sub>DDH</sub>	GND	HD40	V <sub>DDH</sub>	HD33									
Y	HD7	HD15	V <sub>DDH</sub>	HD9	V <sub>DD</sub>	HD60	HD58	GND	V <sub>DDH</sub>	HD51	GND	V <sub>DDH</sub>	HD41	V <sub>DDH</sub>	HD37	HD34	HD31							
AA	V <sub>DD</sub>	HD14	HD12	HD10	HD63	HD59	GND	V <sub>DDH</sub>	HD54	HD52	V <sub>DDH</sub>	GND	V <sub>DDH</sub>	HD46	GND	HD42	HD38	HD35	A0	A2	A3			
AB	GND	HD13	HD11	HD8	HD62	HD61	HD57	HD56	HD55	HD53	HD50	HD49	HD48	HD47	HD45	HD44	HD41	HD39	HD36	A1	V <sub>DD</sub>			

Figure 3. MSC8112 Package, Top View













## 2.5 AC Timings

The following sections include illustrations and tables of timing diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 cm transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

### 2.5.1 Output Buffer Impedances

### 2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. Section 2.5.3 describes the clocking characteristics. Section 2.5.4 describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8112 device:

- $\overline{\text{PORESET}}$  and  $\overline{\text{TRST}}$  must be asserted externally for the duration of the power-up sequence. See Table 2-1 for timing.
- If possible, bring up the  $V_{\text{DD}}$  and  $V_{\text{DDH}}$







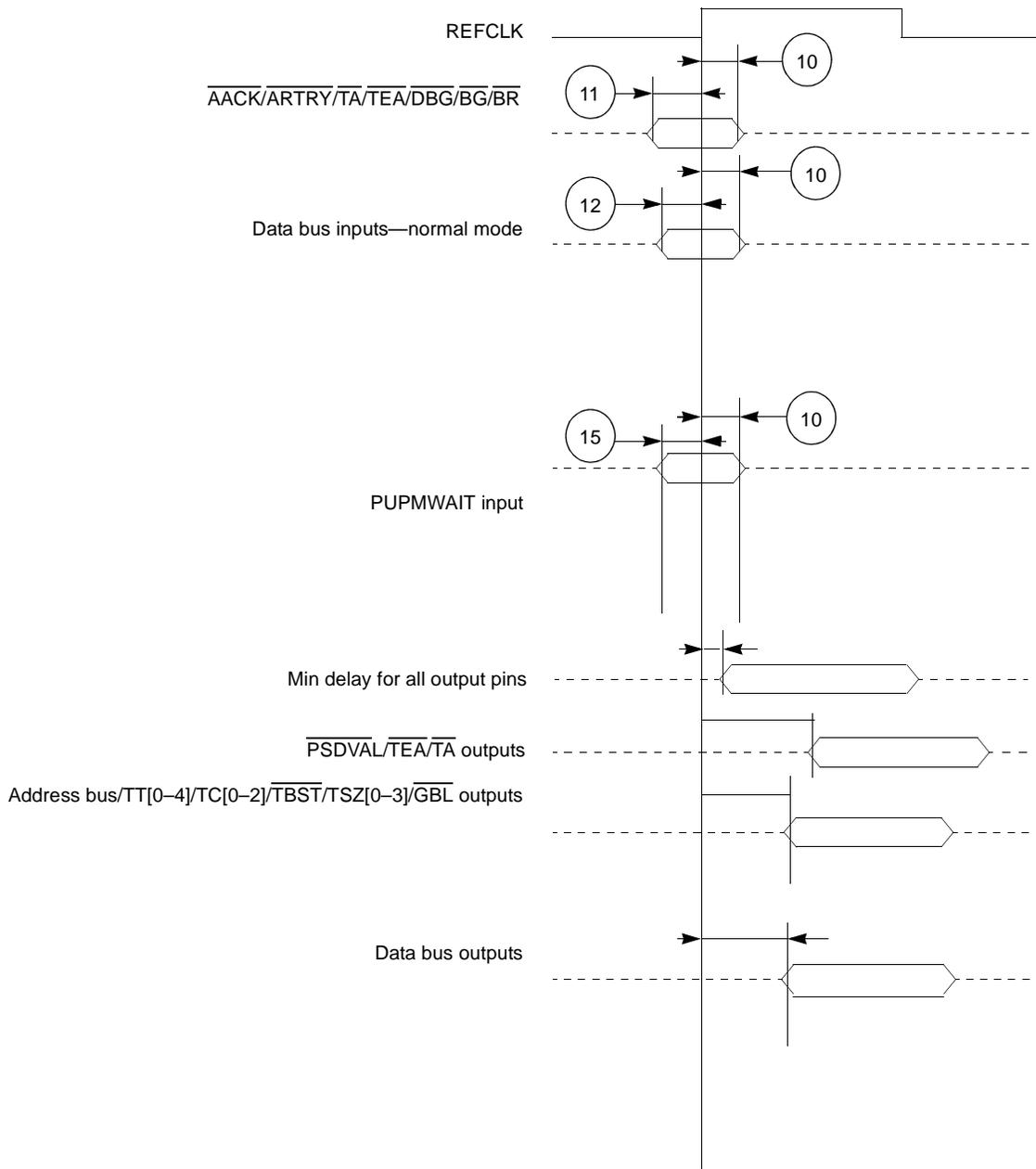


Figure 11. SIU Timing Diagram

Figure 14 shows DSI asynchronous read signals timing.

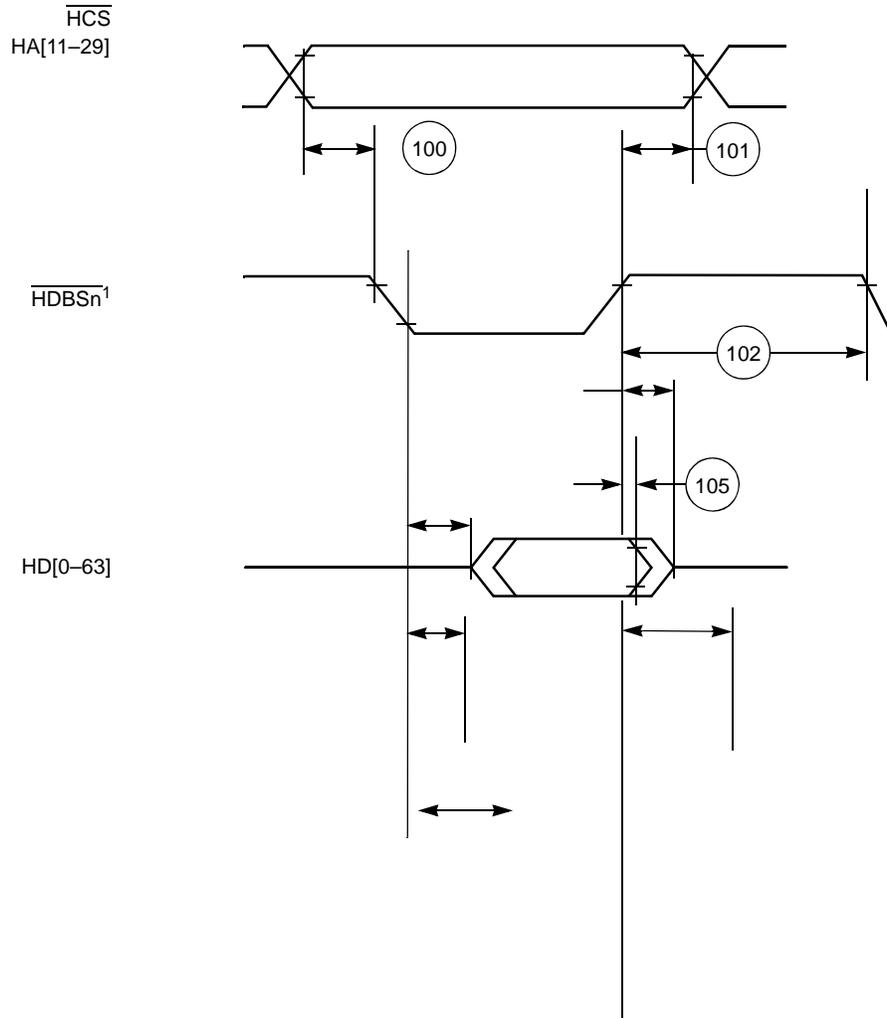


Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram











