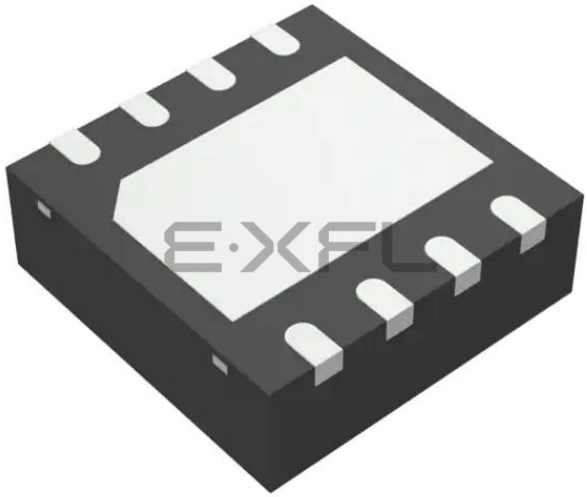

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f609-e-md

TABLE 2-4: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25, 116
81h	OPTION_REG	$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19, 116
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	25, 116
83h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18, 116
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	25, 116
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3(4)	TRISIO2	TRISIO1	TRISIO0	--11 1111	44, 116
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	25, 116
8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF(3)	0000 0000	20, 116
8Ch	PIE1	—	ADIE	CCP1IE	—	CMIE	—	TMR2IE	TMR1IE	-00- 0-00	21, 116
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	23, 116
8Fh	—	Unimplemented								—	—
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	41, 116
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Module Period Register								1111 1111	65, 116
93h	APFCON	—	—	—	T1GSEL	—	—	P1BSEL	P1ASEL	---0 --00	21, 116
94h	—	Unimplemented								—	—
95h	WPU(2)	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	46, 116
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	46, 116
97h	—	Unimplemented								—	—
98h	PMCON1(7)	—	—	—	—	—	WREN	WR	RD	---- -000	29
99h	PMCON2(7)	Program Memory Control Register 2 (not a physical register).								---- ----	—
9Ah	PMADRL(7)	PMADRL7	PMADRL6	PMADRL5	PMADRL4	PMADRL3	PMADRL2	PMADRL1	PMADRL0	0000 0000	28
9Bh	PMADRH(7)	—	—	—	—	—	PMADRH2	PMADRH1	PMADRH0	---- -000	28
9Ch	PMDATL(7)	PMDATL7	PMDATL6	PMDATL5	PMDATL4	PMDATL3	PMDATL2	PMDATL1	PMDATL0	0000 0000	28
9Dh	PMDATH(7)	—	—	Program Memory Data Register High Byte.						--00 0000	28
9Eh	ADRESL(5, 6)	Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result								xxxx xxxx	85, 117
9Fh	ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	45, 117

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: GP3 pull-up is enabled when MCLRE is '1' in the Configuration Word register.

3: $\overline{MCLR}$ and WDT Reset does not affect the previous value data latch. The GPIF bit will clear upon Reset but will set again if the mismatch exists.

4: TRISIO3 always reads as '1' since it is an input only pin.

5: Read only register.

6: PIC12F615/617/HV615 only.

7: PIC12F617 only.

3.0 FLASH PROGRAM MEMORY SELF READ/SELF WRITE CONTROL (FOR PIC12F617 ONLY)

The Flash program memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 3-1 to 3-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word which holds the 14-bit data for read/write, and the PMADRL and PMADRH registers form a two-byte word which holds the 13-bit address of the Flash location being accessed. These devices have 2K words of program Flash with an address range from 0000h to 07FFh.

The program memory allows single word read and a by four word write. A four word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the Flash program memory.

Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory, however, reads of the program memory are allowed.

When the Flash program memory Code Protection ($\overline{CP}$) bit in the Configuration Word register is enabled, the program memory is code-protected, and the device programmer (ICSP™) cannot access data or program memory.

3.1 PMADRH and PMADRL Registers

The PMADRH and PMADRL registers can address up to a maximum of 8K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADRH register and the Least Significant Byte (LSB) is written to the PMADRL register.

3.2 PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

PMCON2 is not a physical register. Reading PMCON2 will read all '0's. The PMCON2 register is used exclusively in the Flash memory write sequence.

REGISTER 5-3: ANSEL: ANALOG SELECT REGISTER (PIC12F609/HV609)

U-0	U-0	U-0	U-0	R/W-1	U-0	R/W-1	R/W-1
—	—	—	—	ANS3	—	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented**: Read as '0'

bit 3 **ANS3**: Analog Select Between Analog or Digital Function on Pin GP4
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

bit 2 **Unimplemented**: Read as '0'

bit 1 **ANS1:** Analog Select Between Analog or Digital Function on Pin GP1
1 = Analog input. Pin is assigned as analog input.(1)
0 = Digital I/O. Pin is assigned to port or special function.

bit 0 **ANS0:** Analog Select Between Analog or Digital Function on Pin GP0
0 = Digital I/O. Pin is assigned to port or special function.
1 = Analog input. Pin is assigned as analog input.(1)

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 5-4: ANSEL: ANALOG SELECT REGISTER (PIC12F615/617/HV615)

U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**: Read as '0'

bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits
000 = Fosc/2
001 = Fosc/8
010 = Fosc/32
x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)
100 = Fosc/4
101 = Fosc/16
110 = Fosc/64

bit 3-0 **ANS<3:0>**: Analog Select Between Analog or Digital Function on Pins GP4, GP2, GP1, GP0, respectively.
1 = Analog input. Pin is assigned as analog input(1).
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

6.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 6-1 is a block diagram of the Timer0 module.

6.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

6.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.

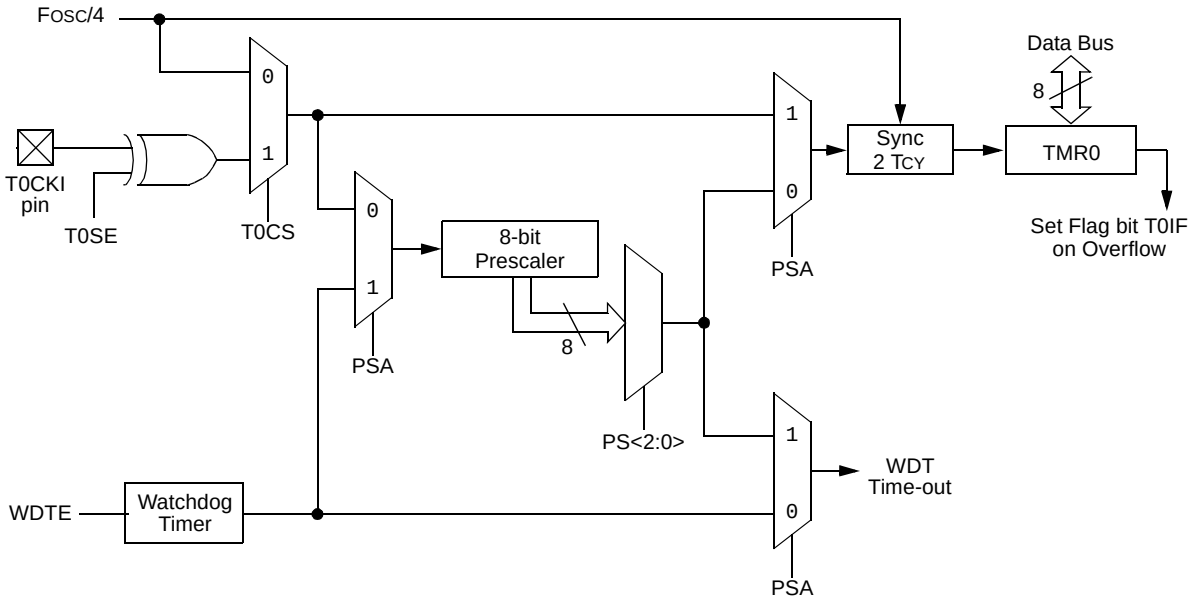
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

6.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the T0CKI pin. The incrementing edge is determined by the T0SE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

FIGURE 6-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

2: WDTE bit is in the Configuration Word register.

7.10 ECCP Special Event Trigger (PIC12F615/617/HV615 only)

If a ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 11.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)"**.

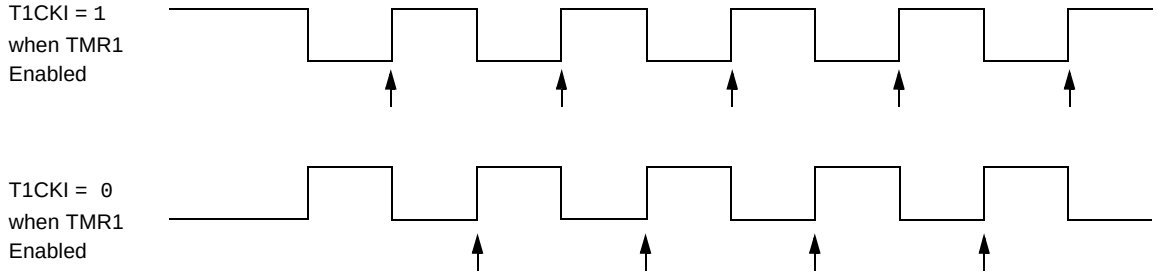
7.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 9.0 "Comparator Module"**.

FIGURE 7-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

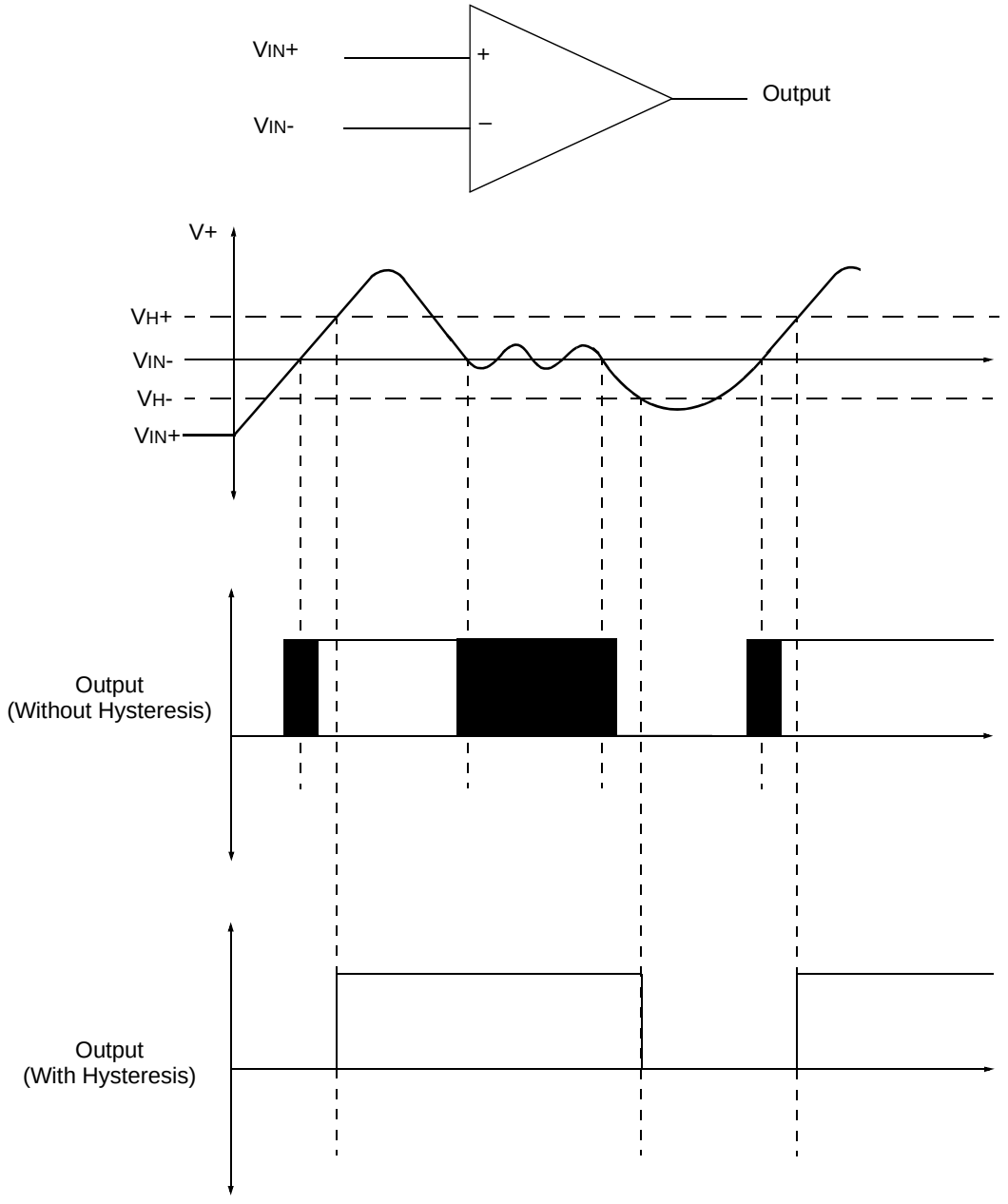
2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

9.11 Comparator Hysteresis

Each comparator has built-in hysteresis that is user enabled by setting the CMHYS bit of the CMCON1 register. The hysteresis feature can help filter noise and reduce multiple comparator output transitions when the output is changing state.

Figure 9-7 shows the relationship between the analog input levels and digital output of a comparator with and without hysteresis. The output of the comparator changes from a low state to a high state only when the analog voltage at VIN+ rises above the upper hysteresis threshold (VH+). The output of the comparator changes from a high state to a low state only when the analog voltage at VIN+ falls below the lower hysteresis threshold (VH-).

FIGURE 9-7: COMPARATOR HYSTERESIS



Note: The black areas of the comparator output represents the uncertainty due to input offsets and response time.

REGISTER 10-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 10-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 10-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

REGISTER 10-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

TABLE 10-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0(1)	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON	00-0 0000	00-0 0000
ANSEL	—	ADCS2(1)	ADCS1(1)	ADCS0(1)	ANS3	ANS2(1)	ANS1	ANS0	-000 1111	-000 1111
ADRESH(1,2)	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL(1,2)	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--x0 x000	--x0 x000
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	-00- 0-00	-00- 0-00
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

Note 1: For PIC12F615/617/HV615 only.

2: Read Only Register.

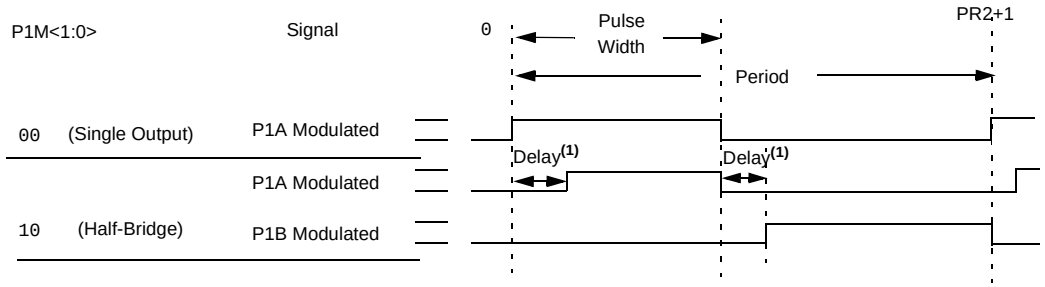
TABLE 11-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	0-00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	-00- 0-00	-00- 0-00
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture.

Note 1: For PIC12F615/617/HV615 only.

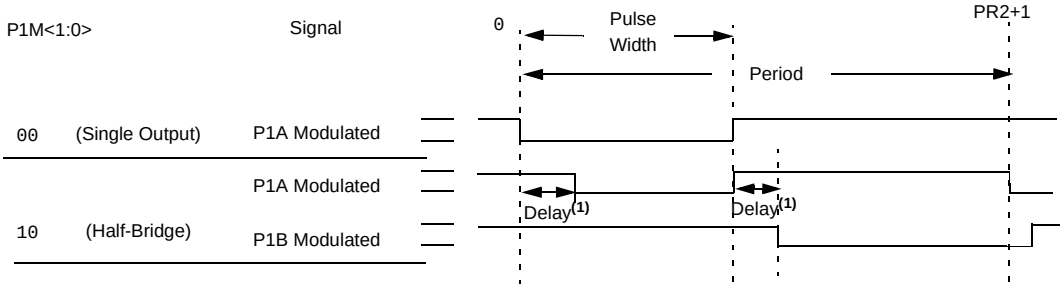
FIGURE 11-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)



Relationships:
- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 11.4.6 "Programmable Dead-Band Delay mode"**).

FIGURE 11-7: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)



Relationships:
- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 11.4.6 "Programmable Dead-Band Delay mode"**).

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1

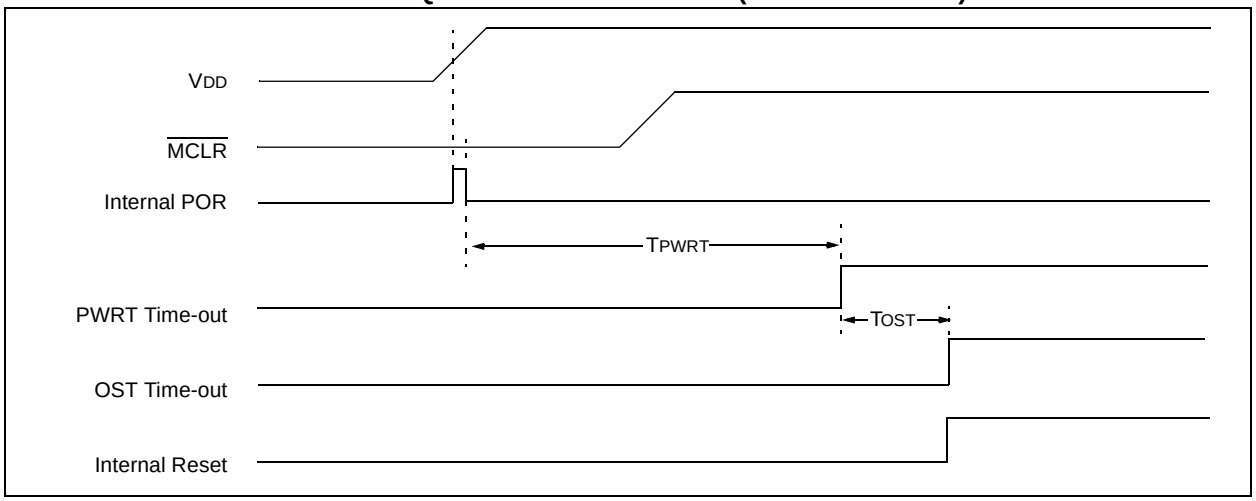


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 2

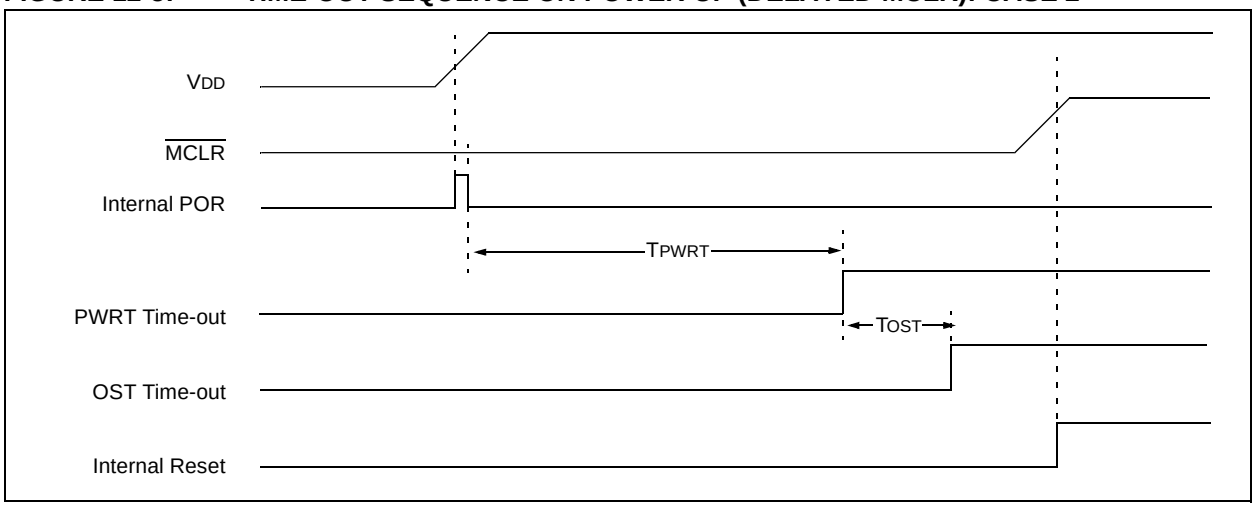
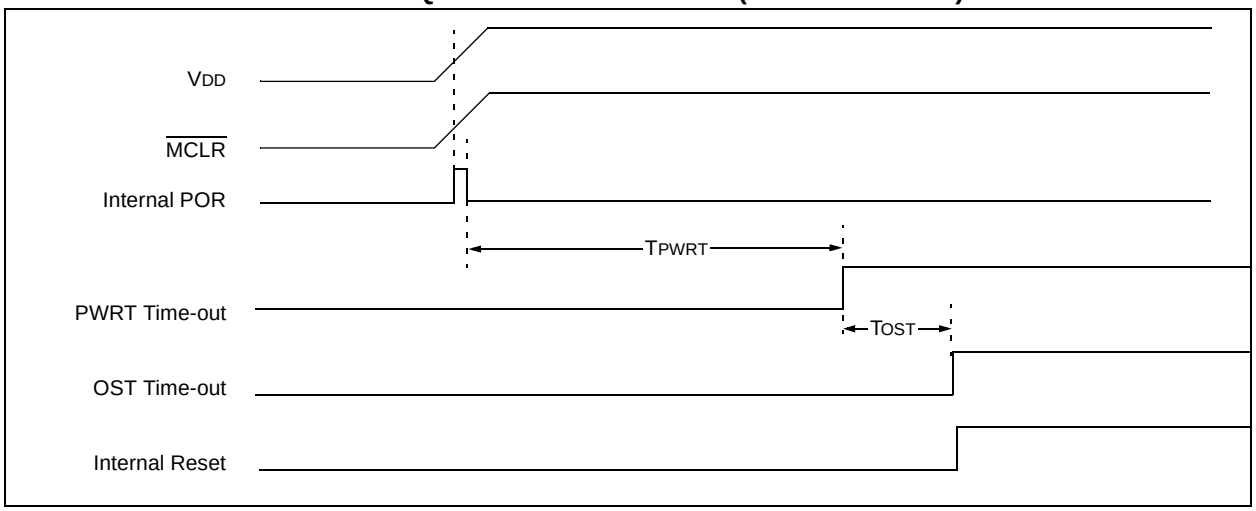


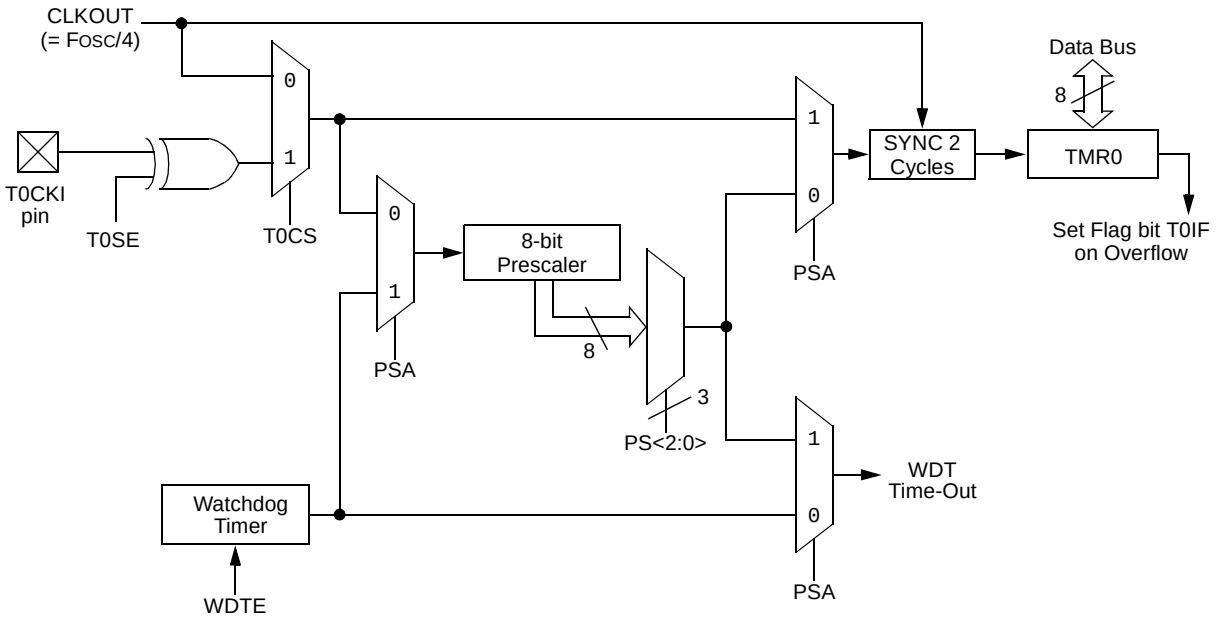
FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD)



12.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst-case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time out occurs.

FIGURE 12-2: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

TABLE 12-8: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

TABLE 12-9: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
OPTION_REG	$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
CONFIG	IOSCFS	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 12-1 for operation of all Configuration Word register bits.

15.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

15.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

15.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

15.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

15.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

16.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40° to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on $\overline{MCLR}$ with respect to Vss ..... -0.3V to +13.5V
Voltage on all other pins with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Total power dissipation(1) ..... 800 mW
Maximum current out of V_{SS} pin ..... 95 mA
Maximum current into V_{DD} pin ..... 95 mA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ± 20 mA
Output clamp current, I_{OK} (Vo < 0 or Vo >V_{DD}) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA
Maximum current sunk by GPIO ..... 90 mA
Maximum current sourced GPIO ..... 90 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(Vol \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

16.1 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VDD	**Supply Voltage**					
D001		PIC12F609/615/617	2.0	—	5.5	V	FOSC < = 4 MHz
D001		PIC12HV609/615	2.0	—	—(2)	V	FOSC < = 4 MHz
D001B		PIC12F609/615/617	2.0	—	5.5	V	FOSC < = 8 MHz
D001B		PIC12HV609/615	2.0	—	—(2)	V	FOSC < = 8 MHz
D001C		PIC12F609/615/617	3.0	—	5.5	V	FOSC < = 10 MHz
D001C		PIC12HV609/615	3.0	—	—(2)	V	FOSC < = 10 MHz
D001D		PIC12F609/615/617	4.5	—	5.5	V	FOSC < = 20 MHz
D001D		PIC12HV609/615	4.5	—	—(2)	V	FOSC < = 20 MHz
D002*	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	Device in Sleep mode
D003	VPOR	**VDD Start Voltage** to ensure internal Power-on Reset signal	—	VSS	—	V	See **Section 12.3.1 "Power-on Reset (POR)"** for details.
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 12.3.1 "Power-on Reset (POR)"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: User defined. Voltage across the shunt regulator should not exceed 5V.

16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O port:					
D030		with TTL buffer	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			Vss	—	0.15 VDD	V	2.0V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer	Vss	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
D032		$\overline{MCLR}$, OSC1 (RC mode)	Vss	—	0.2 VDD	V	**(NOTE 1)**
D033		OSC1 (XT and LP modes)	Vss	—	0.3	V	
D033A		OSC1 (HS mode)	Vss	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	VDD	V	2.0V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	2.0V ≤ VDD ≤ 5.5V
D042		$\overline{MCLR}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	**(NOTE 1)**
	IIL	**Input Leakage Current(2,3)**					
D060		I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D061		GP3/$\overline{MCLR}$(3,4)	—	± 0.7	± 5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070*	IPUR	**GPIO Weak Pull-up Current(5)**	50	250	400	µA	VDD = 5.0V, VPIN = VSS
	VOL	**Output Low Voltage**	—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
	VOH	**Output High Voltage**	VDD – 0.7	—	—	V	IOH = -2.5mA, VDD = 4.5V, -40°C to +125°C
D090		I/O ports(2)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: This specification applies to GP3/$\overline{MCLR}$ configured as GP3 with the internal weak pull-up disabled.

5: This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/$\overline{MCLR}$. When GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ reset pin, the weak pull-up is always enabled.

6: Applies to PIC12F617 only.

17.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

FIGURE 17-1: PIC12F609/615/617 IDD LP (32 kHz) vs. VDD

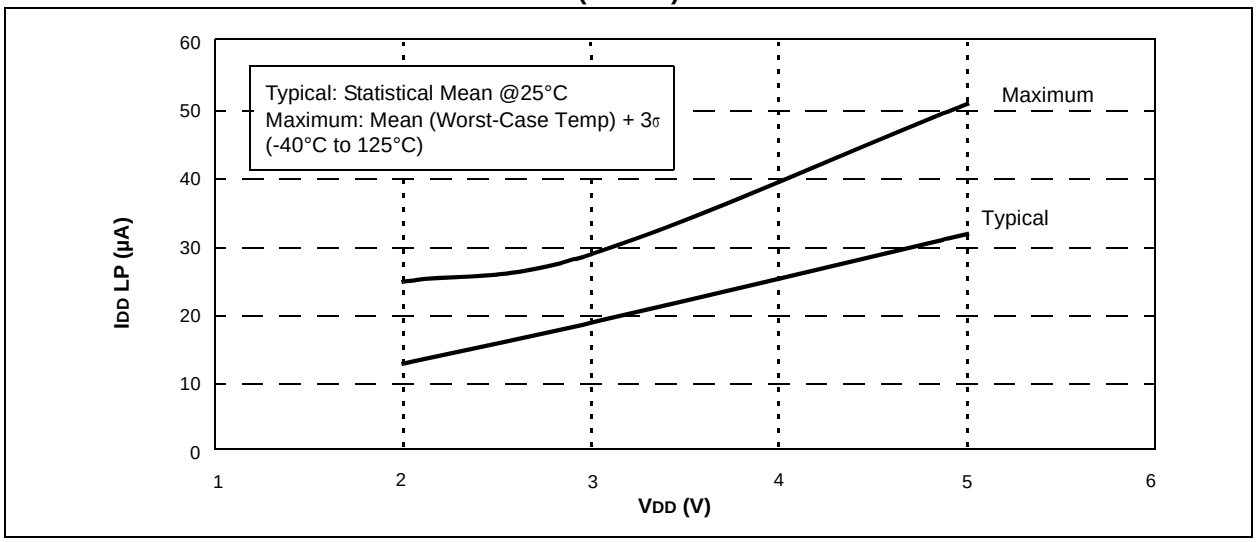


FIGURE 17-2: PIC12F609/615/617 IDD EC (1 MHz) vs. VDD

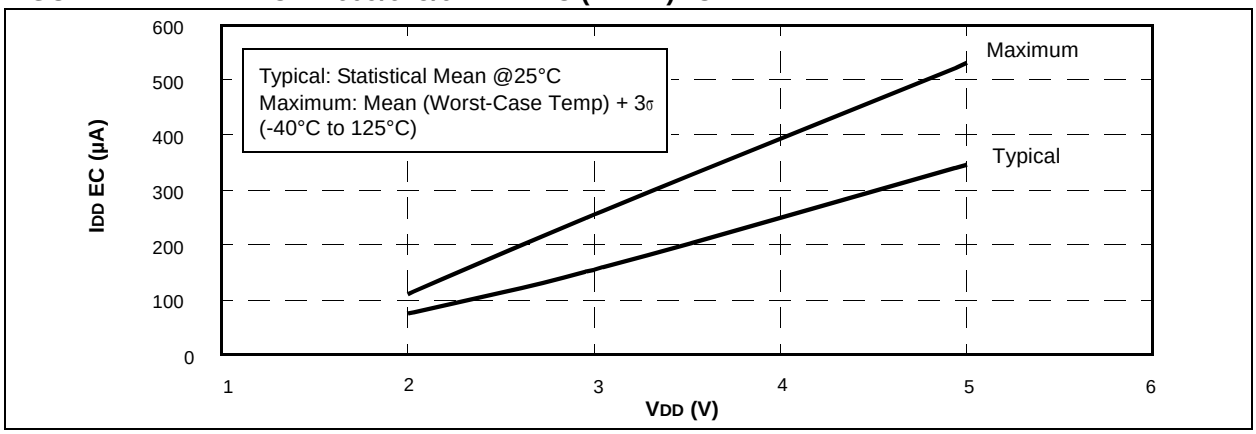


FIGURE 17-12: PIC12F609/615/617 IPD WDT vs. VDD

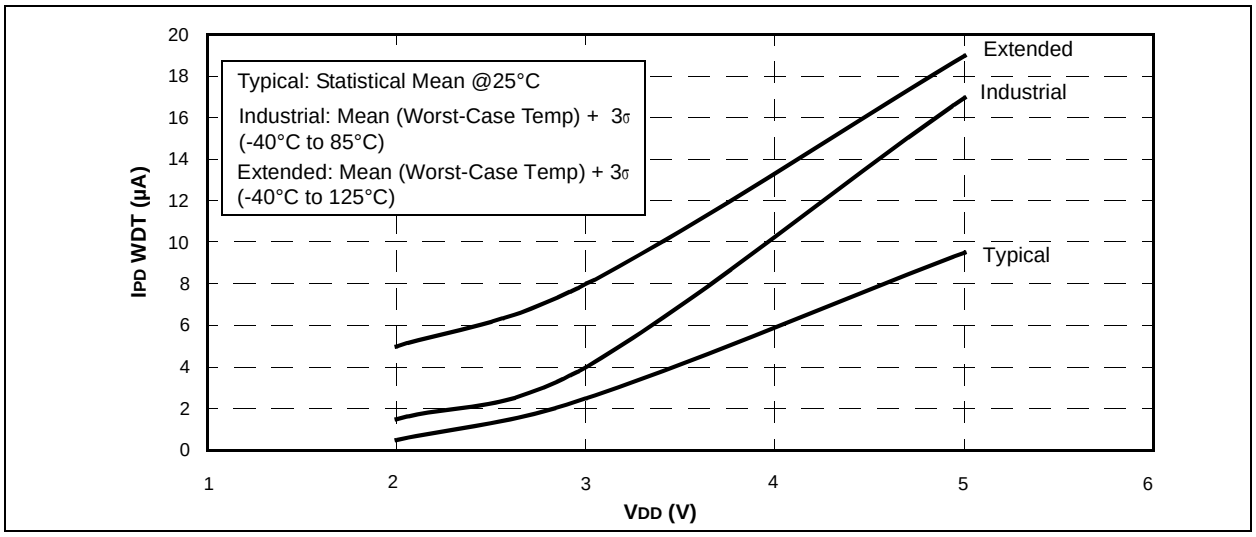


FIGURE 17-13: PIC12F609/615/617 IPD BOR vs. VDD

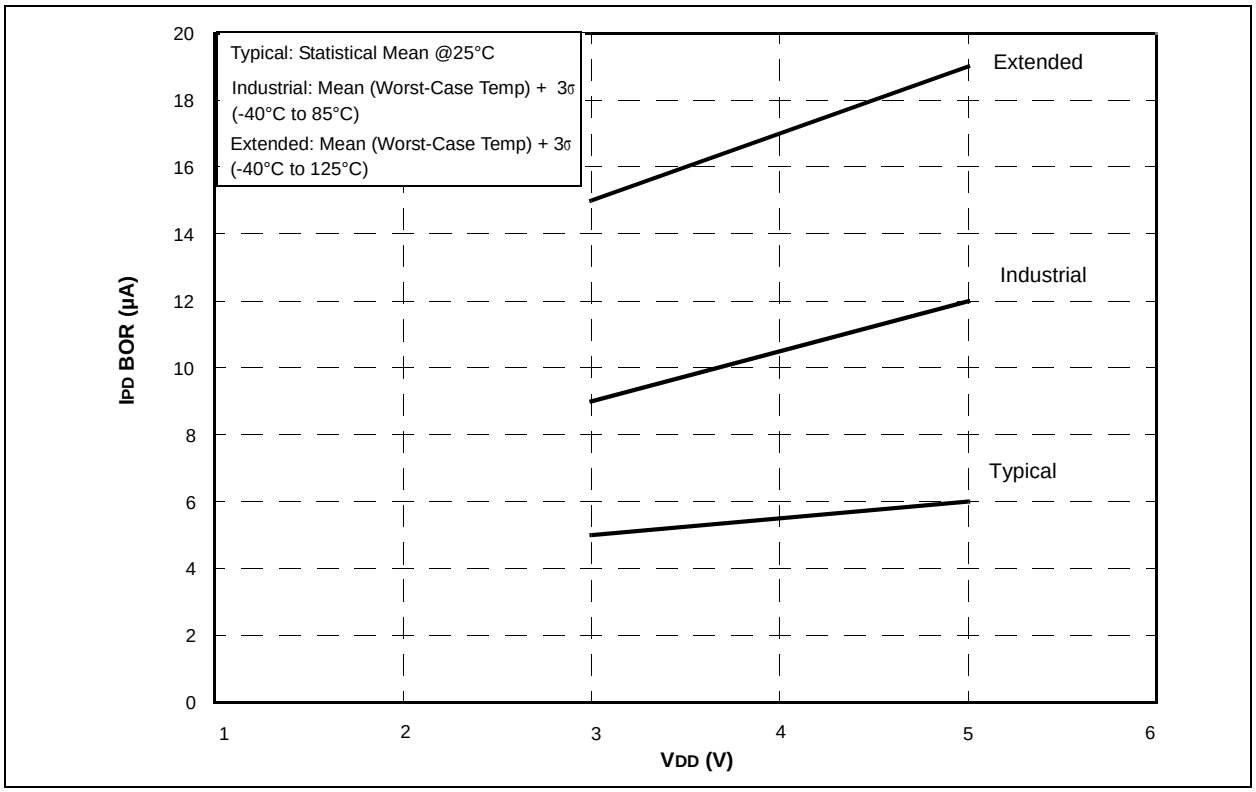


FIGURE 17-35: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

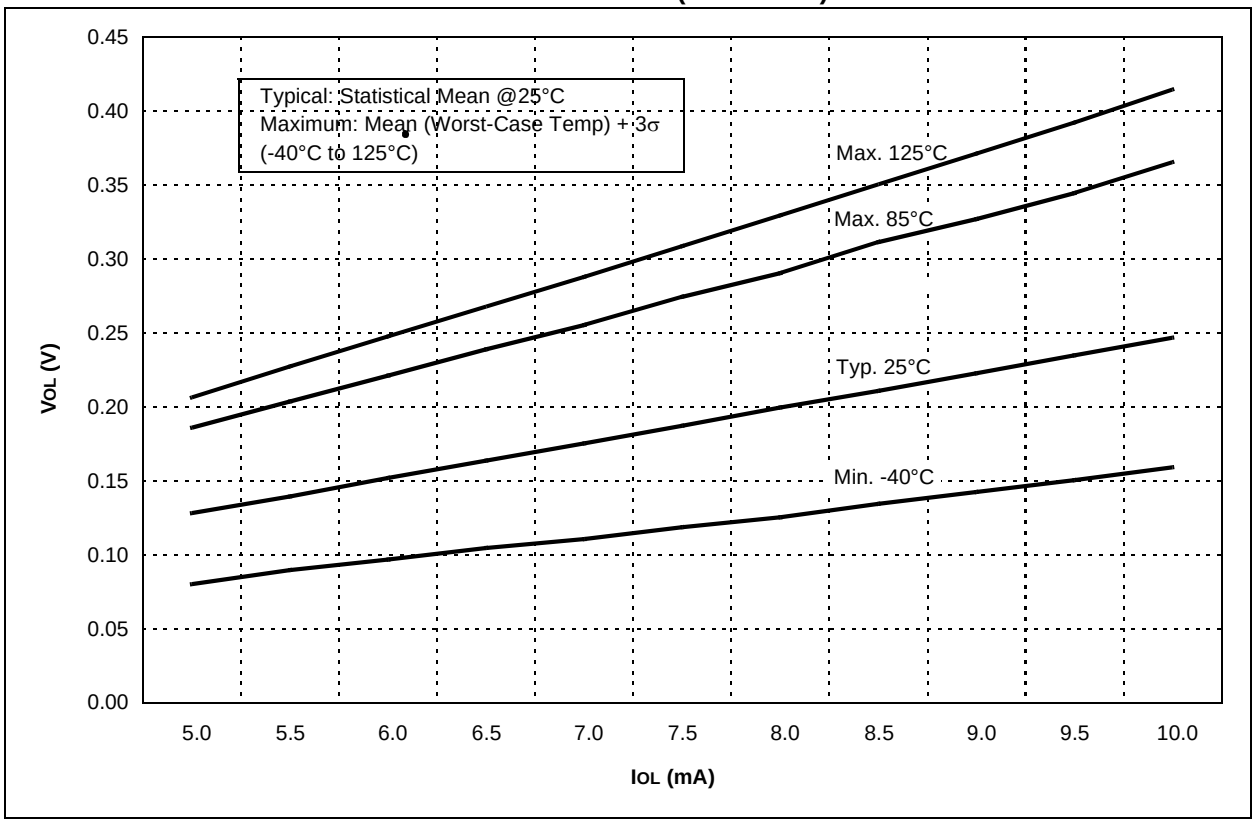
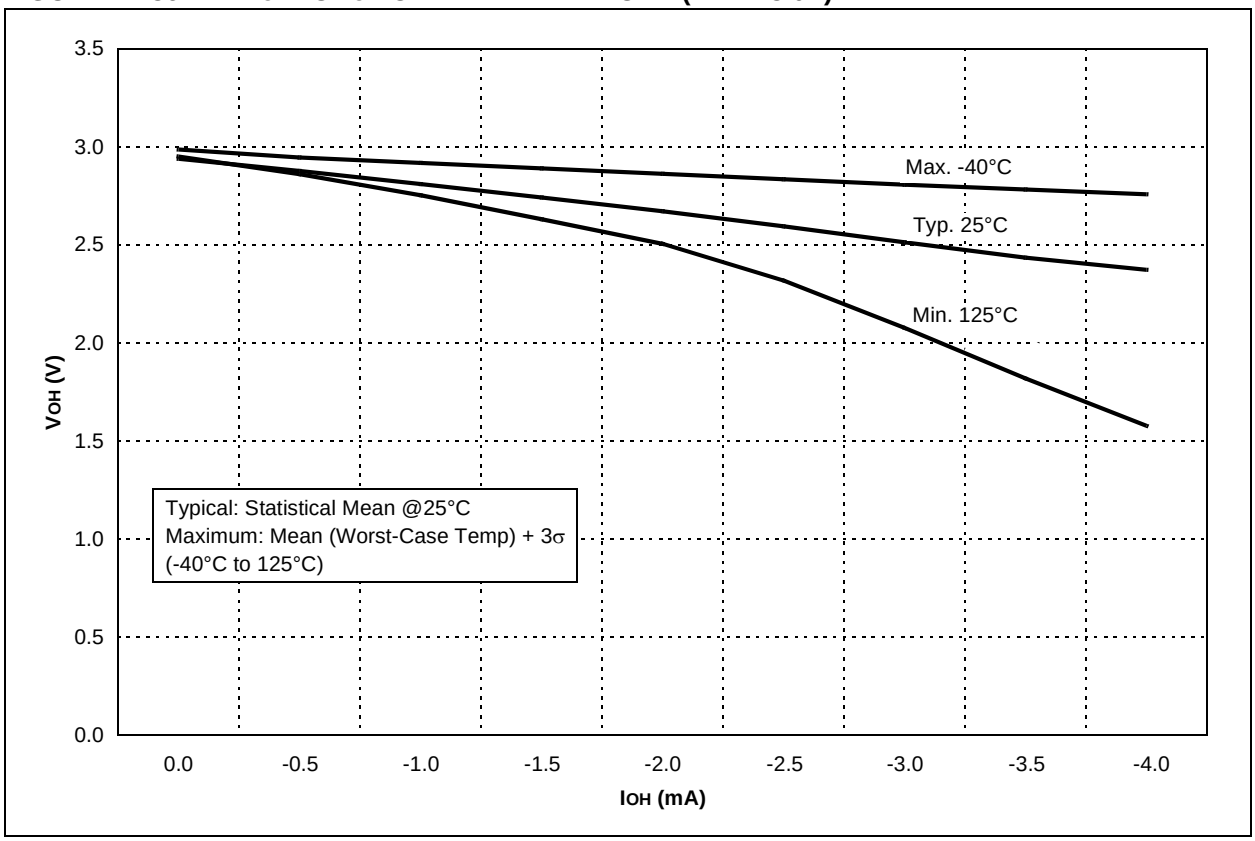


FIGURE 17-36: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)



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