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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f609-e-sn



MICROCHIP PIC12F609/615/617/12HV609/615

8-Pin Flash-Based, 8-Bit CMOS Microcontrollers

High-Performance RISC CPU:

- Only 35 Instructions to Learn:
 - All single-cycle instructions except branches
- Operating Speed:
 - DC – 20 MHz oscillator/clock input
 - DC – 200 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$, typical
 - Software selectable frequency: 4 MHz or 8 MHz
- Power-Saving Sleep mode
- Voltage Range:
 - PIC12F609/615/617: 2.0V to 5.5V
 - PIC12HV609/615: 2.0V to user defined maximum (**see note**)
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT) with independent Oscillator for Reliable Operation
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High Endurance Flash:
 - 100,000 write Flash endurance
 - Flash retention: > 40 years
- Self Read/ Write Program Memory (PIC12F617 only)

Low-Power Features:

- Standby Current:
 - 50 nA @ 2.0V, typical
- Operating Current:
 - 11 μ A @ 32 kHz, 2.0V, typical
 - 260 μ A @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
 - 1 μ A @ 2.0V, typical

Note: Voltage across the shunt regulator should not exceed 5V.

Peripheral Features:

- Shunt Voltage Regulator (PIC12HV609/615 only):
 - 5 volt regulation
 - 4 mA to 50 mA shunt range
- 5 I/O Pins and 1 Input Only
- High Current Source/Sink for Direct LED Drive
 - Interrupt-on-pin change or pins
 - Individually programmable weak pull-ups
- Analog Comparator module with:
 - One analog comparator
 - Programmable on-chip voltage reference (CVREF) module (% of VDD)
 - Comparator inputs and output externally accessible
 - Built-In Hysteresis (software selectable)
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Timer1 Gate (count enable)
 - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
 - Option to use system clock as Timer1
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC12F615/617/HV615 ONLY:

- Enhanced Capture, Compare, PWM module:
 - 16-bit Capture, max. resolution 12.5 ns
 - Compare, max. resolution 200 ns
 - 10-bit PWM with 1 or 2 output channels, 1 output channel programmable “dead time,” max. frequency 20 kHz, auto-shutdown
- A/D Converter:
 - 10-bit resolution and 4 channels, samples internal voltage references
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler

PIC12F609/615/617/12HV609/615

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PIC12F609/615/617/12HV609/615

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F609/615/617/12HV609/615 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) for the PIC12F609/615/12HV609/615 is physically implemented. For the PIC12F617, the first 2K x 14 (0000h-07FFh) is physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 1K x 14 space for PIC12F609/615/12HV609/615 devices, and within the first 2K x 14 space for the PIC12F617 device. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F609/615/12HV609/615

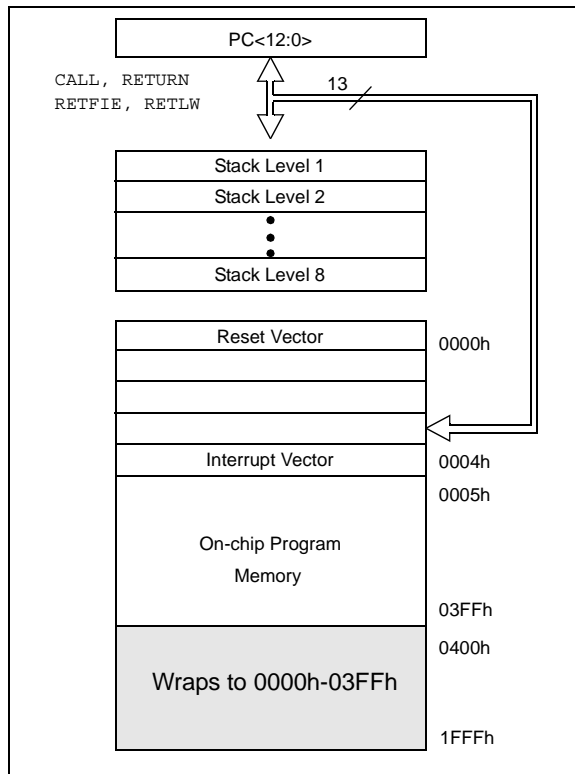
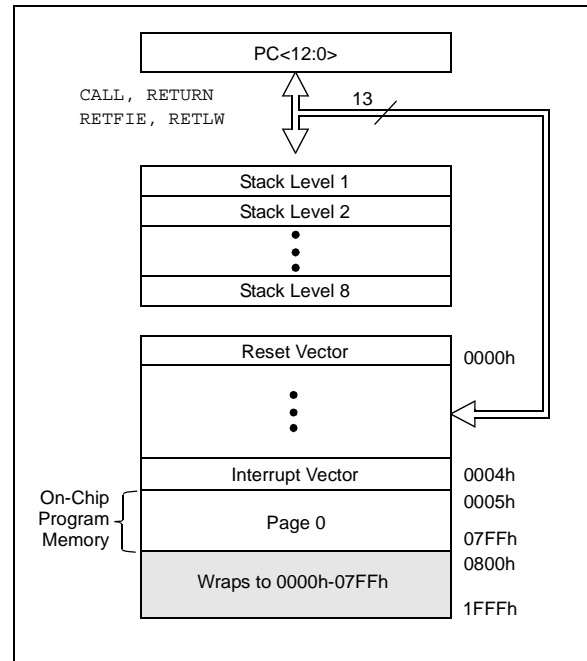


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F617



2.2 Data Memory Organization

The data memory (see Figure 2-3) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 40h-7Fh in Bank 0 are General Purpose Registers, implemented as static RAM. For the PIC12F617, the register locations 20h-7Fh in Bank 0 and A0h-EFh in Bank 1 are general purpose registers implemented as Static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. The RP0 bit of the STATUS register is the bank select bit.

RP0

- 0 → Bank 0 is selected
- 1 → Bank 1 is selected

Note: The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's.

PIC12F609/615/617/12HV609/615

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE	PEIE	TOIE	INTE	GPIE	T0IF	INTF	GPIF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
- bit 5 **TOIE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt
- bit 4 **INTE:** GP2/INT External Interrupt Enable bit
1 = Enables the GP2/INT external interrupt
0 = Disables the GP2/INT external interrupt
- bit 3 **GPIE:** GPIO Change Interrupt Enable bit⁽¹⁾
1 = Enables the GPIO change interrupt
0 = Disables the GPIO change interrupt
- bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit⁽²⁾
1 = Timer0 register has overflowed (must be cleared in software)
0 = Timer0 register did not overflow
- bit 1 **INTF:** GP2/INT External Interrupt Flag bit
1 = The GP2/INT external interrupt occurred (must be cleared in software)
0 = The GP2/INT external interrupt did not occur
- bit 0 **GPIF:** GPIO Change Interrupt Flag bit
1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software)
0 = None of the GPIO <5:0> pins have changed state

Note 1: IOC register must also be enabled.

2: T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.

PIC12F609/615/617/12HV609/615

2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Brown-out Reset ($\overline{\text{BOR}}$)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the software enable of the $\overline{\text{BOR}}$.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0 ⁽¹⁾
—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{\text{POR}}$:** Power-on Reset Status bit

1 = No Power-on Reset occurred

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{\text{BOR}}$:** Brown-out Reset Status bit

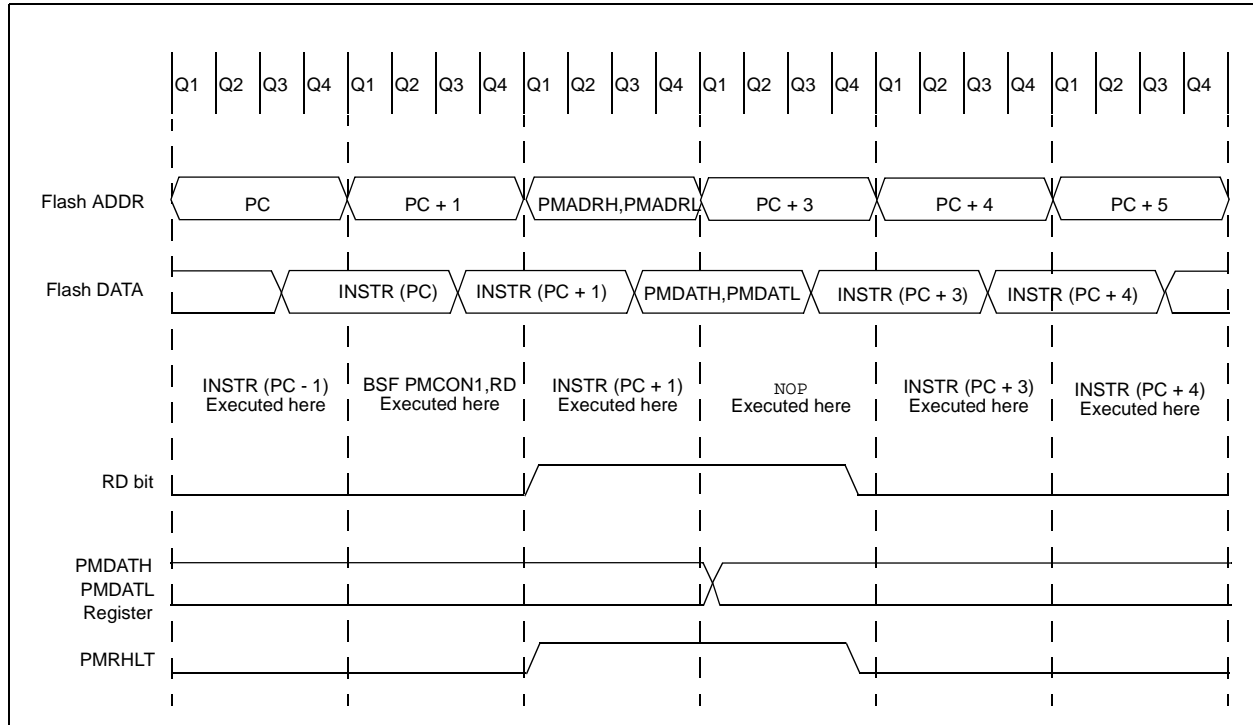
1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: Reads as '0' if Brown-out Reset is disabled.

PIC12F609/615/617/12HV609/615

FIGURE 3-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION



PIC12F609/615/617/12HV609/615

NOTES:

PIC12F609/615/617/12HV609/615

4.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 4-1).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency

01110 =

•

•

•

00001 =

00000 = Oscillator module is running at the calibrated frequency.

11111 =

•

•

•

10000 = Minimum frequency

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	IOSCFS	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.

PIC12F609/615/617/12HV609/615

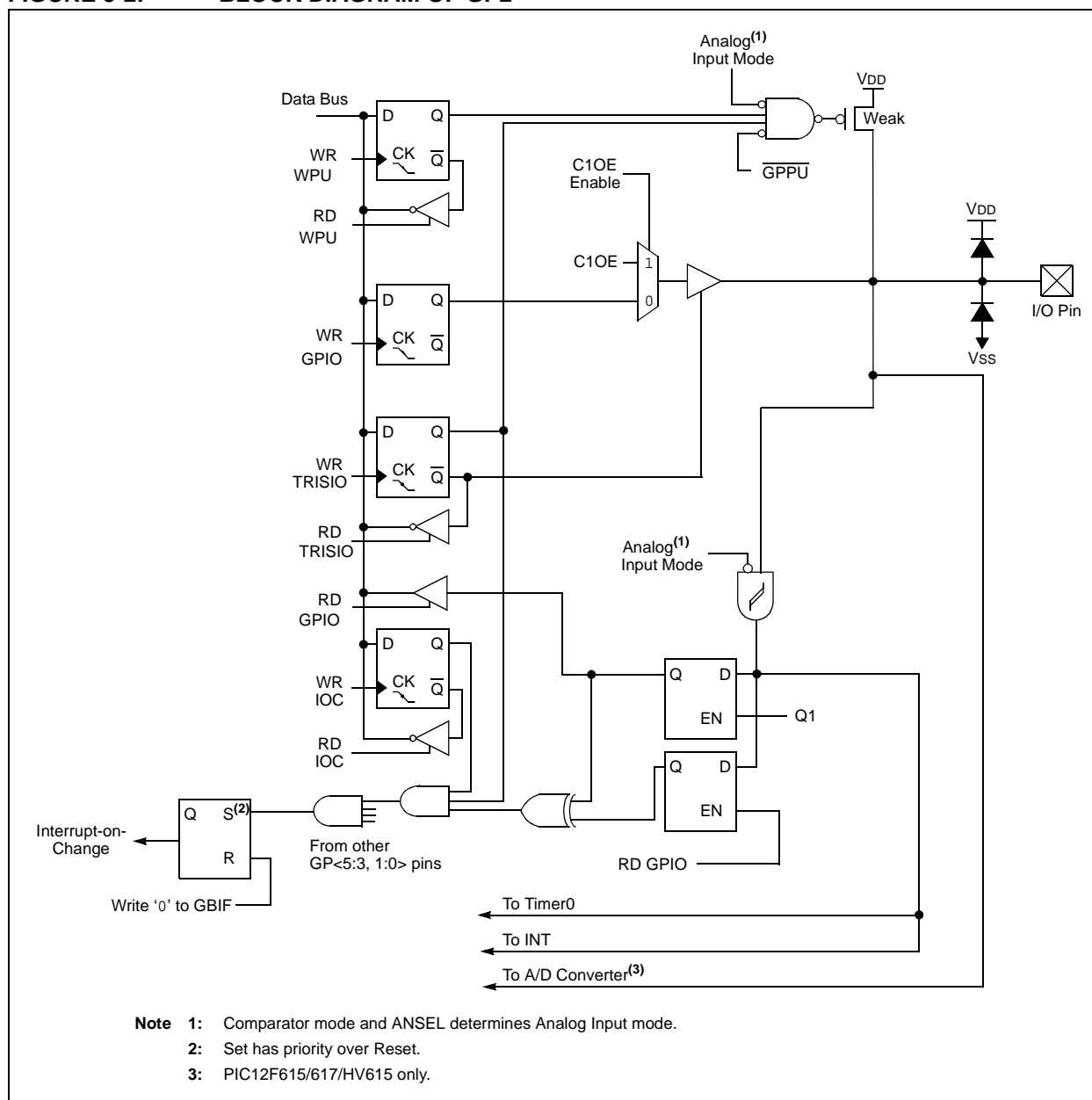
5.2.4.3 GP2/AN2⁽¹⁾/T0CKI/INT/COUT/ CCP1⁽¹⁾/P1A⁽¹⁾

Note 1: PIC12F615/617/HV615 only.

Figure 5-2 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC⁽¹⁾
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from Comparator
- a Capture input/Compare input/PWM output⁽¹⁾
- a PWM output⁽¹⁾

FIGURE 5-2: BLOCK DIAGRAM OF GP2



9.8 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See **Section 7.0 “Timer1 Module with Gate Control”** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

9.9 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 7-1) for more information.

REGISTER 9-2: CMCON1: COMPARATOR CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **T1ACS:** Timer1 Alternate Clock Select bit

1 = Timer 1 Clock Source is System Clock (Fosc)

0 = Timer 1 Clock Source is Instruction Clock (Fosc/4)

bit 3 **CMHYS:** Comparator Hysteresis Select bit

1 = Comparator Hysteresis enabled

0 = Comparator Hysteresis disabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit⁽¹⁾

1 = Timer 1 Gate Source is $\overline{T1G}$ pin (pin should be configured as digital input)

0 = Timer 1 Gate Source is comparator output

bit 0 **CMSYNC:** Comparator Output Synchronization bit⁽²⁾

1 = Output is synchronized with falling edge of Timer1 clock

0 = Output is asynchronous

Note 1: Refer to **Section 7.6 “Timer1 Gate”**.

2: Refer to Figure 9-2.

PIC12F609/615/617/12HV609/615

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0–00 0000	0–00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIE1	—	ADIE ⁽¹⁾	CCP1IE ⁽¹⁾	—	CMIE	—	TMR2IE ⁽¹⁾	TMR1IE	–00– 0–00	–00– 0–00
PIR1	—	ADIF ⁽¹⁾	CCP1IF ⁽¹⁾	—	CMIF	—	TMR2IF ⁽¹⁾	TMR1IF	–00– 0–00	–00– 0–00
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR2	Timer2 Module Register								0000 0000	0000 0000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Compare.

Note 1: For PIC12F615/617/HV615 only.

PIC12F609/615/617/12HV609/615

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1

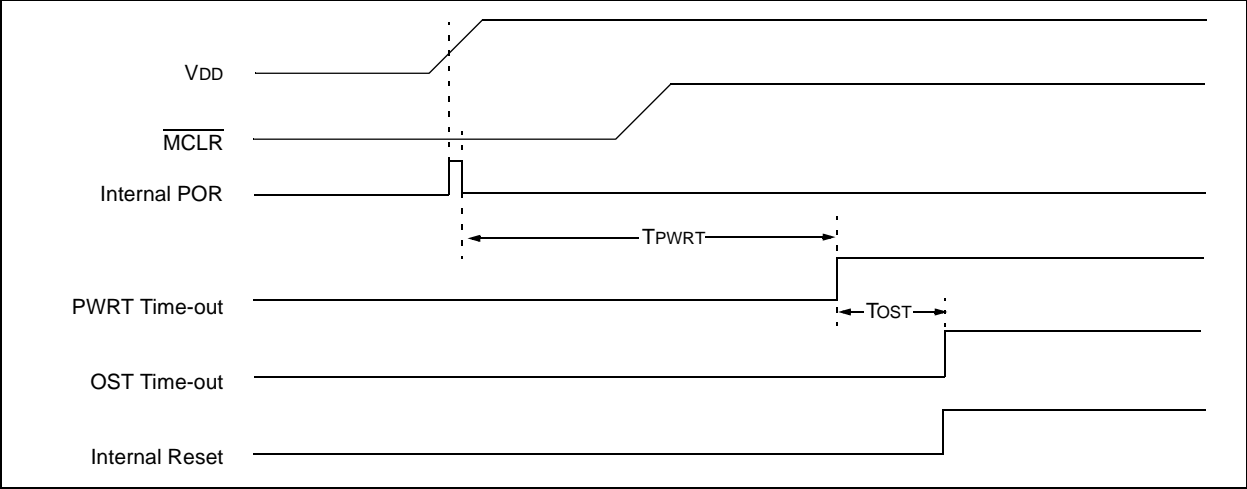


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 2

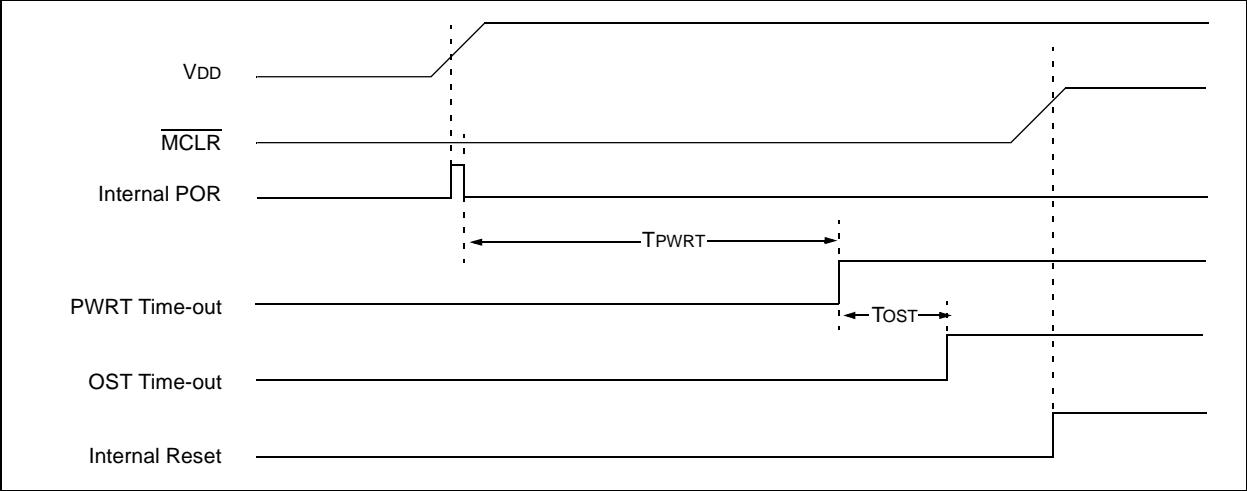
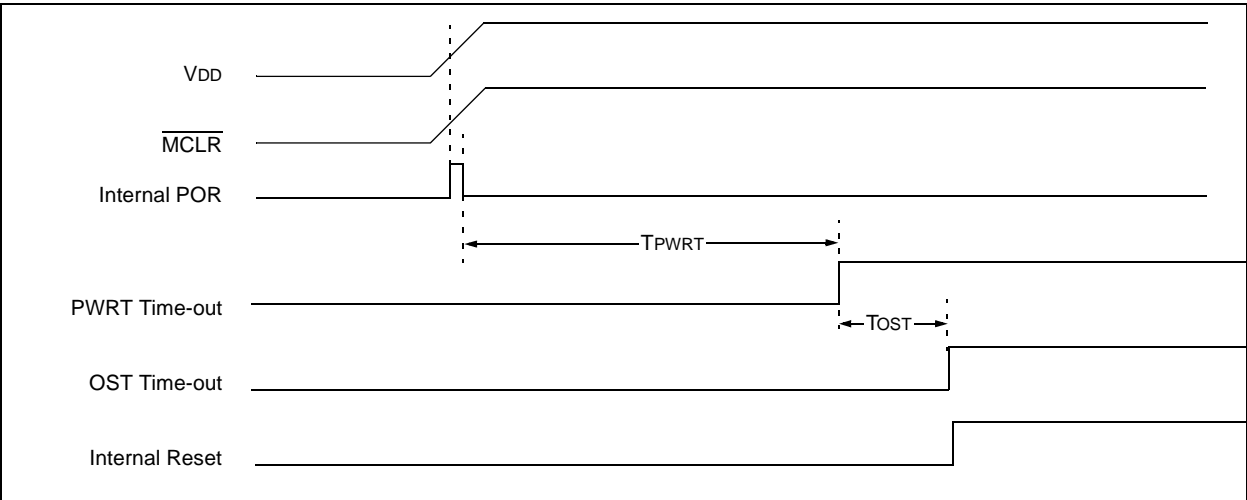
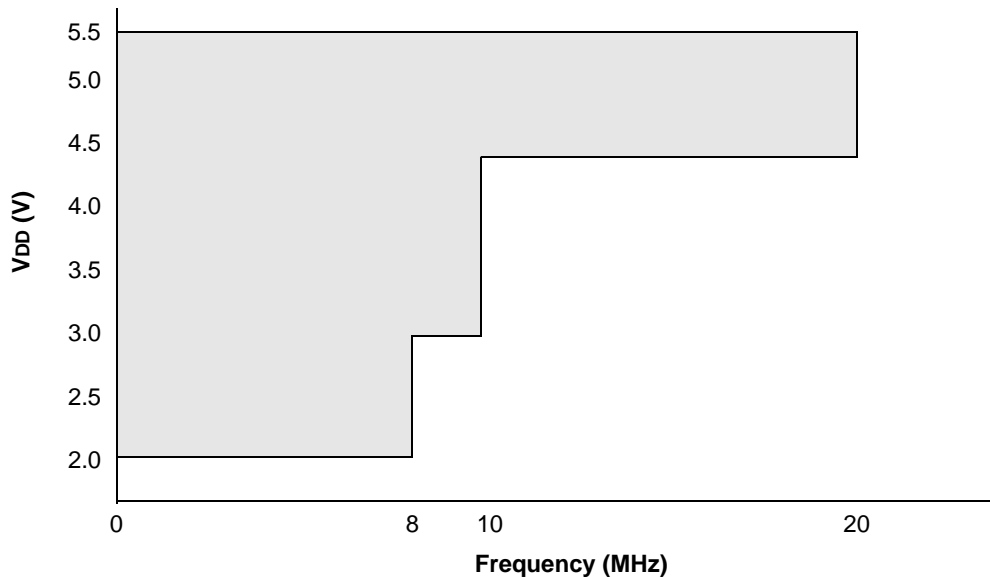


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD)



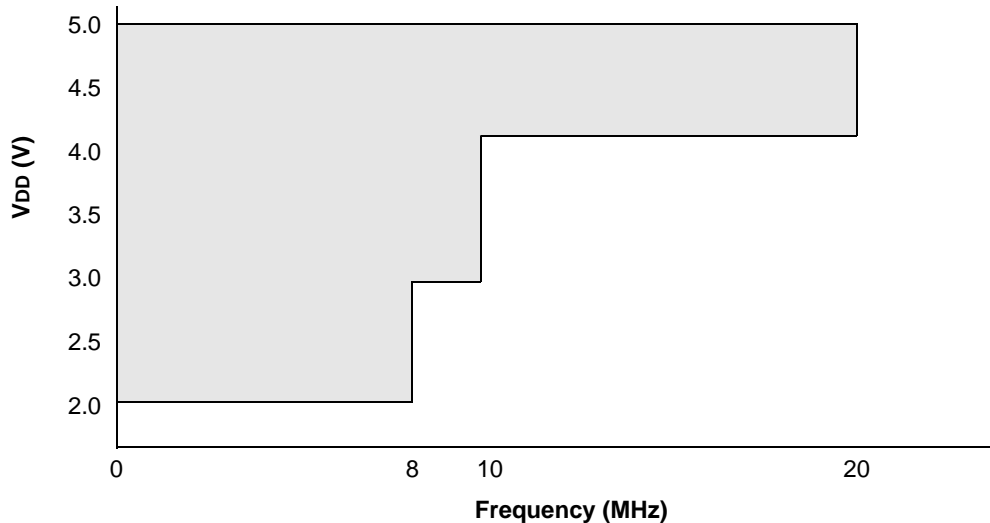
PIC12F609/615/617/12HV609/615

FIGURE 16-1: PIC12F609/615/617 VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 16-2: PIC12HV609/615 VOLTAGE-FREQUENCY GRAPH, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

PIC12F609/615/617/12HV609/615

16.11 AC Characteristics: PIC12F609/615/617/12HV609/615 (Industrial, Extended)

FIGURE 16-4: CLOCK TIMING

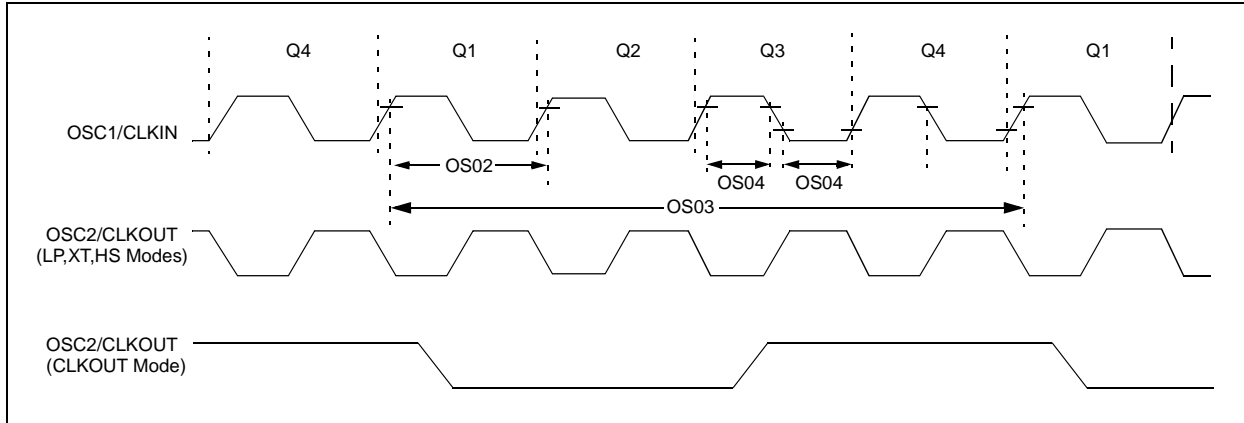


TABLE 16-1: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS01	FOSC	External CLKIN Frequency ⁽¹⁾	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency ⁽¹⁾	—	32.768	—	kHz	LP Oscillator mode
OS02	TOSC	External CLKIN Period ⁽¹⁾	0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
		Oscillator Period ⁽¹⁾	—	30.5	—	μs	LP Oscillator mode
OS03	Tcy	Instruction Cycle Time ⁽¹⁾	250	—	∞	ns	XT Oscillator mode
			50	—	∞	ns	HS Oscillator mode
			50	—	∞	ns	EC Oscillator mode
			50	—	∞	ns	EC Oscillator mode
		Oscillator Period ⁽¹⁾	—	30.5	—	μs	LP Oscillator mode
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
			250	—	—	ns	RC Oscillator mode
		Oscillator Period ⁽¹⁾	—	30.5	—	μs	LP Oscillator mode
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	200	Tcy	DC	ns	Tcy = 4/FOSC
			200	Tcy	DC	ns	Tcy = 4/FOSC
			200	Tcy	DC	ns	Tcy = 4/FOSC
			200	Tcy	DC	ns	Tcy = 4/FOSC
		Oscillator Period ⁽¹⁾	—	30.5	—	μs	LP Oscillator mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

PIC12F609/615/617/12HV609/615

FIGURE 16-5: CLKOUT AND I/O TIMING

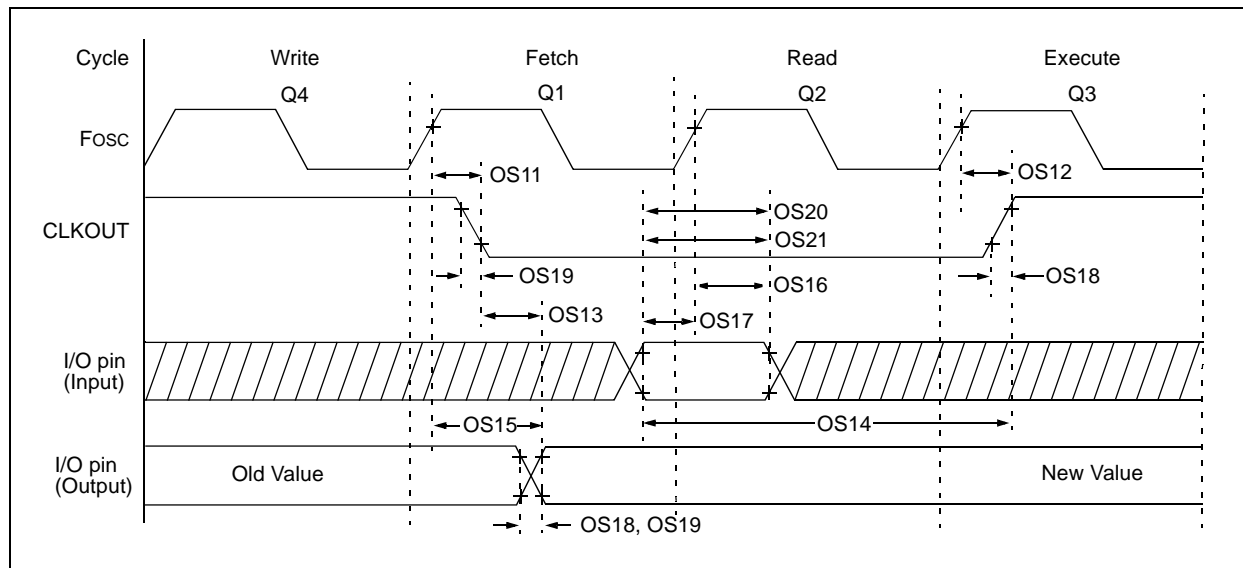


TABLE 16-3: CLKOUT AND I/O TIMING PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS11	TosH2ckL	Fosc↑ to CLKOUT↓ ⁽¹⁾	—	—	70	ns	VDD = 5.0V
OS12	TosH2ckH	Fosc↑ to CLKOUT↑ ⁽¹⁾	—	—	72	ns	VDD = 5.0V
OS13	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾	—	—	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT↑ ⁽¹⁾	Tosc + 200 ns	—	—	ns	
OS15	TosH2ioV	Fosc↑ (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 5.0V
OS16	TosH2ioI	Fosc↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 5.0V
OS17	TioV2osH	Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TioR	Port output rise time ⁽²⁾	—	15 40	72 32	ns	VDD = 2.0V VDD = 5.0V
OS19	TioF	Port output fall time ⁽²⁾	—	28 15	55 30	ns	VDD = 2.0V VDD = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TRAP	GPIO interrupt-on-change new input level time	TCY	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x TOSC.

2: Includes OSC2 in CLKOUT mode.

PIC12F609/615/617/12HV609/615

FIGURE 17-10: PIC12F609/615/617 IPD BASE vs. VDD

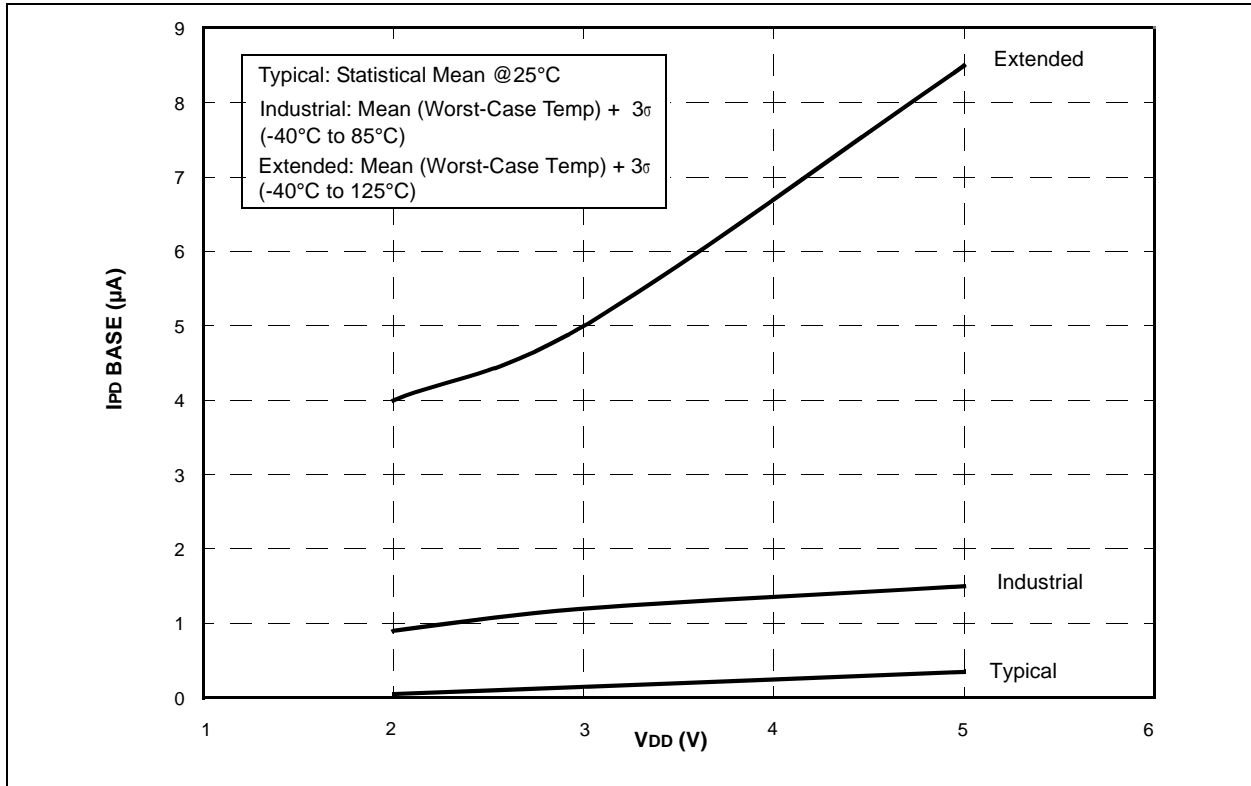
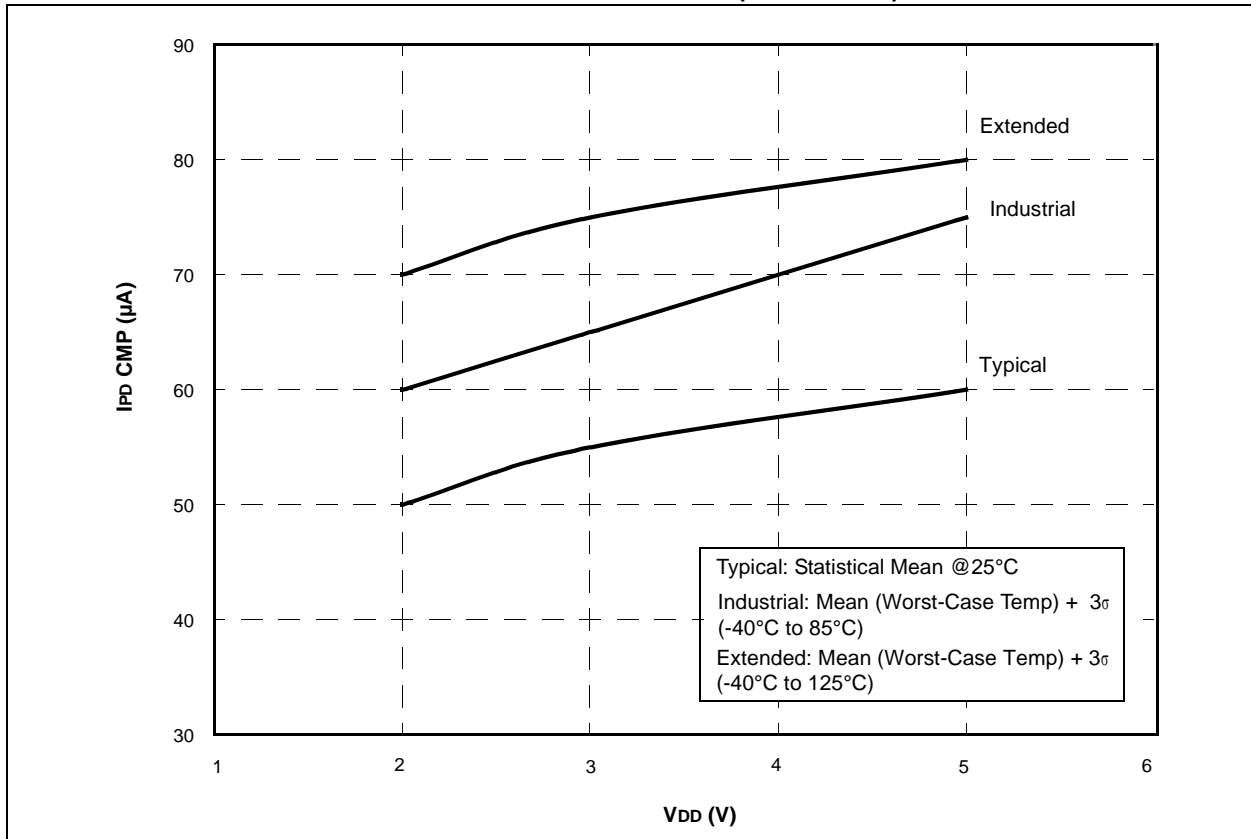


FIGURE 17-11: PIC12F609/615/617 IPD COMPARATOR (SINGLE ON) vs. VDD



PIC12F609/615/617/12HV609/615

FIGURE 17-41: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

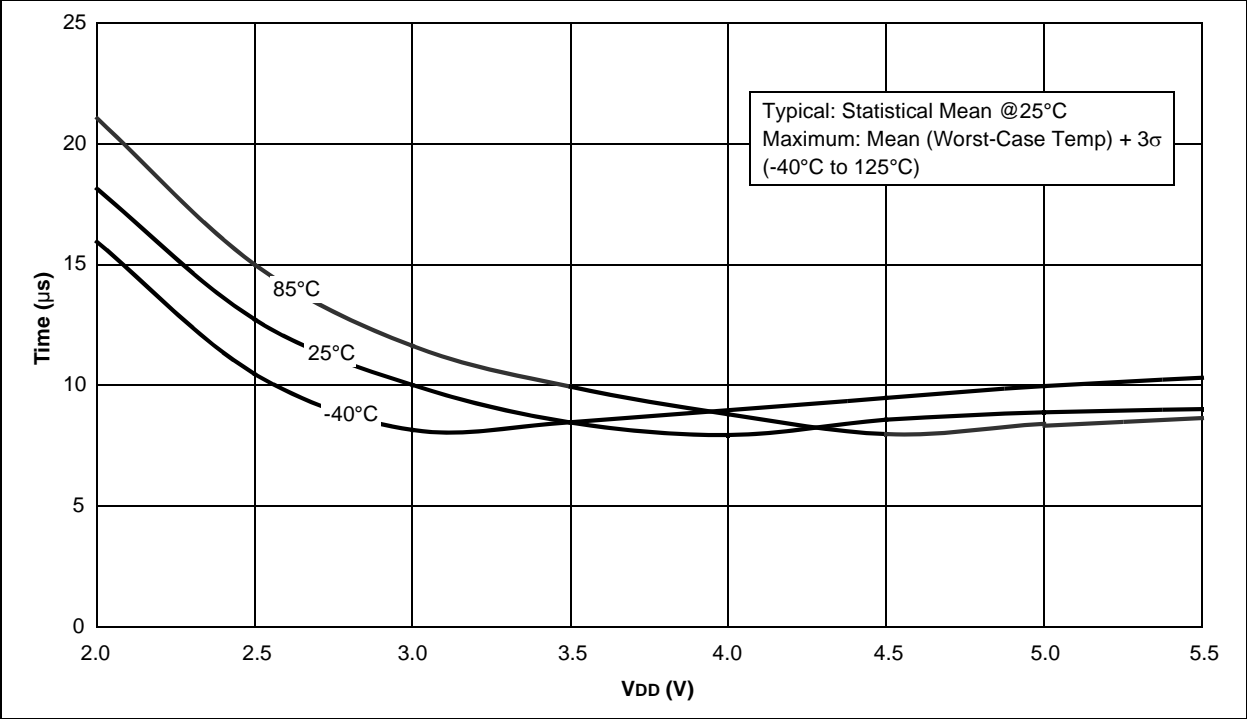
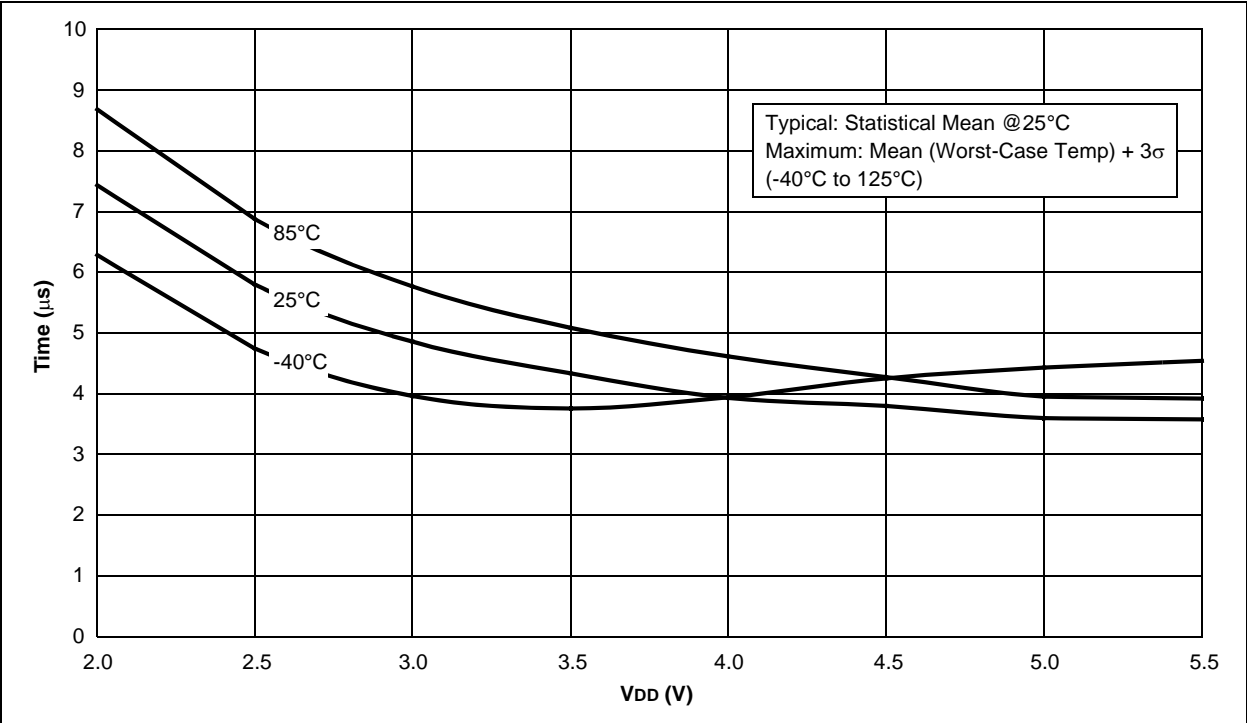


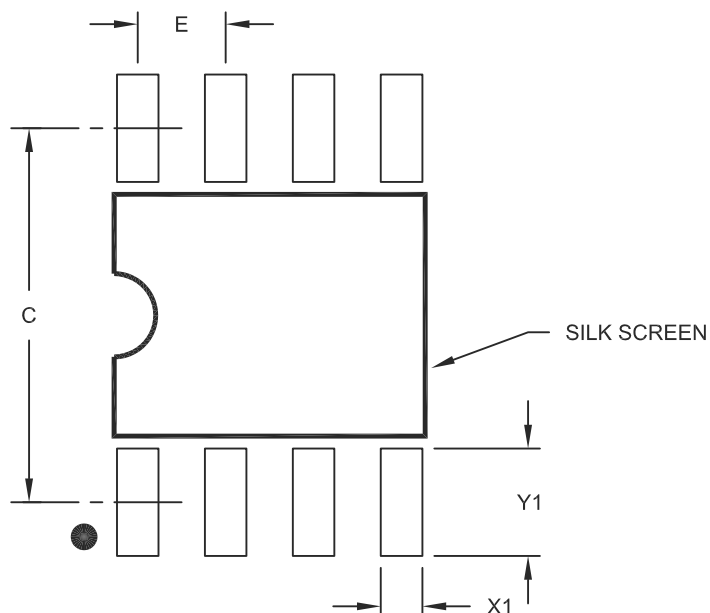
FIGURE 17-42: MINIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE



PIC12F609/615/617/12HV609/615

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

PIC12F609/615/617/12HV609/615

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