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Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f609-i-mf

PIC12F609/615/617/12HV609/615

FIGURE 2-4: DATA MEMORY MAP OF THE PIC12F615/617/HV615

File Address	File Address
Indirect Addr. ⁽¹⁾ 00h	Indirect Addr. ⁽¹⁾ 80h
TMR0 01h	OPTION_REG 81h
PCL 02h	PCL 82h
STATUS 03h	STATUS 83h
FSR 04h	FSR 84h
GPIO 05h	TRISIO 85h
06h	86h
07h	87h
08h	88h
09h	89h
PCLATH 0Ah	PCLATH 8Ah
INTCON 0Bh	INTCON 8Bh
PIR1 0Ch	PIE1 8Ch
0Dh	8Dh
TMR1L 0Eh	PCON 8Eh
TMR1H 0Fh	8Fh
T1CON 10h	OSCTUNE 90h
TMR2 11h	91h
T2CON 12h	PR2 92h
CCPR1L 13h	APFCON 93h
CCPR1H 14h	94h
CCP1CON 15h	WPU 95h
PWM1CON 16h	IOC 96h
ECCPAS 17h	97h
18h	PMCON1 ⁽²⁾ 98h
VRCON 19h	PMCON2 ⁽²⁾ 99h
CMCON0 1Ah	PMADRL ⁽²⁾ 9Ah
1Bh	PMADRH ⁽²⁾ 9Bh
CMCON1 1Ch	PMDATL ⁽²⁾ 9Ch
1Dh	PMDATH ⁽²⁾ 9Dh
ADRESH 1Eh	ADRESL 9Eh
ADCON0 1Fh	ANSEL 9Fh
20h	A0h
General Purpose Registers 96 Bytes from 20h-7Fh ⁽²⁾ Unimplemented for PIC12F615/HV615	General Purpose Registers 32 Bytes ⁽²⁾ Unimplemented for PIC12F615/HV615
3Fh	BFh
40h	C0h
General Purpose Registers 64 Bytes	
6Fh	EFh
Accesses 70h-7Fh	F0h
7Fh	FFh
Bank 0	Bank 1

Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.
Note 2: Used for the PIC12F617 only.

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3.3 Reading the Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the PMADRL and PMADRH registers, and then set control bit RD (PMCON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the “BSF PMCON1,RD” instruction to be ignored. The data is available in the very next cycle in the PMDATL and PMDATH registers; it can be read as two bytes in the following instructions. PMDATL and PMDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-1: FLASH PROGRAM READ

```
BANKSEL PM_ADR           ; Change STATUS bits RP1:0 to select bank with PMADRL
MOVLW  MS_PROG_PM_ADDR  ;
MOVWF  PMADRH           ; MS Byte of Program Address to read
MOVLW  LS_PROG_PM_ADDR  ;
MOVWF  PMADRL           ; LS Byte of Program Address to read
BANKSEL PMCON1          ; Bank to containing PMCON1
BSF    PMCON1, RD       ; PM Read

NOP                       ; First instruction after BSF PMCON1,RD executes normally

NOP                       ; Any instructions here are ignored as program
                          ; memory is read in second cycle after BSF PMCON1,RD
                          ;

BANKSEL PMDATL          ; Bank to containing PMADRL
MOVF   PMDATL, W        ; W = LS Byte of Program PMDATL
MOVF   PMDATH, W        ; W = MS Byte of Program PMDATL
```

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4.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two selectable clock frequencies: 4 MHz and 8 MHz

The system clock can be selected between external or internal clock sources via the FOSC<2:0> bits of the Configuration Word register.

4.3 External Clock Modes

4.3.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 4-1.

TABLE 4-1: OSCILLATOR DELAY EXAMPLES

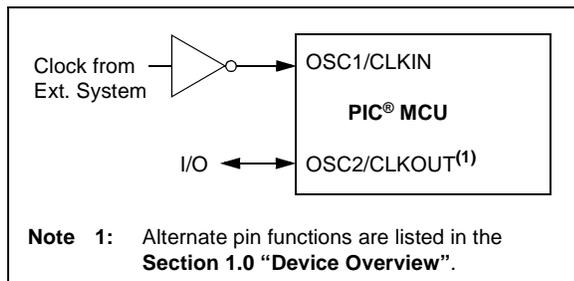
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	INTOSC	125 kHz to 8 MHz	Oscillator Warm-Up Delay (TWARM)
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)

4.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 4-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 4-2: EXTERNAL CLOCK (EC) MODE OPERATION



4.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

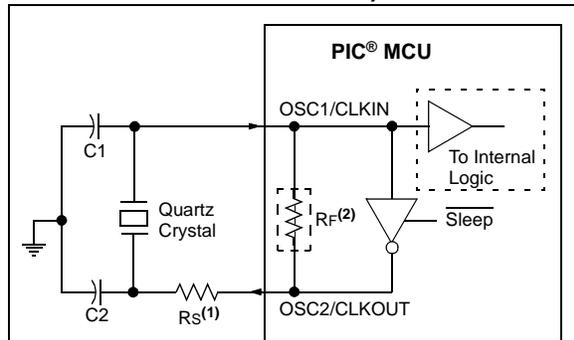
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 4-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



- Note 1:** A series resistor (R_S) may be required for quartz crystals with low drive level.
- 2:** The value of R_F varies with the Oscillator mode selected (typically between 2 M Ω to 10 M Ω).

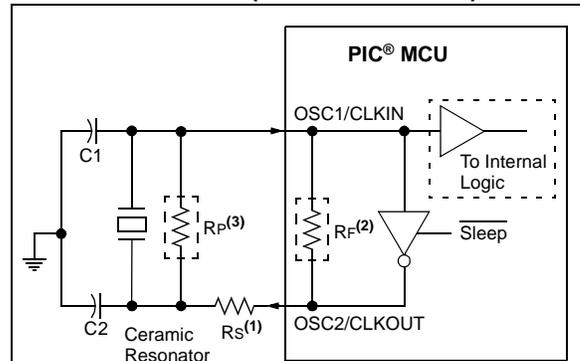
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "Crystal Oscillator Basics and Crystal Selection for rPIC[®] and PIC[®] Devices" (DS00826)
- AN849, "Basic PIC[®] Oscillator Design" (DS00849)
- AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
- AN949, "Making Your Oscillator Work" (DS00949)

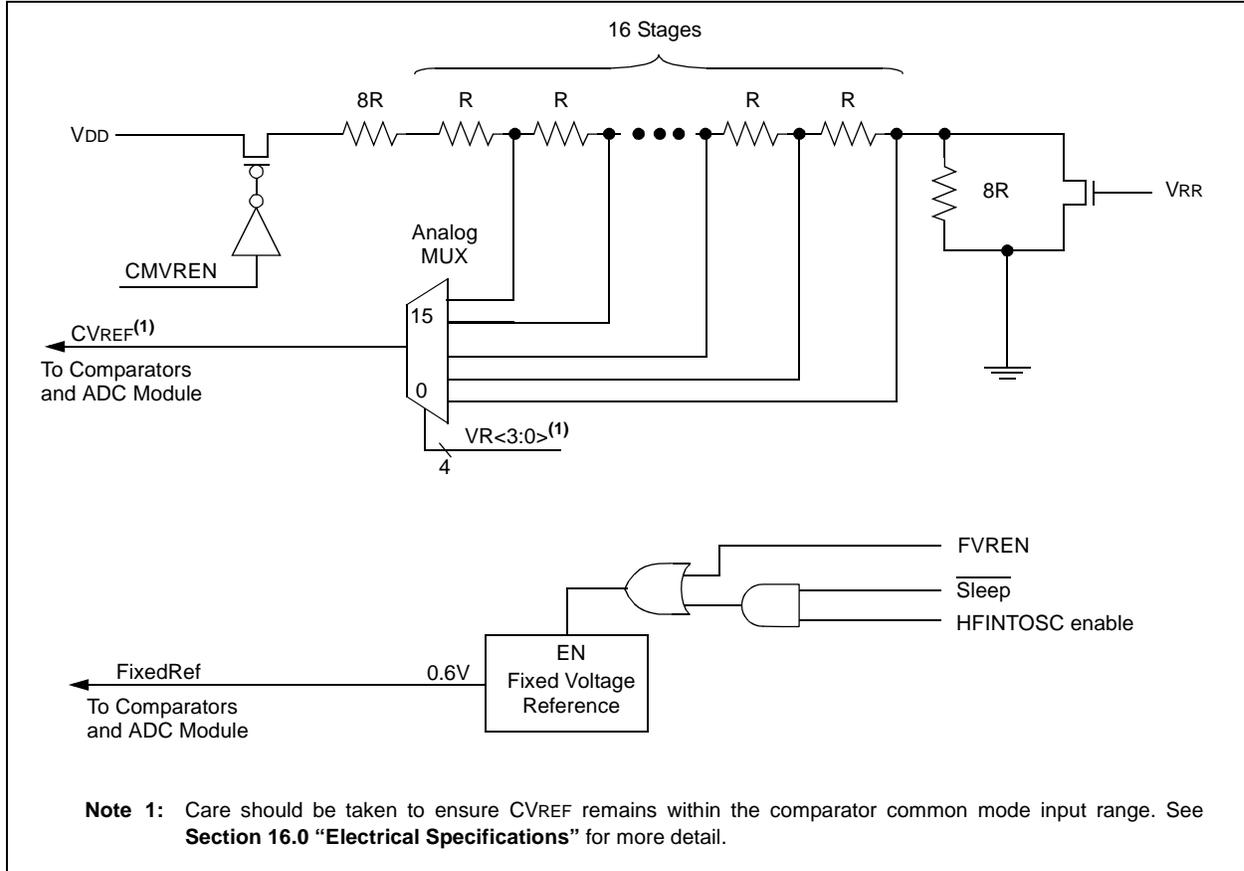
FIGURE 4-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



- Note 1:** A series resistor (R_S) may be required for ceramic resonators with low drive level.
- 2:** The value of R_F varies with the Oscillator mode selected (typically between 2 M Ω to 10 M Ω).
- 3:** An additional parallel feedback resistor (R_P) may be required for proper ceramic resonator operation.

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FIGURE 9-6: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



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REGISTER 9-3: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMVREN	—	VRR	FVREN	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 7 **CMVREN:** Comparator Voltage Reference Enable bit^(1, 2)
 1 = CVREF circuit powered on and routed to CVREF input of the Comparator
 0 = 0.6 Volt constant reference routed to CVREF input of the Comparator
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **VRR:** CVREF Range Selection bit
 1 = Low range
 0 = High range
- bit 4 **FVREN:** 0.6V Reference Enable bit⁽²⁾
 1 = Enabled
 0 = Disabled
- bit 3-0 **VR<3:0>:** Comparator Voltage Reference CVREF Value Selection bits ($0 \leq VR<3:0> \leq 15$)
When VRR = 1: $CVREF = (VR<3:0>/24) * VDD$
When VRR = 0: $CVREF = VDD/4 + (VR<3:0>/32) * VDD$

- Note 1:** When CMVREN is low, the CVREF circuit is powered down and does not contribute to IDD current.
Note 2: When CMVREN is low and the FVREN bit is low, the CVREF signal should provide Vss to the comparator.

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10.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE (PIC12F615/617/HV615 ONLY)

Note: The ADRESL and ADRESH registers are Read Only.

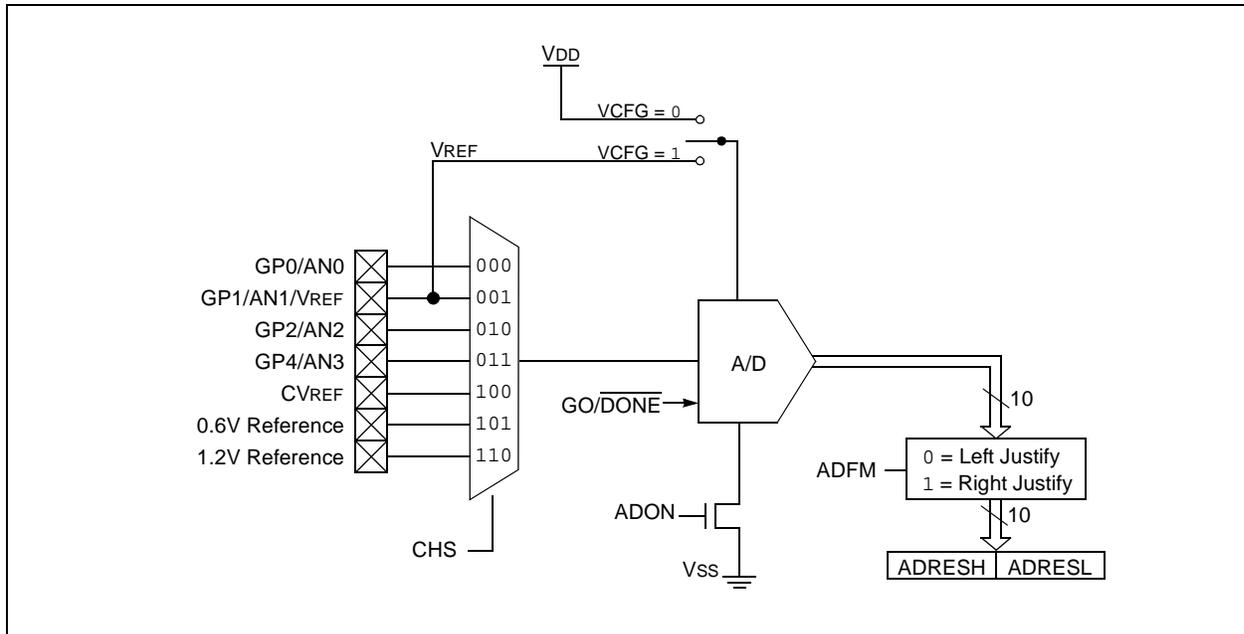
The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 10-1 shows the block diagram of the ADC.

FIGURE 10-1: ADC BLOCK DIAGRAM



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10.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 10-4. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 10-4.

The maximum recommended impedance for analog sources is 10 kΩ. As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed),

an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 10-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 10-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{2047} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left(1 - e^{-\frac{T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{-\frac{T_C}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{2047} \right) \quad ;\text{combining [1] and [2]}$$

Solving for TC:

$$\begin{aligned} T_C &= -CHOLD(RIC + RSS + RS) \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.37\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\ &= 4.67\mu s \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

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12.2 Calibration Bits

The 8 MHz internal oscillator is factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the *Memory Programming Specification* (DS41204) and thus, does not require reprogramming.

12.3 Reset

The PIC12F609/615/617/12HV609/615 device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- MCLR Reset during normal operation
- MCLR Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

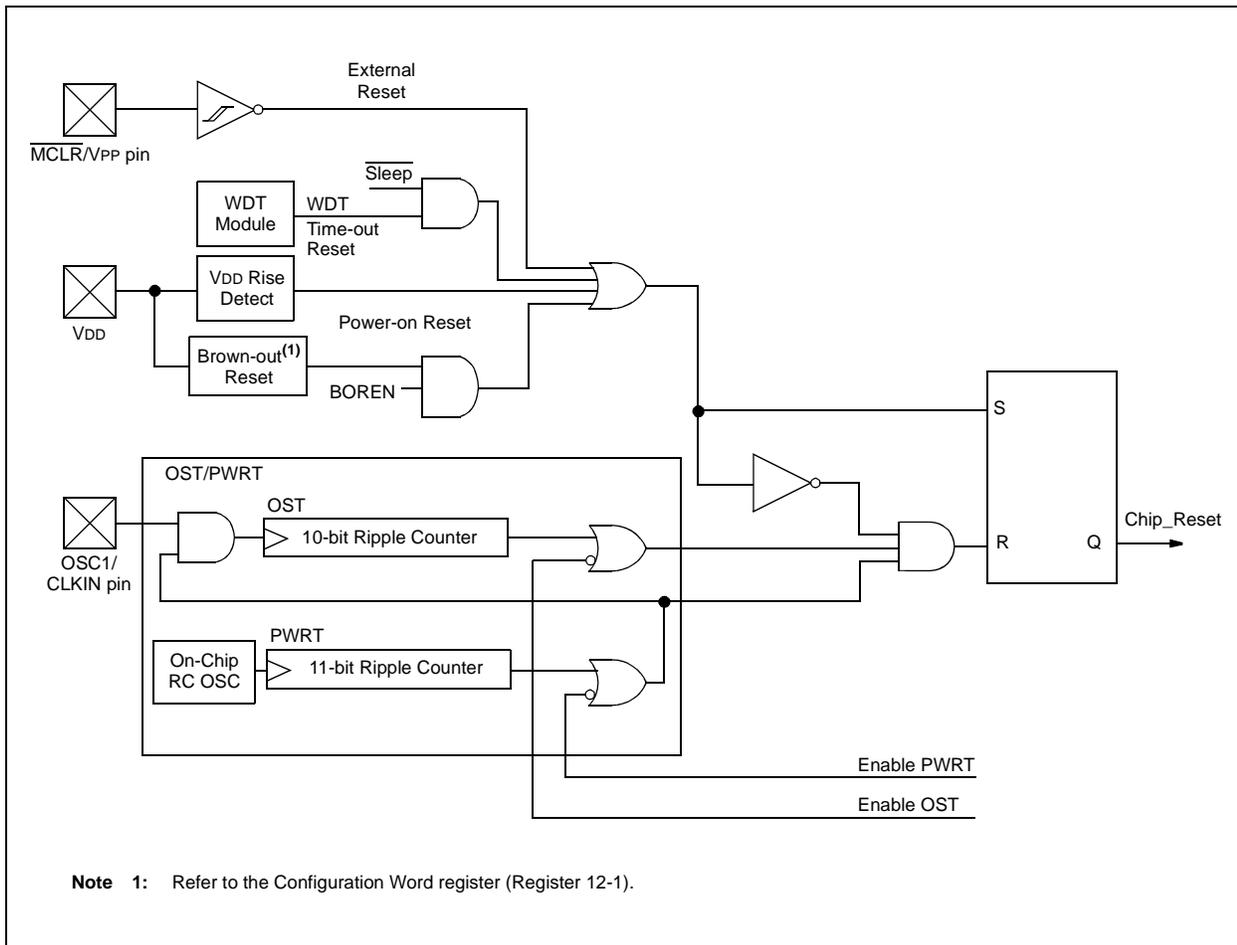
- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. \overline{TO} and \overline{PD} bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-5 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See **Section 16.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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12.3.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See **Section 16.0 “Electrical Specifications”** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOR (see **Section 12.3.4 “Brown-out Reset (BOR)”**).

Note: The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach Vss for a minimum of 100 μ s.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure proper operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, “Power-up Trouble Shooting” (DS00607).

12.3.2 MCLR

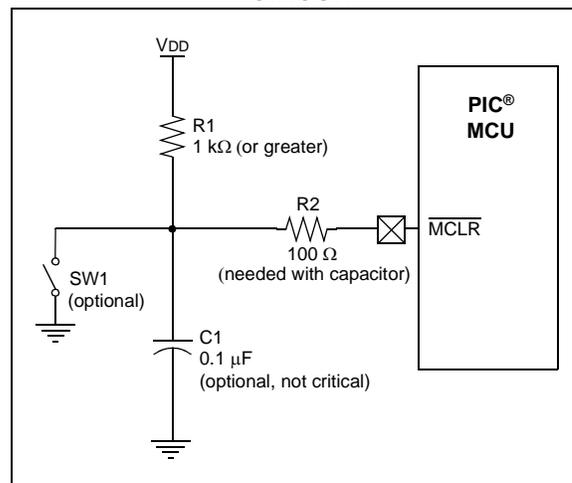
PIC12F609/615/617/12HV609/615 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 12-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the GP3/MCLR pin becomes an external Reset input. In this mode, the GP3/MCLR pin has a weak pull-up to VDD.

FIGURE 12-2: RECOMMENDED MCLR CIRCUIT



12.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from an internal RC oscillator. For more information, see **Section 4.4 “Internal Clock Modes”**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRTE, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 16.0 “Electrical Specifications”**).

Note: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the MCLR pin, rather than pulling this pin directly to Vss.

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TABLE 12-5: INITIALIZATION CONDITION FOR REGISTERS (PIC12F615/617/HV615)

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	05h	--x0 x000	--u0 u000	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu ⁽²⁾
PIR1	0Ch	-000 0-00	-000 0-00	-uuu u-uu ⁽²⁾
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2 ⁽¹⁾	11h	0000 0000	0000 0000	uuuu uuuu
T2CON ⁽¹⁾	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L ⁽¹⁾	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H ⁽¹⁾	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON ⁽¹⁾	15h	0-00 0000	0-00 0000	u-uu uuuu
PWM1CON ⁽¹⁾	16h	0000 0000	0000 0000	uuuu uuuu
ECCPAS ⁽¹⁾	17h	0000 0000	0000 0000	uuuu uuuu
VRCON	19h	0-00 0000	0-00 0000	u-uu uuuu
CMCON0	1Ah	0000 -0-0	0000 -0-0	uuuu -u-u
CMCON1	1Ch	---0 0-10	---0 0-10	---u u-qu
ADRESH ⁽¹⁾	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0 ⁽¹⁾	1Fh	00-0 0000	00-0 0000	uu-u uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISIO	85h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	-00- 0-00	-00- 0-00	-uu- u-uu
PCON	8Eh	---- --0x	---- --uu ^(1, 5)	---- --uu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
APFCON	93h	---0 --00	---0 --00	---u --uu
WPU	95h	--11 -111	--11 -111	--uu -uuu
IOC	96h	--00 0000	--00 0000	--uu uuuu
PMCON1 ⁽⁶⁾	98h	---- -000	---- -000	---- -uuu
PMCON2 ⁽⁶⁾	99h	---- ----	---- ----	---- ----
PMADRL ⁽⁶⁾	9Ah	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-6 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: For PIC12F617 only.

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NOTES:

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MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If d = 0, destination is W register. If d = 1, the destination is file register 'f' itself. d = 1 is useful to test a file register since Status flag Z is affected.
Words:	1
Cycles:	1
Example:	<pre>MOVF FSR, 0</pre> <p>After Instruction</p> <pre>W = value in FSR register Z = 1</pre>

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	<pre>MOVWF OPTION F</pre> <p>Before Instruction</p> <pre>OPTION = 0xFF W = 0x4F</pre> <p>After Instruction</p> <pre>OPTION = 0x4F W = 0x4F</pre>

MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	k → (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	<pre>MOVLW 0x5A</pre> <p>After Instruction</p> <pre>W = 0x5A</pre>

NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	<pre>NOP</pre>

PIC12F609/615/617/12HV609/615

NOTES:

PIC12F609/615/617/12HV609/615

17.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 17-1: PIC12F609/615/617 I_{DD LP} (32 kHz) vs. V_{DD}

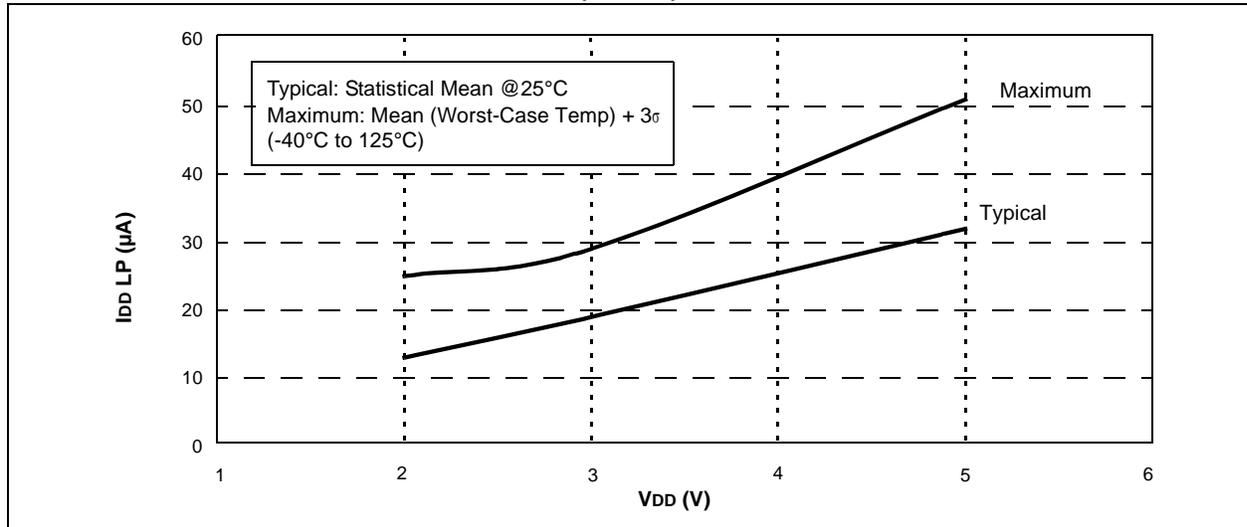
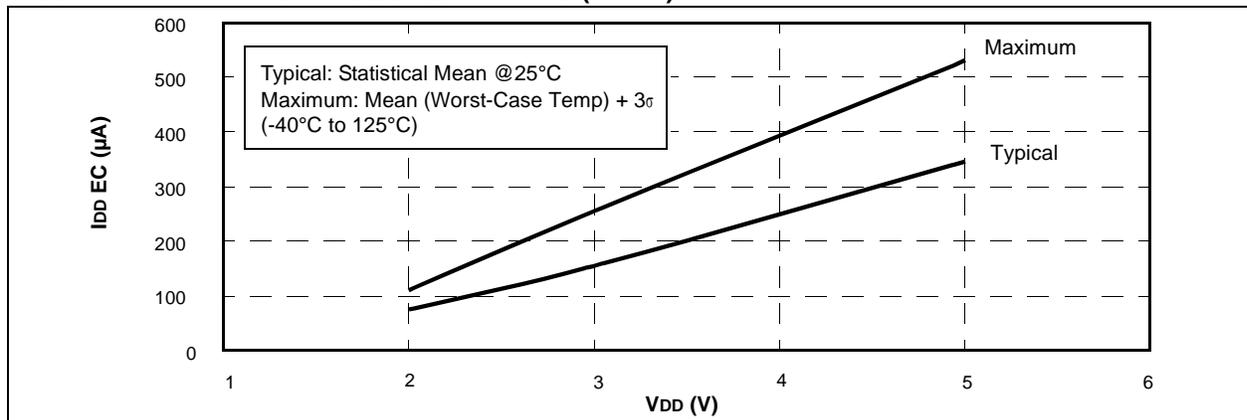


FIGURE 17-2: PIC12F609/615/617 I_{DD EC} (1 MHz) vs. V_{DD}



PIC12F609/615/617/12HV609/615

FIGURE 17-10: PIC12F609/615/617 IPD BASE vs. VDD

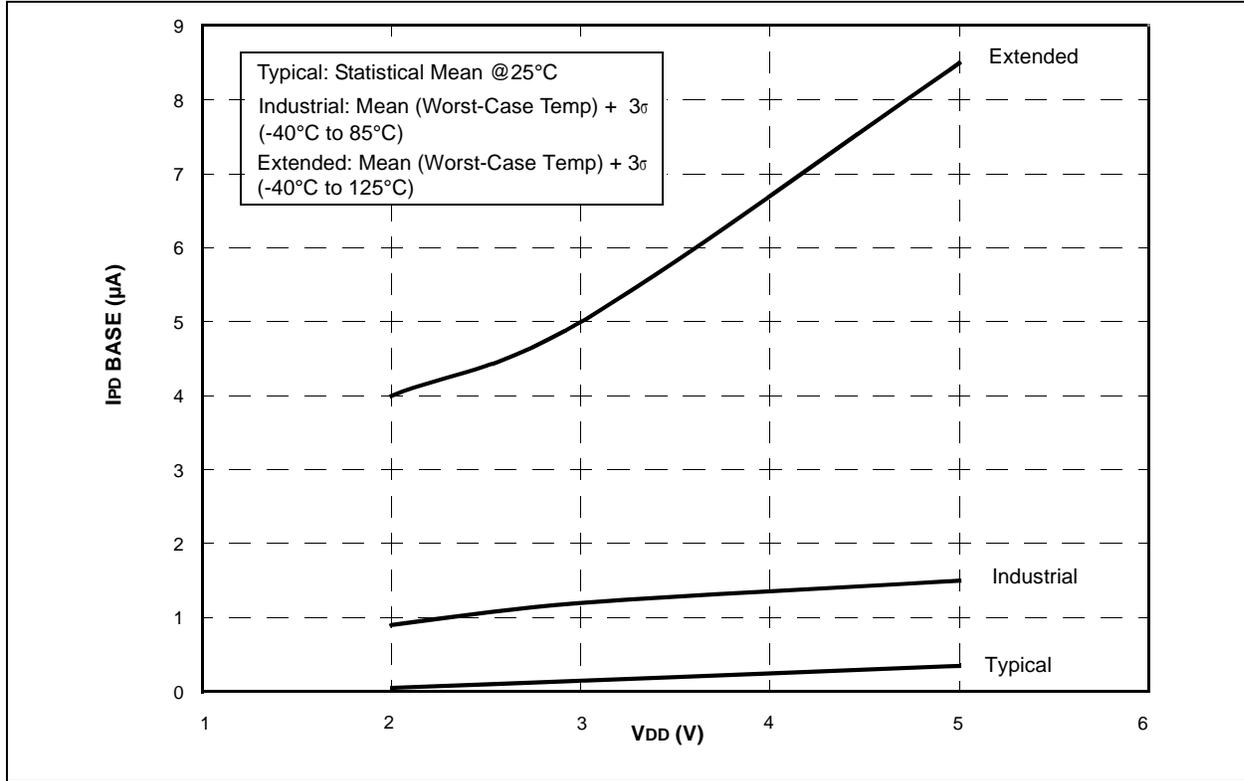
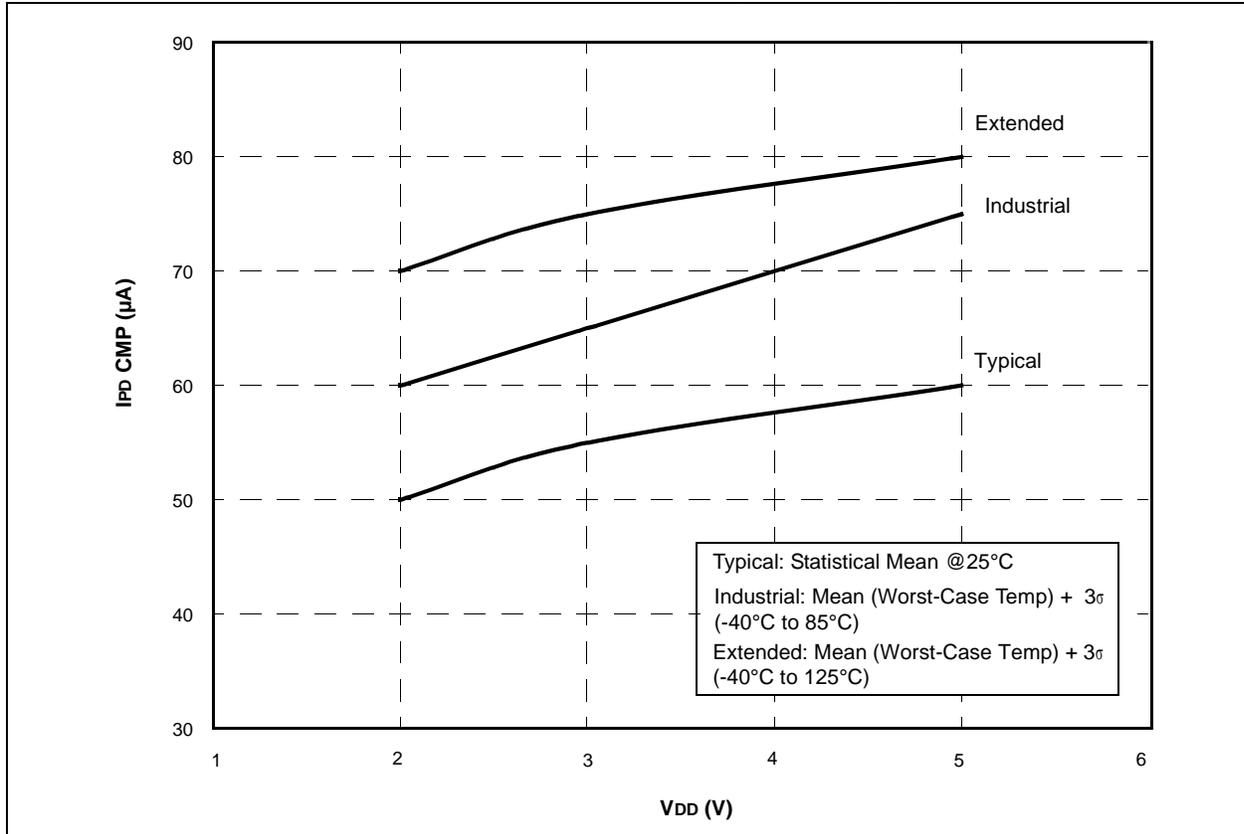


FIGURE 17-11: PIC12F609/615/617 IPD COMPARATOR (SINGLE ON) vs. VDD



PIC12F609/615/617/12HV609/615

FIGURE 17-14: PIC12F609/615/617 IPD CVREF (LOW RANGE) vs. VDD

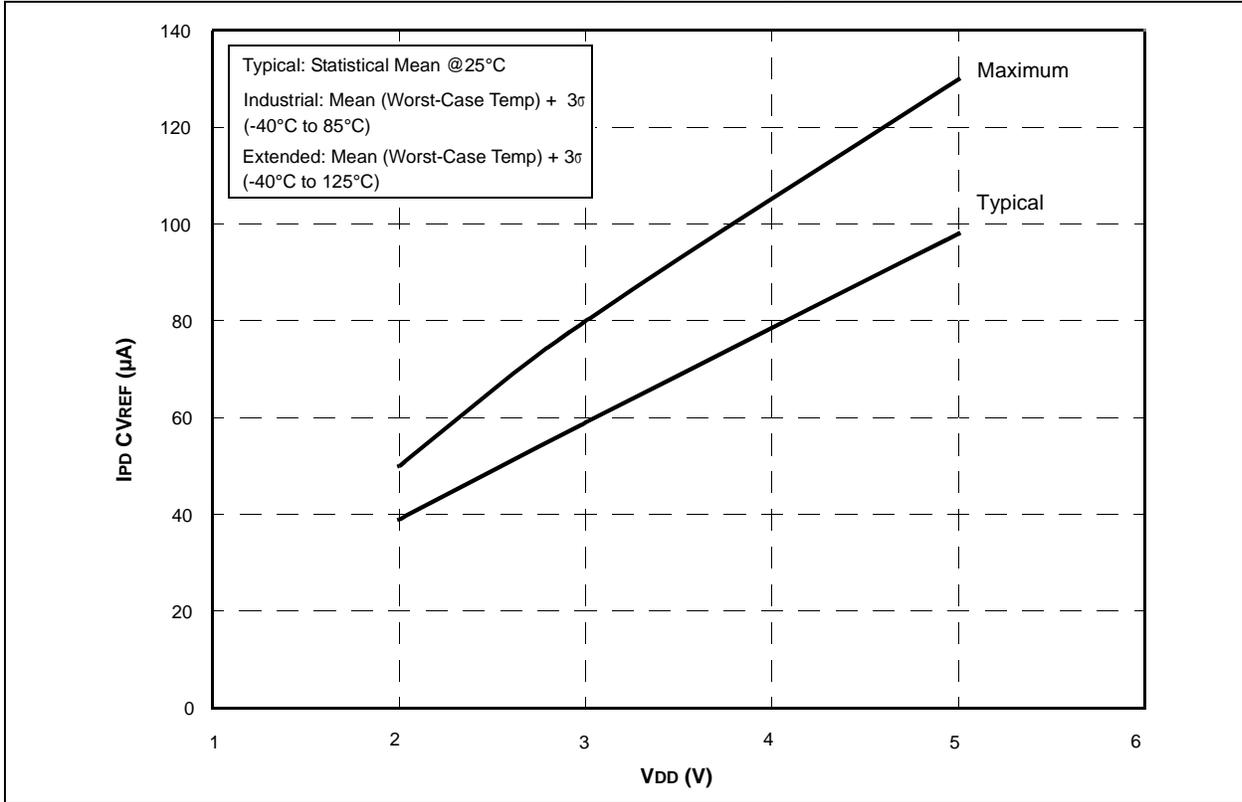
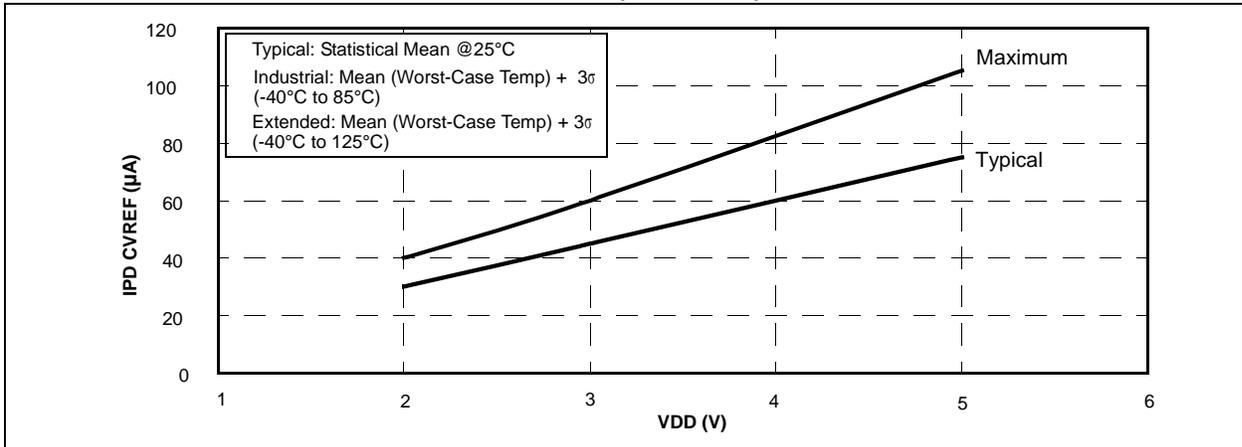


FIGURE 17-15: PIC12F609/615/617 IPD CVREF (HI RANGE) vs. VDD



PIC12F609/615/617/12HV609/615

FIGURE 17-33: PIC12HV615 IPD A/D vs. VDD

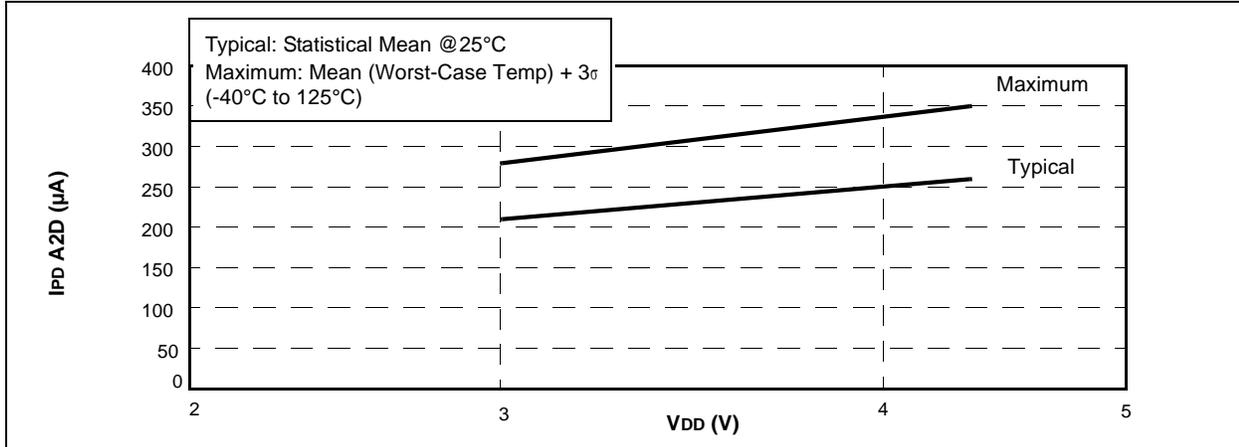
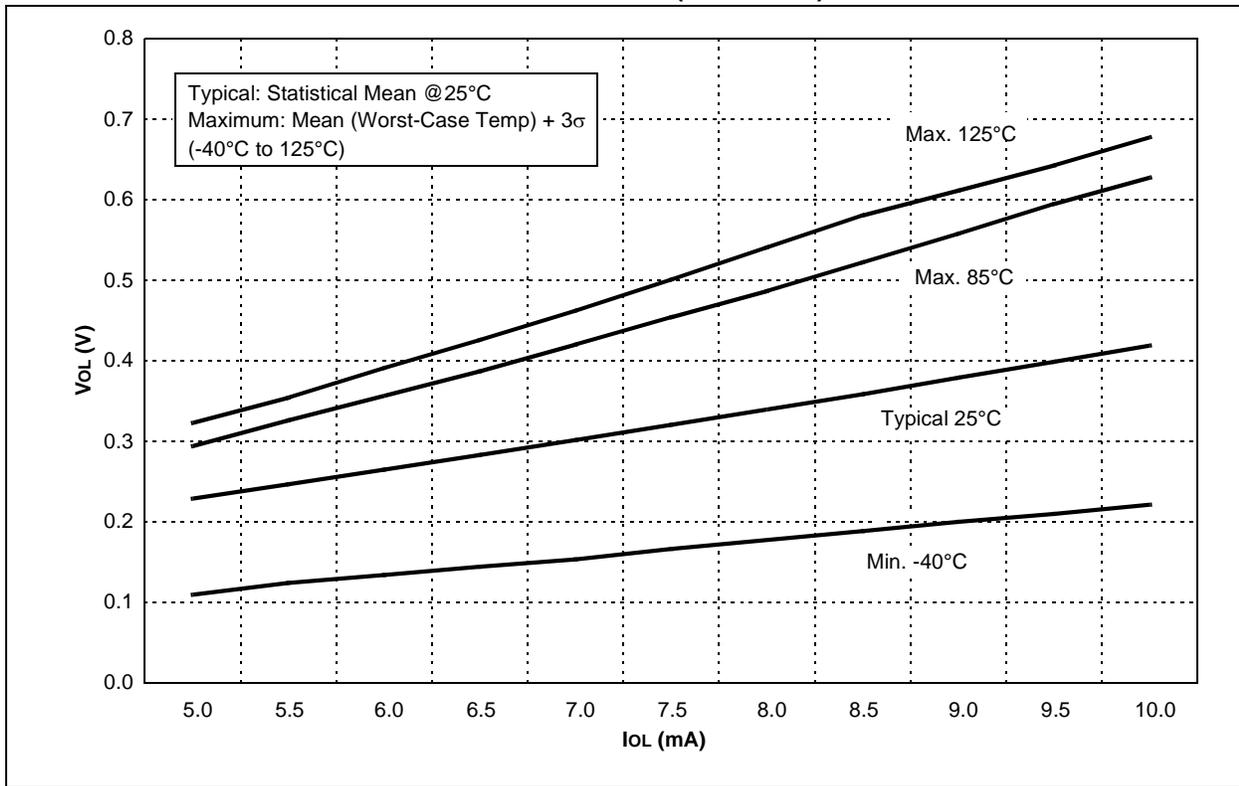


FIGURE 17-34: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)



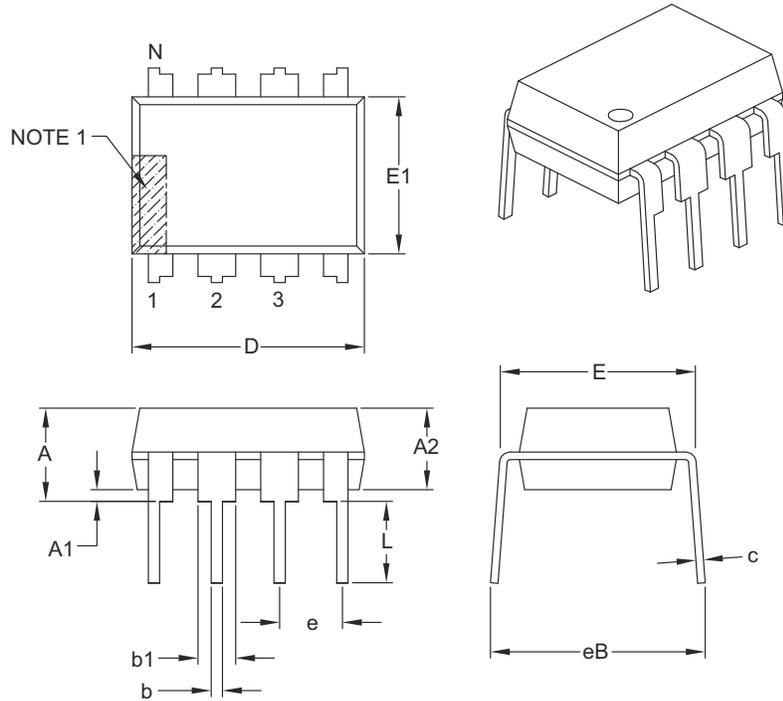
PIC12F609/615/617/12HV609/615

18.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

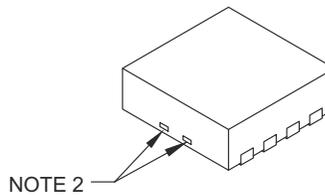
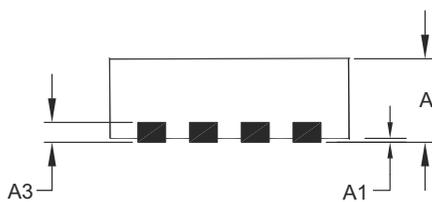
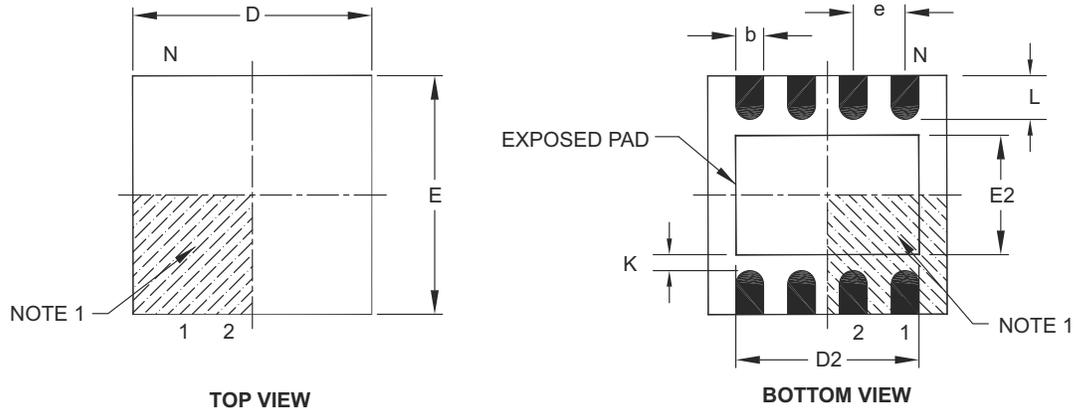
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

PIC12F609/615/617/12HV609/615

8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Width	E2	0.00	–	1.60
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	0.00	–	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B