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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f609-i-ms

Device	Program Memory	Data Memory	Self Read/	elf Read/		Comparators	ECCD	Timers	Voltage Range	
Device	Flash (words)	SRAM (bytes)	Self Write	1/0	(ch)	Comparators		8/16-bit	voltage Kange	
PIC12F609	1024	64	_	5	0	1		1/1	2.0V-5.5V	
PIC12HV609	1024	64	_	5	0	1		1/1	2.0V-user defined	
PIC12F615	1024	64	_	5	4	1	YES	2/1	2.0V-5.5V	
PIC12HV615	1024	64	_	5	4	1	YES	2/1	2.0V-user defined	
PIC12F617	2048	128	YES	5	4	1	YES	2/1	2.0V-5.5V	

8-Pin Diagram, PIC12F609/HV609 (PDIP, SOIC, MSOP, DFN)

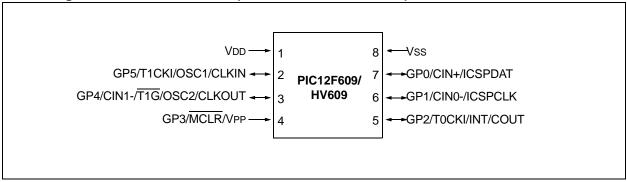


TABLE 1: PIC12F609/HV609 PIN SUMMARY (PDIP, SOIC, MSOP, DFN)

I/O	Pin	Comparators	Timer	Interrupts	Pull-ups	Basic
GP0	7	CIN+	1	IOC	Y	ICSPDAT
GP1	6	CIN0-	_	IOC	Y	ICSPCLK
GP2	5	COUT	T0CKI	INT/IOC	Υ	_
GP3 ⁽¹⁾	4	_	_	IOC	Y ⁽²⁾	MCLR/Vpp
GP4	3	CIN1-	T1G	IOC	Υ	OSC2/CLKOUT
GP5	2	_	T1CKI	IOC	Y	OSC1/CLKIN
_	1	_		_	_	VDD
_	8	_	_	_	_	Vss

Note 1: Input only.

2: Only when pin is configured for external MCLR.

FIGURE 2-4: DATA MEMORY MAP OF THE PIC12F615/617/HV615

0h 1h 2h 3h 5h 6h 8h 8h 8h 8h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h	Indirect Addr.(1) OPTION_REG PCL STATUS FSR TRISIO PCLATH INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1(2) PMCON2(2) PMADRL(2)	80h 81h 82h 83h 84h 85h 86h 87h 88h 8Ch 8Dh 8Eh 90h 91h 92h 93h 95h 96h 97h 98h
2h 3h 4h 5h 6h 7h 8h Bh Ch Eh 0h 1h 2h 4h 5h 6h 7h 8h Bh Ch 1h 2h 4h 5h 6h 7h 8h 8h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h	PCL STATUS FSR TRISIO PCLATH INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	82h 83h 84h 85h 86h 87h 88h 8Ch 8Dh 8Eh 90h 91h 92h 93h 95h 96h 97h
3h 4h 5h 6h 7h 8h 9h Bh Ch Dh Eh 1h 2h 3h 4h 5h 6h 7h 8h Bh Ch Dh 1h 2h 5h 1h 8h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h 1h	PCLATH INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	83h 84h 85h 86h 87h 88h 80h 8Ch 8Dh 8Eh 90h 91h 92h 93h 95h 95h 97h
4h 5h 6h 7h 8h 9h Bh Ch Dh Eh 0h 1h 2h 4h 5h 6h 7h 8h Bh Bh Bh Bh Bh Bh Bh Bh Bh Bh Bh Bh Bh	PCLATH INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	84h 85h 86h 87h 88h 89h 8Ch 8Dh 8Eh 90h 91h 92h 93h 95h 96h 97h 98h
5h 6h 7h 8h 9h Bh Ch Dh Eh 0h 1h 2h 3h 4h 5h 6h 7h 8h Bh Bh	PCLATH INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	85h 86h 87h 88h 89h 8Ah 8Ch 8Dh 8Eh 90h 91h 92h 93h 95h 96h 97h
6h 7h 8h 9h Ah Bh Ch Dh Eh 5h 3h 4h 5h 6h 7h 8h Bh	PCLATH INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	86h 87h 88h 89h 8Ch 8Ch 8Ch 90h 91h 92h 93h 94h 95h 96h 97h
7h 8h 9h Ah Bh Ch Dh Eh Fh 0h 12h 3h 4h 5h 6h 7h 8h 9h 8h 8h 8h 8h 8h 8h 8h 8h 8h 8h 8h 8h 8h	INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	87h 88h 89h 8Ah 8Br 8Cr 8Dr 8Er 90h 91h 92h 93h 94h 95h 96h 97h 98h
8h 9h Ah Bh Ch Dh Eh 7h 3h 4h 5h 6h 7h 8h 9h Bh	INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	88h 89h 8Ah 8Bh 8Cr 8Dr 8Eh 90h 91h 92h 93h 94h 95h 96h 97h
9h Ah Bh Ch Dh Eh 7h 3h 4h 5h 6h 7h 8h 9h Bh	INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	89h 8Ah 8Bh 8Ch 8Dh 8Eh 90h 91h 92h 93h 94h 95h 96h 97h
Ah Bh Ch Dh Eh Fh 0h 1h 2h 3h 4h 5h 6h 7h 8h 9h Ah Bh	INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	8Ah 8Bh 8Ch 8Dh 8Eh 90h 91h 92h 93h 94h 95h 96h 97h
Bh Ch Dh Eh Fh Oh 1h 2h 3h 5h 6h 7h 8h 9h Ah Bh	INTCON PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	8Bh 8Ch 8Ch 8Dh 8Eh 90h 91h 92h 93h 94h 95h 97h 98h
Ch Dh Eh Fh Oh 1h 2h 3h 4h 5h 6h 7h 8h 9h Ah Bh	PIE1 PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	8Ch 8Dh 8Eh 90h 91h 92h 93h 94h 95h 96h 97h 98h
Dh Eh Fh Oh 1h 2h 3h 4h 5h 6h 7h 8h 9h Ah Bh	PCON OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	8Dh 8Eh 90h 91h 92h 93h 94h 95h 96h 98h
Eh Fh Oh 1h 2h 3h 4h 5h 6h 7h 8h 9h Ah	OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	8Eh 8Fh 90h 91h 92h 93h 94h 95h 96h 98h
Fh Oh 1h 2h 3h 4h 5h 6h 7h 8h 9h Ah	OSCTUNE PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	8Fh 90h 91h 92h 93h 94h 95h 96h 97h
0h 1h 2h 3h 4h 5h 6h 7h 8h 9h Ah	PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	90h 91h 92h 93h 94h 95h 96h 97h 98h
1h 2h 3h 4h 5h 6h 7h 8h 9h Ah	PR2 APFCON WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	91h 92h 93h 94h 95h 96h 97h 98h
2h 3h 4h 5h 6h 7h 8h 9h Ah	MPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	92h 93h 94h 95h 96h 97h 98h
3h 4h 5h 6h 7h 8h 9h Ah	MPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	93h 94h 95h 96h 97h 98h
4h 5h 6h 7h 8h 9h Ah	WPU IOC PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	94h 95h 96h 97h 98h
5h 6h 7h 8h 9h Ah Bh	PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	95h 96h 97h 98h
6h 7h 8h 9h Ah Bh	PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	96h 97h 98h
7h 8h 9h Ah Bh	PMCON1 ⁽²⁾ PMCON2 ⁽²⁾	97h 98h
8h 9h Ah Bh	PMCON2 ⁽²⁾	98h
9h Ah Bh	PMCON2 ⁽²⁾	
Ah Bh	PMCON2 ⁽²⁾ PMADRL ⁽²⁾	99h
Bh	PMADRL ⁽²⁾	1 000
	781	9Ah
	PMADRH ⁽²⁾	9Bh
Ch	PMDATL ⁽²⁾	9Ch
Dh	PMDATH ⁽²⁾	9Dł
Eh	ADRESL	9Er
Fh	ANSEL	9Fh
0h	General Purpose Registers 32 Bytes ⁽²⁾ Unimplemented for PIC12F615/HV615	A0h
		BFh
Fh		C0h
Fh		EFh
0h	Accesses 70h-7Fh	F0h
Fh	L Bank 1	FFr
	Fh Oh Fh Oh Fh	Fh ANSEL General Purpose Registers 32 Bytes ⁽²⁾ Unimplemented for PIC12F615/HV615 Fh Oh Accesses 70h-7Fh

4.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two selectable clock frequencies: 4 MHz and 8 MHz

The system clock can be selected between external or internal clock sources via the FOSC<2:0> bits of the Configuration Word register.

4.3 External Clock Modes

4.3.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 4-1.

TABLE 4-1: OSCILLATOR DELAY EXAMPLES

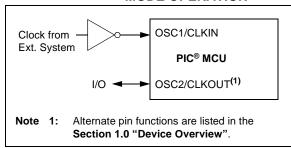
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	INTOSC	125 kHz to 8 MHz	Oscillator Warm-Up Delay (ТWARM)
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)

4.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 4-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 4-2: EXTERNAL CLOCK (EC)
MODE OPERATION



REGISTER 5-5: WPU: WEAK PULL-UP GPIO REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
_	_	WPU5	WPU4	_	WPU2	WPU1	WPU0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-4 WPU<5:4>: Weak Pull-up Control bits

1 = Pull-up enabled0 = Pull-up disabled

bit 3 **WPU<3>:** Weak Pull-up Register bit⁽³⁾ bit 2-0 **WPU<2:0>:** Weak Pull-up Control bits

1 = Pull-up enabled0 = Pull-up disabled

Note 1: Global GPPU must be enabled for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).

3: The GP3 pull-up is enabled when configured as MCLR in the Configuration Word, otherwise it is disabled as an input and reads as '0'.

4: WPU<5:4> always reads '1' in XT, HS and LP Oscillator modes.

REGISTER 5-6: IOC: INTERRUPT-ON-CHANGE GPIO REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	_	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 IOC<5:0>: Interrupt-on-change GPIO Control bit

1 = Interrupt-on-change enabled0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.

2: IOC<5:4> always reads '1' in XT, HS and LP Oscillator modes.

7.10 ECCP Special Event Trigger (PIC12F615/617/HV615 only)

If a ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the Fosc to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see Section 11.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)".

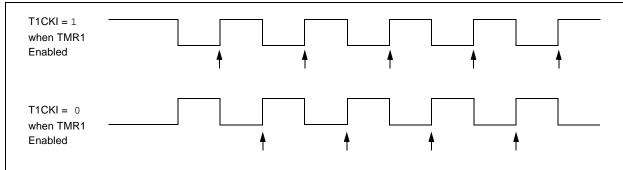
7.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 9.0 "Comparator Module"**.

FIGURE 7-2: TIMER1 INCREMENTING EDGE



- Note 1: Arrows indicate counter increments.
 - 2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

9.0 COMPARATOR MODULE

The comparator can be used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparator is a very useful mixed signal building block because it provides analog functionality independent of the program execution. The Analog Comparator module includes the following features:

- · Programmable input section
- Comparator output is available internally/externally
- · Programmable output polarity
- · Interrupt-on-change
- · Wake-up from Sleep
- PWM shutdown
- Timer1 gate (count enable)
- · Output synchronization to Timer1 clock input
- · Programmable voltage reference
- User-enable Comparator Hysteresis

9.1 Comparator Overview

The comparator is shown in Figure 9-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less

than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

FIGURE 9-1:SINGLE COMPARATOR

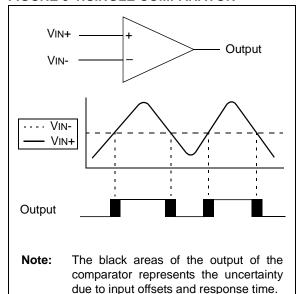
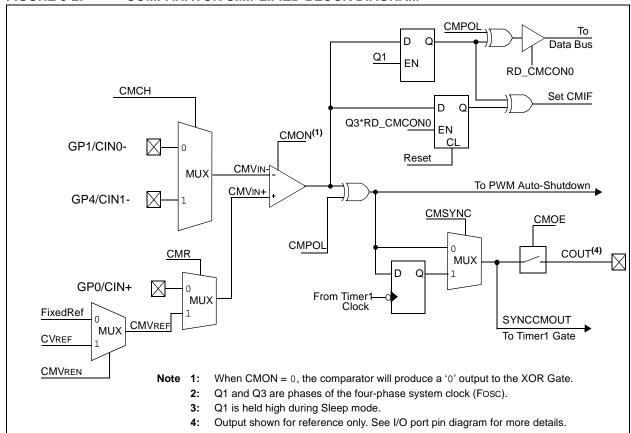


FIGURE 9-2: COMPARATOR SIMPLIFIED BLOCK DIAGRAM



REGISTER 10-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

| R-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES9 | ADRES8 | ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 ADRES<9:2>: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 10-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	_	_	_	_	_	_
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6 ADRES<1:0>: ADC Result Register bits

Lower 2 bits of 10-bit conversion result

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 10-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
_	_	_	_	_	_	ADRES9	ADRES8
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-2 Unimplemented: Read as '0'

bit 1-0 ADRES<9:8>: ADC Result Register bits

Upper 2 bits of 10-bit conversion result

REGISTER 10-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

| R-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits

Lower 8 bits of 10-bit conversion result

11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

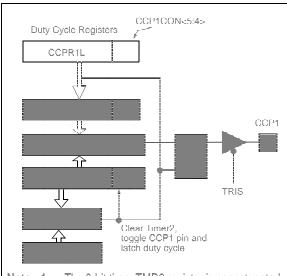
Note: Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

Figure 11-3 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 11.3.7** "**Setup for PWM Operation**".

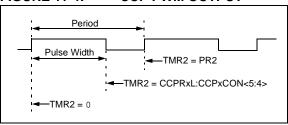
FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM



- The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base.
 - 2: In PWM mode, CCPR1H is a read-only register.

The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 11-4: CCP PWM OUTPUT



12.4 Interrupts

The PIC12F609/615/617/12HV609/615 has 8 sources of interrupt:

- External Interrupt GP2/INT
- Timer0 Overflow Interrupt
- · GPIO Change Interrupts
- · Comparator Interrupt
- A/D Interrupt (PIC12F615/617/HV615 only)
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt (PIC12F615/617/HV615 only)
- Enhanced CCP Interrupt (PIC12F615/617/HV615 only)
- Flash Memory Self Write (PIC12F617 only)

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- . The PC is loaded with 0004h.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- GPIO Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

For external interrupt events, such as the INT pin or GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or twocycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

- Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.
 - 2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, Enhanced CCP modules, refer to the respective peripheral section.

12.4.1 GP2/INT INTERRUPT

The external interrupt on the GP2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See Section 12.7 "Power-Down Mode (Sleep)" for details on Sleep and Figure 12-9 for timing of wake-up from Sleep through GP2/INT interrupt.

Note: The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

15.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

15.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC[®] Flash MCUs and dsPIC[®] Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with incircuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a rugge-dized probe interface and long (up to three meters) interconnection cables.

15.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

15.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC[®] and dsPIC[®] Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming[™].

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

16.4 DC Characteristics: PIC12F609/615/617 - I (Industrial)

DC CHA	ARACTERISTICS		ard Operating temp				s otherwise stated) 85°C for industrial
Param	Davisa Characteristics	Min	T 1	Max	l luite		Conditions
No.	Device Characteristics	Min	Тур†	Max	Units	VDD	Note
D020	Power-down Base Current (IPD) ⁽²⁾	_	0.05	0.9	μА	2.0	WDT, BOR, Comparator, VREF and T1OSC disabled
		_	0.15	1.2	μА	3.0	
	PIC12F609/615/617	_	0.35	1.5	μА	5.0	
			150	500	nA	3.0	$-40^{\circ}C \le TA \le +25^{\circ}C$ for industrial
D021		_	0.5	1.5	μА	2.0	WDT Current ⁽¹⁾
		_	2.5	4.0	μА	3.0	7
		_	9.5	17	μА	5.0]
D022		_	5.0	9	μΑ	3.0	BOR Current ⁽¹⁾
		_	6.0	12	μΑ	5.0	
D023		_	50	60	μΑ	2.0	Comparator Current ⁽¹⁾ , single
		_	55	65	μΑ	3.0	comparator enabled
		_	60	75	μΑ	5.0	
D024		—	30	40	μΑ	2.0	CVREF Current ⁽¹⁾ (high range)
		_	45	60	μΑ	3.0	
		—	75	105	μΑ	5.0	
D025*		_	39	50	μΑ	2.0	CVREF Current ⁽¹⁾ (low range)
		_	59	80	μΑ	3.0	
		_	98	130	μΑ	5.0	
D026		_	5.5	10	μΑ	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		_	7.0	12	μΑ	3.0	
		_	8.5	14	μΑ	5.0	
D027			0.2	1.6	μΑ	3.0	A/D Current ⁽¹⁾ , no conversion in
			0.36	1.9	μΑ	5.0	progress

^{*} These parameters are characterized but not tested.

- Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
 - 2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

[†] Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16.6 DC Characteristics: PIC12HV609/615 - I (Industrial)

DC CHA	ARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ Ta ≤ +85°C for industrial					
Param	Davisa Charactaristics	NA:	T 1	Max	l luita		Conditions
No.	Device Characteristics	Min	Тур†	Max	Units	V DD	Note
D020	Power-down Base Current (IPD) ^(2,3)	_	135	200	μΑ	2.0	WDT, BOR, Comparator, VREF and T1OSC disabled
		_	210	280	μΑ	3.0	
	PIC12HV609/615	_	260	350	μΑ	4.5	
D021		_	135	200	μΑ	2.0	WDT Current ⁽¹⁾
		_	210	285	μΑ	3.0	
		_	265	360	μΑ	4.5	
D022		_	215	285	μΑ	3.0	BOR Current ⁽¹⁾
		_	265	360	μΑ	4.5	
D023		_	185	270	μΑ	2.0	Comparator Current ⁽¹⁾ , single
			265	350	μΑ	3.0	comparator enabled
		_	320	430	μΑ	4.5	
D024		_	165	235	μΑ	2.0	CVREF Current ⁽¹⁾ (high range)
			255	330	μΑ	3.0	
		_	330	430	μΑ	4.5	
D025*		_	175	245	μΑ	2.0	CVREF Current ⁽¹⁾ (low range)
		_	275	350	μΑ	3.0	
			355	450	μΑ	4.5	
D026			140	205	μΑ	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		_	220	290	μΑ	3.0	
		_	270	360	μΑ	4.5	
D027		_	210	280	μΑ	3.0	A/D Current ⁽¹⁾ , no conversion in
		_	260	350	μΑ	4.5	progress

^{*} These parameters are characterized but not tested.

- Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
 - 2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.
 - 3: Shunt regulator is always on and always draws operating current.

[†] Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended) (Continued)

			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$ for extended				
Param No.	Sym	Characteristic	Min	Conditions			
D101*	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	_	_	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	Сю	All I/O pins	_	_	50	pF	
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	_	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	_	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	_	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Bulk Erase/Write	4.5	_	5.5	V	
D132A	VPEW	VDD for Row Erase/Write ⁽⁶⁾	VMIN	_	5.5	V	
D133	TPEW	Erase/Write cycle time	_	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	_	_	Year	Provided no other specifications are violated

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
 - 2: Negative current is defined as current sourced by the pin.
 - 3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
 - 4: This specification applies to GP3/MCLR configured as GP3 with the internal weak pull-up disabled.
 - 5: This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/MCLR. When GP3/MCLR is configured as MCLR reset pin, the weak pull-up is always enabled.
 - 6: Applies to PIC12F617 only.

TABLE 16-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40 °C \leq TA \leq +125°C							
Param No.	Sym	Characteristics	Min	Typ†	Max	Units	Comments
CV01*	CLSB	Step Size ⁽²⁾	_ _	VDD/24 VDD/32		V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02*	CACC	Absolute Accuracy ⁽³⁾	_	_	± 1/2 ± 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03*	CR	Unit Resistor Value (R)	_	2k	_	Ω	
CV04*	Сѕт	Settling Time ⁽¹⁾	_	_	10	μS	

- * These parameters are characterized but not tested.
- † Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
- Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.
 - 2: See Section 9.10 "Comparator Voltage Reference" for more information.
 - 3: Absolute Accuracy when CVREF output is \leq (VDD -1.5).

TABLE 16-9: VOLTAGE REFERENCE SPECIFICATIONS

VR Voltage Reference Specifications				d Operati g tempera	-	tions (unle 40°C ≤ TA	ess otherwise stated) ≤ +125°C
Param No.	Symbol	Characteristics	Min	Тур	Max	Units	Comments
VR01	VP6оит	VP6 voltage output	0.5	0.6	0.7	V	
VR02	V1P2out	V1P2 voltage output	1.05	1.20	1.35	V	
VR03*	TSTABLE	Settling Time	_	10	_	μS	

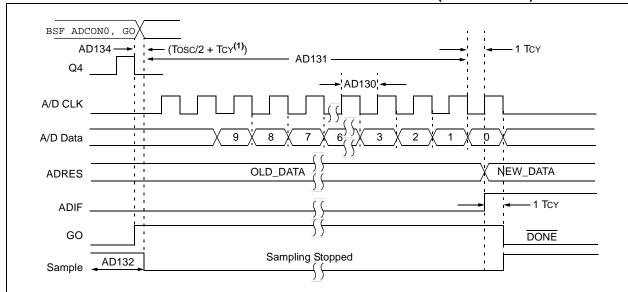
^{*} These parameters are characterized but not tested.

TABLE 16-10: SHUNT REGULATOR SPECIFICATIONS (PIC12HV609/615 only)

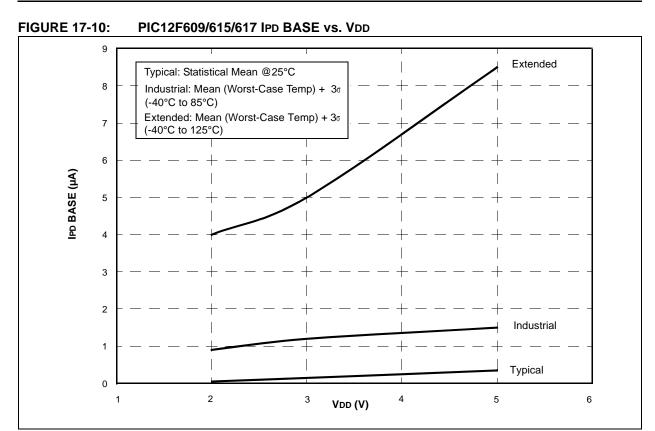
SHUNT REGULATOR CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \le \text{TA} \le +125^{\circ}\text{C}$				
Param No.	Symbol	Characteristics	Min Typ Max Units Comments				Comments
SR01	VSHUNT	Shunt Voltage	4.75	5	5.4	V	
SR02	ISHUNT	Shunt Current	4	_	50	mA	
SR03*	TSETTLE	Settling Time	_	_	150	ns	To 1% of final value
SR04	CLOAD	Load Capacitance	0.01	_	10	μF	Bypass capacitor on VDD pin
SR05	ΔISNT	Regulator operating current	_	180	_	μА	Includes band gap reference current

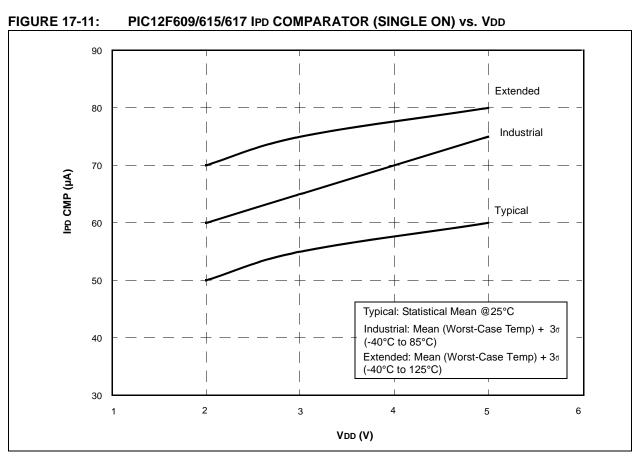
^{*} These parameters are characterized but not tested.

FIGURE 16-11: PIC12F615/617/HV615 A/D CONVERSION TIMING (SLEEP MODE)



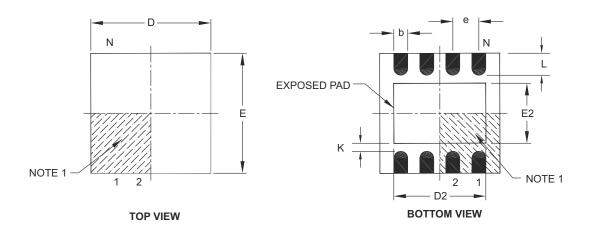
Note 1: If the A/D clock source is selected as RC, a time of TcY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

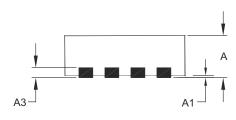


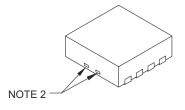


8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Units		MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	
Number of Pins	N	8			
Pitch	е	0.65 BSC			
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Length	D	3.00 BSC			
Exposed Pad Width	E2	0.00	_	1.60	
Overall Width	E	3.00 BSC			
Exposed Pad Length	D2	0.00	_	2.40	
Contact Width	b	0.25	0.30	0.35	
Contact Length	L	0.20	0.30	0.55	
Contact-to-Exposed Pad	K	0.20	_	_	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B

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