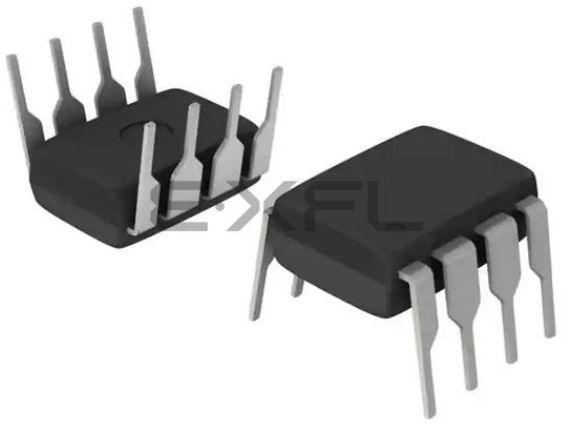

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f609-i-p

PIC12F609/615/617/12HV609/615

8-Pin Flash-Based, 8-Bit CMOS Microcontrollers

High-Performance RISC CPU:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to ±1%, typical
  - Software selectable frequency: 4 MHz or 8 MHz
- Power-Saving Sleep mode
- Voltage Range:
  - PIC12F609/615/617: 2.0V to 5.5V
  - PIC12HV609/615: 2.0V to user defined maximum **(see note)**
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT) with independent Oscillator for Reliable Operation
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High Endurance Flash:
  - 100,000 write Flash endurance
  - Flash retention: > 40 years
- Self Read/ Write Program Memory (PIC12F617 only)

Low-Power Features:

- Standby Current:
  - 50 nA @ 2.0V, typical
- Operating Current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 260 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical

Note: Voltage across the shunt regulator should not exceed 5V.

Peripheral Features:

- Shunt Voltage Regulator (PIC12HV609/615 only):
  - 5 volt regulation
  - 4 mA to 50 mA shunt range
- 5 I/O Pins and 1 Input Only
- High Current Source/Sink for Direct LED Drive
  - Interrupt-on-pin change or pins
  - Individually programmable weak pull-ups
- Analog Comparator module with:
  - One analog comparator
  - Programmable on-chip voltage reference (CV_{REF}) module (% of V_{DD})
  - Comparator inputs and output externally accessible
  - Built-In Hysteresis (software selectable)
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
  - Option to use system clock as Timer1
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

PIC12F615/617/HV615 ONLY:

- Enhanced Capture, Compare, PWM module:
  - 16-bit Capture, max. resolution 12.5 ns
  - Compare, max. resolution 200 ns
  - 10-bit PWM with 1 or 2 output channels, 1 output channel programmable “dead time,” max. frequency 20 kHz, auto-shutdown
- A/D Converter:
  - 10-bit resolution and 4 channels, samples internal voltage references
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler

1.0 DEVICE OVERVIEW

The PIC12F609/615/617/12HV609/615 devices are covered by this data sheet. They are available in 8-pin PDIP, SOIC, MSOP and DFN packages.

Block Diagrams and pinout descriptions of the devices are as follows:

- PIC12F609/HV609 (Figure 1-1, Table 1-1)
- PIC12F615/617/HV615 (Figure 1-2, Table 1-2)

FIGURE 1-1: PIC12F609/HV609 BLOCK DIAGRAM

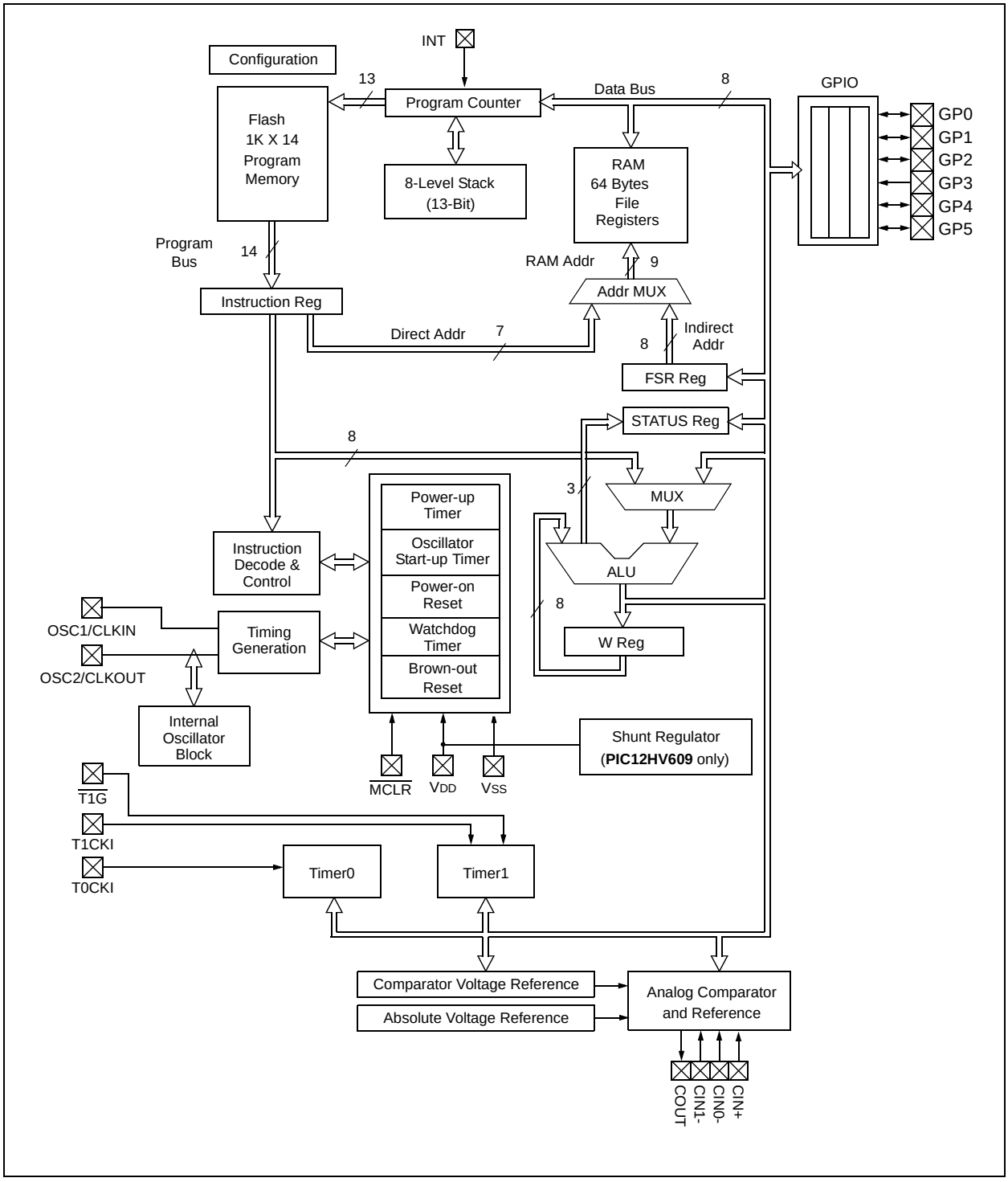


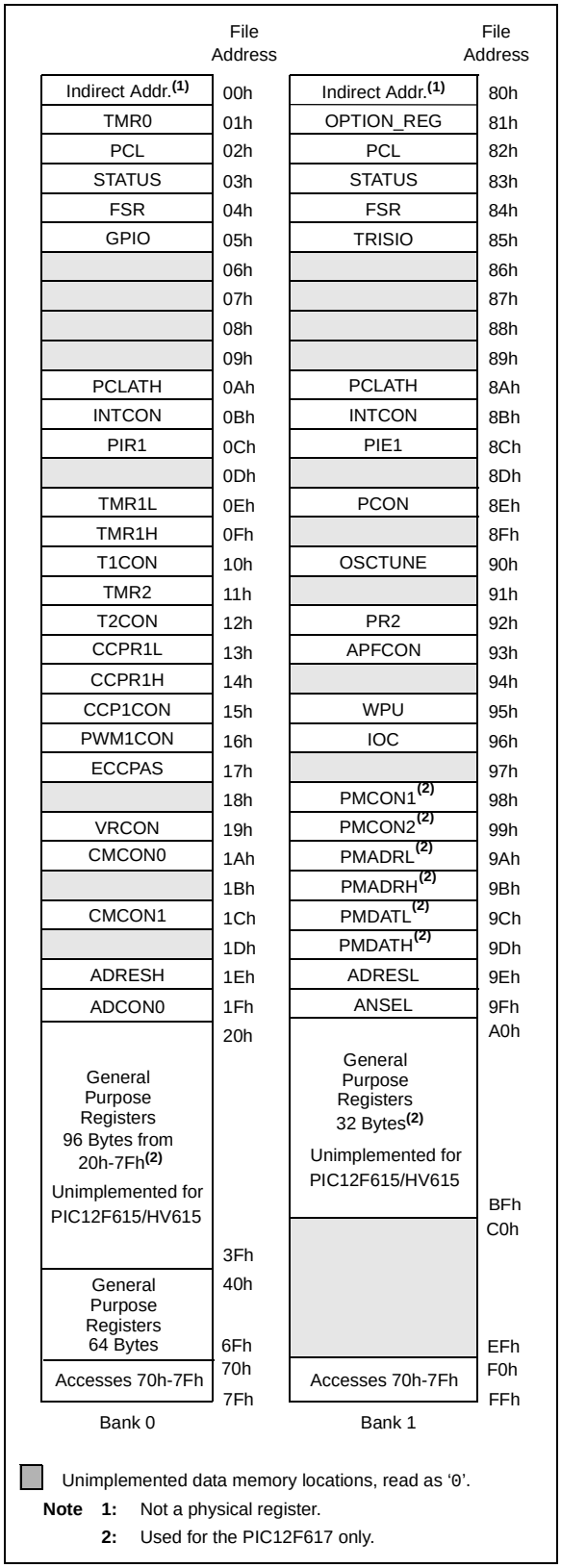
TABLE 1-2: PIC12F615/617/HV615 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/AN0/CIN+/P1B/ICSPDAT	GP0	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	CIN+	AN	—	Comparator non-inverting input
	P1B	—	CMOS	PWM output
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
GP1/AN1/CIN0-/VREF/ICSPCLK	GP1	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	CIN0-	AN	—	Comparator inverting input
	VREF	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
GP2/AN2/T0CKI/INT/COUT/CCP1/P1A	GP2	ST	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	COUT	—	CMOS	Comparator output
	CCP1	ST	CMOS	Capture input/Compare input/PWM output
	P1A	—	CMOS	PWM output
GP3/$\overline{\text{T1G}}$*/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	General purpose input with interrupt-on-change
	$\overline{\text{T1G}}$*	ST	—	Timer1 gate (count enable), alternate pin
	$\overline{\text{MCLR}}$	ST	—	Master Clear w/internal pull-up
	VPP	HV	—	Programming voltage
GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B*/OSC2/CLKOUT	GP4	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	CIN1-	AN	—	Comparator inverting input
	$\overline{\text{T1G}}$	ST	—	Timer1 gate (count enable)
	P1B*	—	CMOS	PWM output, alternate pin
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
GP5/T1CKI/P1A*/OSC1/CLKIN	GP5	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	P1A*	—	CMOS	PWM output, alternate pin
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
VDD	VDD	Power	—	Positive supply
VSS	VSS	Power	—	Ground reference

* Alternate pin function.

Legend: AN=Analog input or output CMOS=CMOS compatible input or output HV= High Voltage
ST=Schmitt Trigger input with CMOS levels TTL = TTL compatible input XTAL=Crystal

FIGURE 2-4: DATA MEMORY MAP OF THE PIC12F615/617/HV615



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: Used for the PIC12F617 only.

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External GP2/INT interrupt
- Timer0
- Weak pull-ups on GPIO

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit to '1' of the OPTION register. See **Section 6.1.3 "Software Programmable Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{GPPU}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of GP2/INT pin
0 = Interrupt on falling edge of GP2/INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on GP2/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on GP2/T0CKI pin
0 = Increment on low-to-high transition on GP2/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

4.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

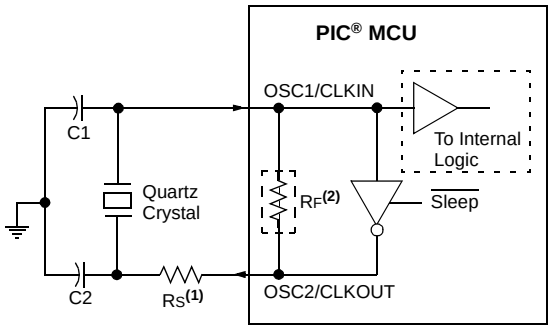
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 4-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: A series resistor (RS) may be required for quartz crystals with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

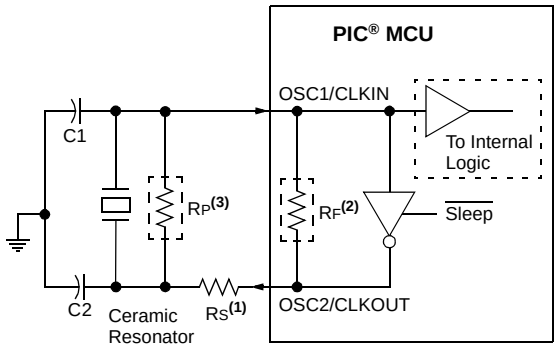
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)

FIGURE 4-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



Note 1: A series resistor (RS) may be required for ceramic resonators with low drive level.

2: The value of RF varies with the Oscillator mode selected (typically between 2 MΩ to 10 MΩ).

3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2(1)	ADCS1(1)	ADCS0(1)	ANS3	ANS2(1)	ANS1	ANS0	-000 1111	-000 1111
CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -0-0	0000 -0-0
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--u0 u000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
WPU	—	—	WPU5	WPU4	WPU3	WPU2	WPU1	WPU0	--11 1111	--11 -111
T1CON	T1GINV	TMR1GE	TICKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
CCP1CON(1)	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	0-00 0000
APFCON(1)	—	—	—	T1GSEL	—	—	P1BSEL	P1ASEL	---0 --00	---0 --00

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by GPIO.
Note 1: PIC12F615/617/HV615 only.

7.10 ECCP Special Event Trigger (PIC12F615/617/HV615 only)

If a ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 11.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)"**.

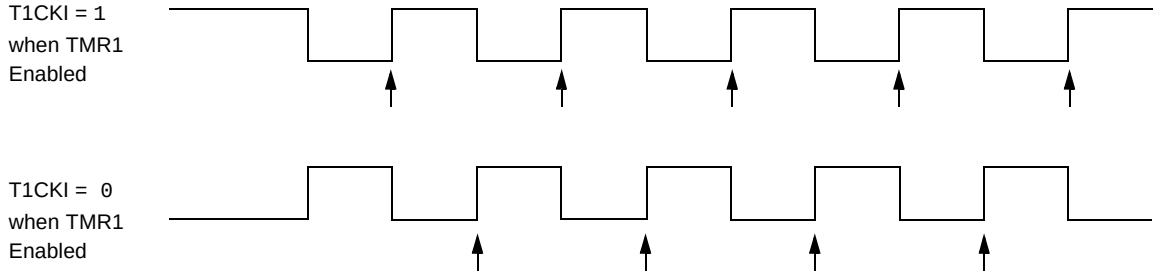
7.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 9.0 "Comparator Module"**.

FIGURE 7-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

9.3 Comparator Control

The comparator has two control and Configuration registers: CMCON0 and CMCON1. The CMCON1 register is used for controlling the interaction with Timer1 and simultaneously reading the comparator output.

The CMCON0 register (Register 9-1) contain the control and Status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity

9.3.1 COMPARATOR ENABLE

Setting the CMON bit of the CMCON0 register enables the comparator for operation. Clearing the CMON bit disables the comparator for minimum current consumption.

9.3.2 COMPARATOR INPUT SELECTION

The CMCH bit of the CMCON0 register directs one of four analog input pins to the comparator inverting input.

Note:	To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

9.3.3 COMPARATOR REFERENCE SELECTION

Setting the CMR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 9.10 "Comparator Voltage Reference"** for more information on the internal voltage reference module.

9.3.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the COUT bit of the CMCON0 register. In order to make the output available for an external connection, the following conditions must be true:

- CMOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CMON bit of the CMCON0 register must be set.

Note 1:	The CMOE bit overrides the PORT data latch. Setting the CMON has no impact on the port override.
2:	The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

9.3.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CMPOL bit of the CMCON0 register. Clearing CMPOL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-1.

TABLE 9-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CMPOL	COUT
$CMV_{IN}- > CMV_{IN}+$	0	0
$CMV_{IN}- < CMV_{IN}+$	0	1
$CMV_{IN}- > CMV_{IN}+$	1	1
$CMV_{IN}- < CMV_{IN}+$	1	0

Note: COUT refers to both the register bit and output pin.

9.4 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See **Section 16.0 "Electrical Specifications"** for more details.

TABLE 11-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	0-00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	-00- 0-00	-00- 0-00
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture.

Note 1: For PIC12F615/617/HV615 only.

12.3.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in Reset until V_{DD} has reached a high enough level for proper operation. To take advantage of the POR, simply connect the $\overline{MCLR}$ pin through a resistor to V_{DD}. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for V_{DD} is required. See **Section 16.0 "Electrical Specifications"** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until V_{DD} reaches V_{BOR} (see **Section 12.3.4 "Brown-out Reset (BOR)"**).

Note:	The POR circuit does not produce an internal Reset when V_{DD} declines. To re-enable the POR, V_{DD} must reach Vss for a minimum of 100 μs.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure proper operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Note AN607, *"Power-up Trouble Shooting"* (DS00607).

12.3.2 $\overline{MCLR}$

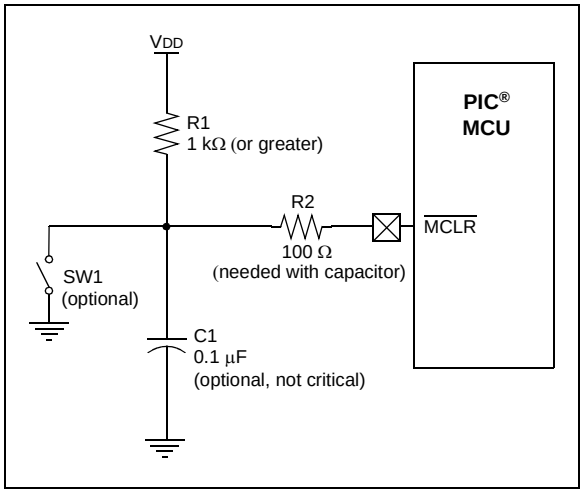
PIC12F609/615/617/12HV609/615 has a noise filter in the $\overline{MCLR}$ Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{MCLR}$ pin low.

Voltages applied to the $\overline{MCLR}$ pin that exceed its specification can result in both $\overline{MCLR}$ Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the $\overline{MCLR}$ pin no longer be tied directly to V_{DD}. The use of an RC network, as shown in Figure 12-2, is suggested.

An internal $\overline{MCLR}$ option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the GP3/$\overline{MCLR}$ pin becomes an external Reset input. In this mode, the GP3/$\overline{MCLR}$ pin has a weak pull-up to V_{DD}.

FIGURE 12-2: RECOMMENDED $\overline{MCLR}$ CIRCUIT



12.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from an internal RC oscillator. For more information, see **Section 4.4 "Internal Clock Modes"**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the V_{DD} to rise to an acceptable level. A Configuration bit, $\overline{PWRTE}$, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- V_{DD} variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 16.0 "Electrical Specifications"**).

Note:	Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

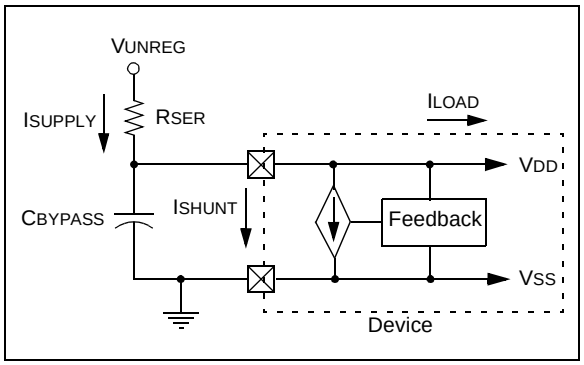
13.0 VOLTAGE REGULATOR

The PIC12HV609/HV615 devices include a permanent internal 5 volt (nominal) shunt regulator in parallel with the VDD pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the VDD pin will share the regulated supply voltage and contribute to the total VDD supply current (ILOAD).

13.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor RSER. The voltage at the VDD pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage VUNREG and the VDD of the microcontroller. See Figure 13-1 for voltage regulator schematic.

FIGURE 13-1: VOLTAGE REGULATOR



An external current limiting resistor, RSER, located between the unregulated supply, VUNREG, and the VDD pin, drops the difference in voltage between VUNREG and VDD. RSER must be between RMAX and RMIN as defined by Equation 13-1.

EQUATION 13-1: RSER LIMITING RESISTOR

$$R_{MAX} = \frac{(VU_{MIN} - 5V)}{1.05 \bullet (4\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(VU_{MAX} - 5V)}{0.95 \bullet (50\ mA)}$$

Where:

RMAX = maximum value of RSER (ohms)

RMIN = minimum value of RSER (ohms)

VUMIN = minimum value of VUNREG

VUMAX = maximum value of VUNREG

VDD = regulated voltage (5V nominal)

ILOAD = maximum expected load current in mA including I/O pin currents and external circuits connected to VDD.

1.05 = compensation for +5% tolerance of RSER

0.95 = compensation for -5% tolerance of RSER

13.2 Regulator Considerations

The supply voltage VUNREG and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for RSER must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC12HV609/HV615 devices.

The shunt regulator will still consume current when below operating voltage range for the shunt regulator.

13.3 Design Considerations

For more information on using the shunt regulator and managing current load, see Application Note AN1035, "*Designing with HV Microcontrollers"* (DS01035).

NOTES:

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Description: The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If d = 0, destination is W register. If d = 1, the destination is file register 'f' itself. d = 1 is useful to test a file register since Status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register
Z = 1

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 127$

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVW    OPTION
F
```
Before Instruction
OPTION = 0xFF
W = 0x4F
After Instruction
OPTION = 0x4F
W = 0x4F

MOVLW **Move literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Description: The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```

15.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

15.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

15.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

16.2 DC Characteristics: PIC12F609/615/617-I (Industrial) PIC12F609/615/617-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	**Supply Current (IDD)(1, 2)** PIC12F609/615/617	—	13	25	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	19	29	µA	3.0	
		—	32	51	µA	5.0	
D011*		—	135	225	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	185	285	µA	3.0	
		—	300	405	µA	5.0	
D012		—	240	360	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	360	505	µA	3.0	
		—	0.66	1.0	mA	5.0	
D013*		—	75	110	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	155	255	µA	3.0	
		—	345	530	µA	5.0	
D014		—	185	255	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	325	475	µA	3.0	
		—	0.665	1.0	mA	5.0	
D016*		—	245	340	µA	2.0	FOSC = 4 MHz INTOSC mode
		—	360	485	µA	3.0	
		—	0.620	0.845	mA	5.0	
D017		—	395	550	µA	2.0	FOSC = 8 MHz INTOSC mode
		—	0.620	0.850	mA	3.0	
		—	1.2	1.6	mA	5.0	
D018		—	175	235	µA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	285	390	µA	3.0	
		—	530	750	µA	5.0	
D019		—	2.2	3.1	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	2.8	3.35	mA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in KOhms (KΩ).

16.6 DC Characteristics: PIC12HV609/615 - I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	**Power-down Base Current (IPD)(2,3)**	—	135	200	µA	2.0	WDT, BOR, Comparator, VREF and T1OSC disabled
		—	210	280	µA	3.0	
	PIC12HV609/615	—	260	350	µA	4.5	
D021		—	135	200	µA	2.0	WDT Current(1)
		—	210	285	µA	3.0	
		—	265	360	µA	4.5	
D022		—	215	285	µA	3.0	BOR Current(1)
		—	265	360	µA	4.5	
D023		—	185	270	µA	2.0	Comparator Current(1), single comparator enabled
		—	265	350	µA	3.0	
		—	320	430	µA	4.5	
D024		—	165	235	µA	2.0	CVREF Current(1) (high range)
		—	255	330	µA	3.0	
		—	330	430	µA	4.5	
D025*		—	175	245	µA	2.0	CVREF Current(1) (low range)
		—	275	350	µA	3.0	
		—	355	450	µA	4.5	
D026		—	140	205	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	220	290	µA	3.0	
		—	270	360	µA	4.5	
D027		—	210	280	µA	3.0	A/D Current(1), no conversion in progress
		—	260	350	µA	4.5	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: Shunt regulator is always on and always draws operating current.

FIGURE 17-6: PIC12F609/615/617 IDD INTOSC (4 MHz) vs. VDD

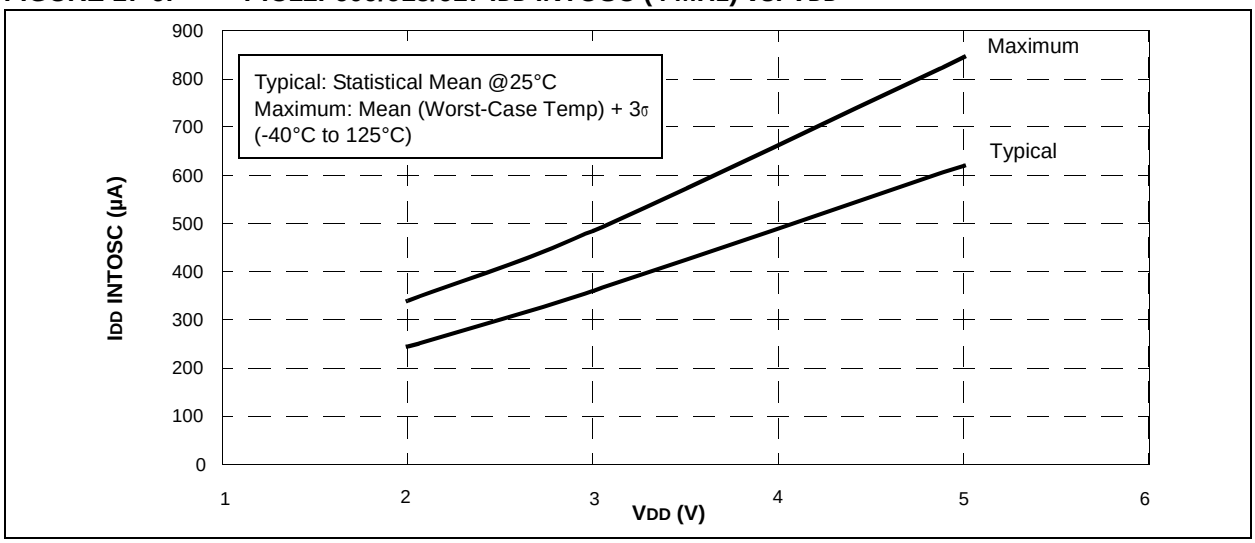


FIGURE 17-7: PIC12F609/615/617 IDD INTOSC (8 MHz) vs. VDD

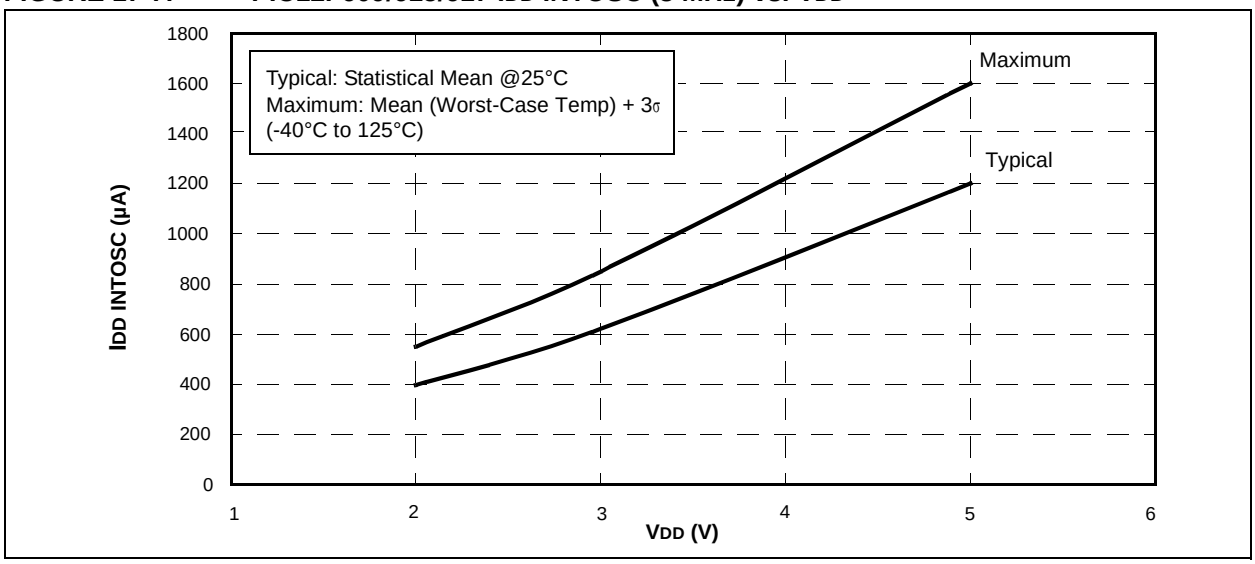


FIGURE 17-21: PIC12HV609/615 IDD XT (1 MHz) vs. VDD

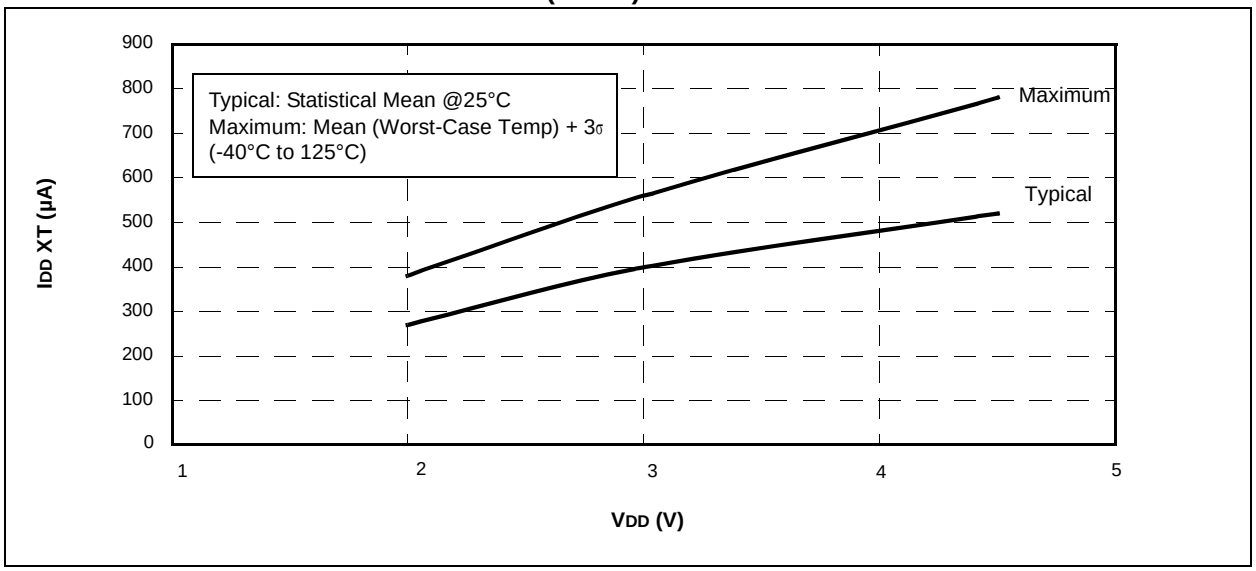


FIGURE 17-22: PIC12HV609/615 IDD XT (4 MHz) vs. VDD

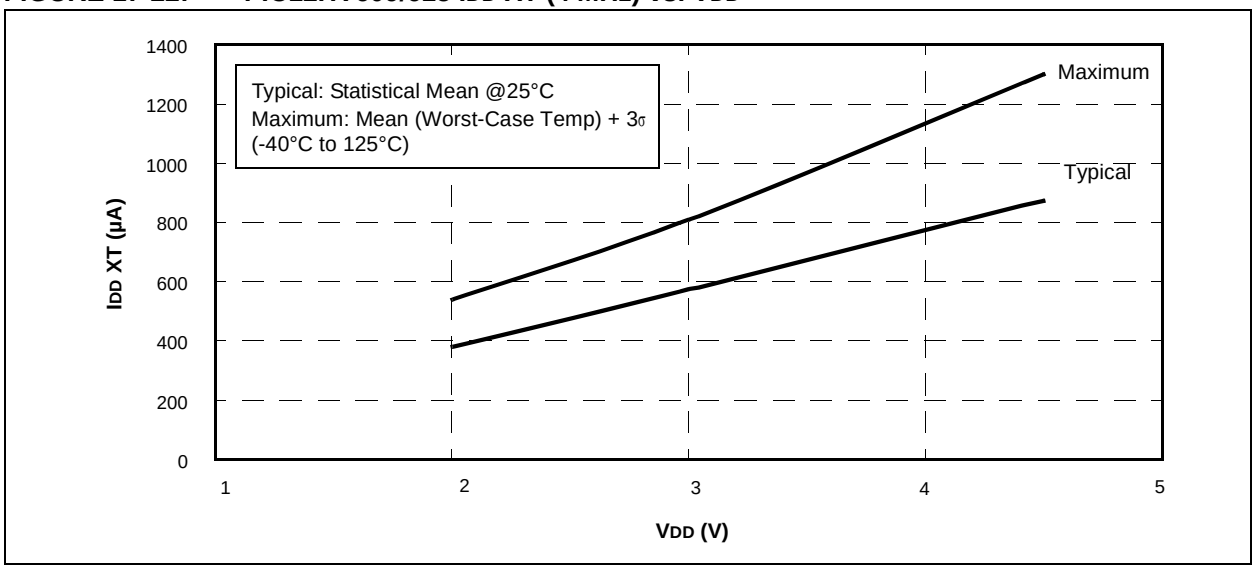
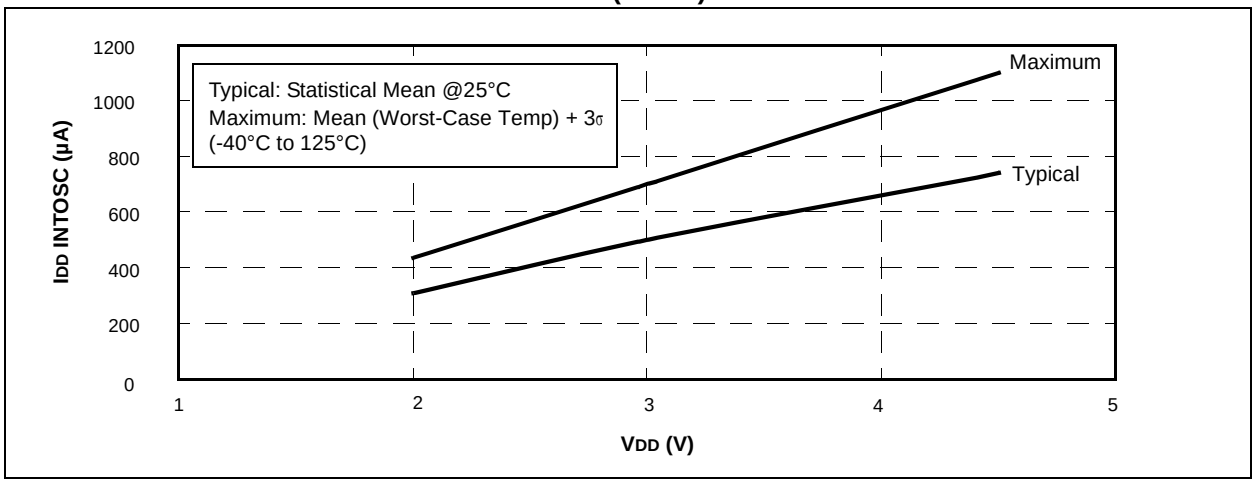
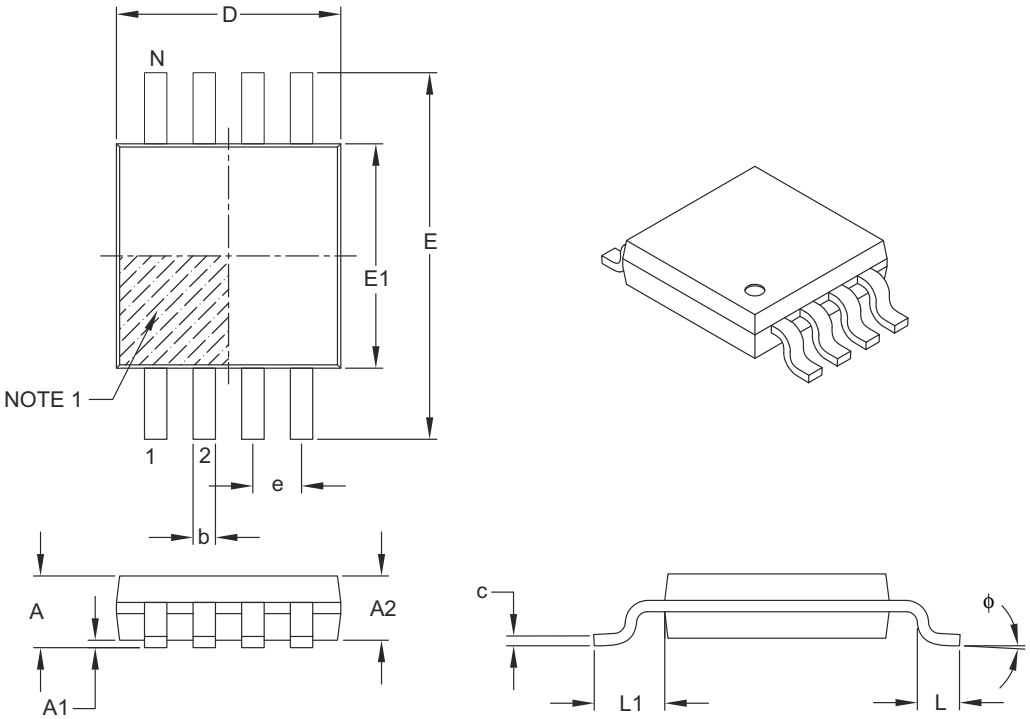


FIGURE 17-23: PIC12HV609/615 IDD INTOSC (4 MHz) vs. VDD



8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B