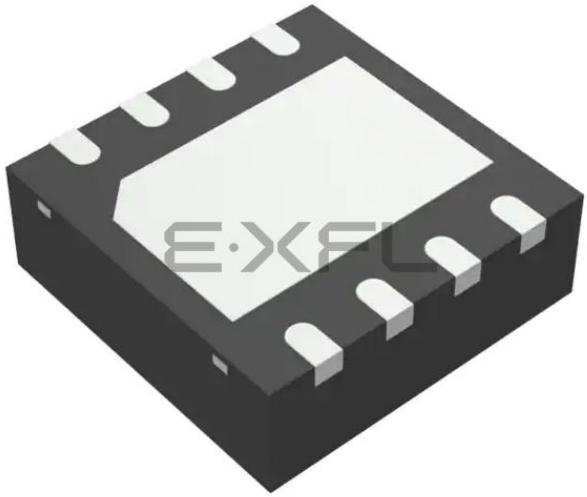

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.75KB (1K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-VDFN Exposed Pad |
| Supplier Device Package | 8-DFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12f609t-i-md |

### 2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

| | |
|---|---|
| **Note:** | Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. |

**REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** GP2/INT External Interrupt Enable bit
1 = Enables the GP2/INT external interrupt
0 = Disables the GP2/INT external interrupt

bit 3 **GPIE:** GPIO Change Interrupt Enable bit(1)
1 = Enables the GPIO change interrupt
0 = Disables the GPIO change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = Timer0 register has overflowed (must be cleared in software)
0 = Timer0 register did not overflow

bit 1 **INTF:** GP2/INT External Interrupt Flag bit
1 = The GP2/INT external interrupt occurred (must be cleared in software)
0 = The GP2/INT external interrupt did not occur

bit 0 **GPIF:** GPIO Change Interrupt Flag bit
1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software)
0 = None of the GPIO <5:0> pins have changed state

**Note 1:** IOC register must also be enabled.
**2:** T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.

An example of the complete four-word write sequence is shown in Example 3-2. The initial address is loaded into the PMADRH and PMADRL register pair; the eight words of data are loaded using indirect addressing.

**EXAMPLE 3-2: WRITING TO FLASH PROGRAM MEMORY**

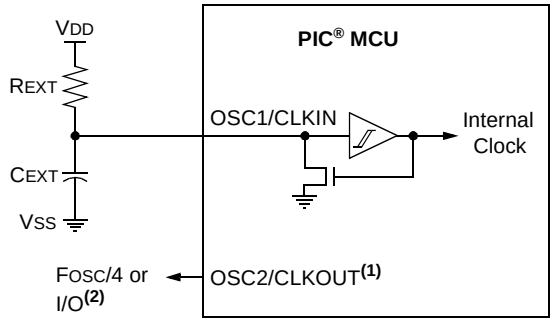
```
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ; This write routine assumes the following:
        ;     A valid starting address (the least significant bits = '00')
        ;     is loaded in ADDRH:ADDRL
        ;     ADDRH, ADDRL and DATADDR are all located in data memory
        ;
        BANKSEL  PMADRH
        MOVF     ADDRH,W      ; Load initial address
        MOVWF    PMADRH       ;
        MOVF     ADDRL,W      ;
        MOVWF    PMADRL       ;
        MOVF     DATAADDR,W   ; Load initial data address
        MOVWF    FSR          ;
LOOP    MOVF     INDF,W       ; Load first data byte into lower
        MOVWF    PMDATL       ;
        INCF     FSR,F        ; Next byte
        MOVF     INDF,W       ; Load second data byte into upper
        MOVWF    PMDATH       ;
        INCF     FSR,F        ;
        BANKSEL  PMCON1
        BSF      PMCON1,WREN  ; Enable writes
        BCF      INTCON,GIE   ; Disable interrupts (if using)
        BTFSC    INTCON,GIE   ; See AN576
        GOTO     $-2
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        ;                          Required Sequence
        MOVLW    55h          ; Start of required write sequence:
        MOVWF    PMCON2       ; Write 55h
        MOVLW    0AAh         ;
        MOVWF    PMCON2       ; Write 0AAh
        BSF      PMCON1,WR    ; Set WR bit to begin write
        NOP                   ; Required to transfer data to the buffer
        NOP                   ; registers
        ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
        BCF      PMCON1,WREN  ; Disable writes
        BSF      INTCON,GIE   ; Enable interrupts (comment out if not using interrupts)
        BANKSEL  PMADRL
        MOVF     PMADRL, W
        INCF     PMADRL,F     ; Increment address
        ANDLW    0x03         ; Indicates when sixteen words have been programmed
        SUBLW    0x03         ;   0x0F = 16 words
                              ;   0x0B = 12 words
                              ;   0x07 = 8 words
                              ;   0x03 = 4 words
        BTFSS    STATUS,Z     ; Exit on a match,
        GOTO     LOOP         ; Continue if more data needs to be written
```

### 4.3.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 4-5 shows the external RC mode connections.

**FIGURE 4-5: EXTERNAL RC MODES**




Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ, <3V
3 kΩ ≤ REXT ≤ 100 kΩ, 3-5V
CEXT > 20 pF, 2-5V

**Note 1:** Alternate pin functions are listed in **Section 1.0 "Device Overview"**.

**2:** Output depends upon RC or RCIO Clock mode.

In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

## 4.4 Internal Clock Modes

The Oscillator module provides a selectable system clock source of either 4 MHz or 8 MHz. The selectable frequency is configured through the IOSCFS bit of the Configuration Word.

The frequency of the internal oscillator can be trimmed with a calibration value in the OSCTUNE register.

### 4.4.1 INTOSC AND INTOSCIO MODES

The INTOSC and INTOSCIO modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 12.0 "Special Features of the CPU"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCIO** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

**NOTES:**

**NOTES:**

## 9.10 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- 16-level voltage range
- Output clamped to VSS
- Ratiometric with VDD
- Fixed Reference (0.6)

The VRCON register (Register 9-3) controls the Voltage Reference module shown in Register 9-6.

### 9.10.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

### 9.10.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

**EQUATION 9-1: CVREF OUTPUT VOLTAGE**

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR<3:0>/24) \times VDD$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VDD/4) + (VR<3:0> \times VDD/32)$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 9-6.

### 9.10.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- FVREN = 0

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

### 9.10.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 16.0 "Electrical Specifications"**.

### 9.10.5 FIXED VOLTAGE REFERENCE

The fixed voltage reference is independent of VDD, with a nominal output voltage of 0.6V. This reference can be enabled by setting the FVREN bit of the VRCON register to '1'. This reference is always enabled when the HFINTOSC oscillator is active.

### 9.10.6 FIXED VOLTAGE REFERENCE STABILIZATION PERIOD

When the Fixed Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See **Section 16.0 "Electrical Specifications"** for the minimum delay requirement.

### 9.10.7 VOLTAGE REFERENCE SELECTION

Multiplexers on the output of the Voltage Reference module enable selection of either the CVREF or fixed voltage reference for use by the comparators.

Setting the CMVREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by the Comparator. Clearing the CMVREN bit selects the fixed voltage for use by the Comparator.

When the CMVREN bit is cleared, current flow in the CVREF voltage divider is disabled minimizing the power drain of the voltage reference peripheral.

### 10.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

**REGISTER 10-1: ADCON0: A/D CONTROL REGISTER 0**

| R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | VCFG | — | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **VCFG:** Voltage Reference bit
1 = $V_{REF}$ pin
0 = $V_{DD}$

bit 5 **Unimplemented:** Read as '0'

bit 4-2 **CHS<2:0>: Analog Channel Select bits**
000 = Channel 00 (AN0)
001 = Channel 01 (AN1)
010 = Channel 02 (AN2)
011 = Channel 03 (AN3)
100 = $CV_{REF}$
101 = 0.6V Reference
110 = 1.2V Reference
111 = Reserved. Do not use.

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

**Note 1:** When the CHS<2:0> bits change to select the 1.2V or 0.6V reference, the reference output voltage will have a transient. If the Comparator module uses this 0.6V reference voltage, the comparator output may momentarily change state due to the transient.

## 11.0 ENHANCED CAPTURE/ COMPARE/PWM (WITH AUTO-SHUTDOWN AND DEAD BAND) MODULE (PIC12F615/617/ HV615 ONLY)

The Enhanced Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event.The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

Table 11-1 shows the timer resources required by the ECCP module.

**TABLE 11-1: ECCP MODE – TIMER RESOURCES REQUIRED**

| ECCP Mode | Timer Resource |
|---|---|
| Capture | Timer1 |
| Compare | Timer1 |
| PWM | Timer2 |

**REGISTER 11-1: CCP1CON: ENHANCED CCP1 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

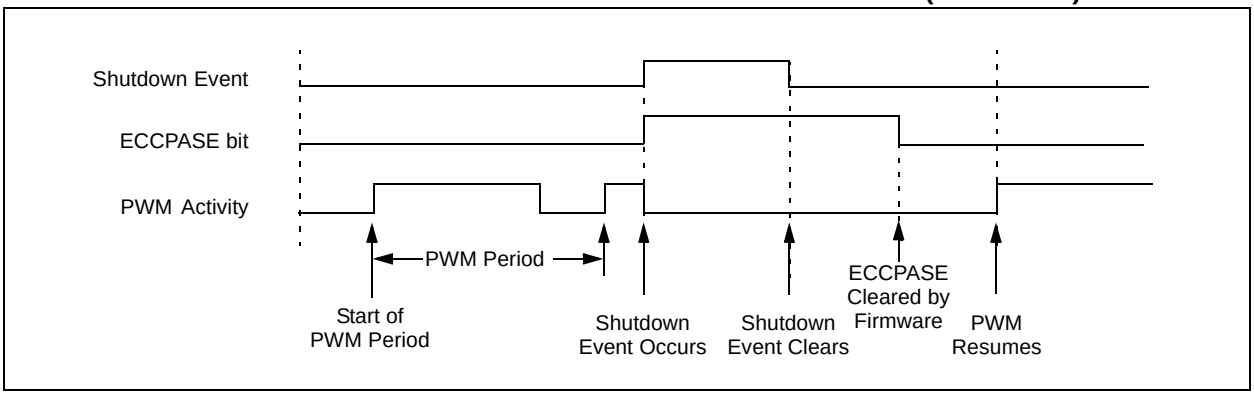
bit 7 **P1M:** PWM Output Configuration bits
If CCP1M<3:2> = 00, 01, 10:
x = P1A assigned as Capture/Compare input; P1B assigned as port pins
If CCP1M<3:2> = 11:
0 = Single output; P1A modulated; P1B assigned as port pins
1 = Half-Bridge output; P1A, P1B modulated with dead-band control

bit 6 **Unimplemented:** Read as ‘0’

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits
Capture mode:
Unused.
Compare mode:
Unused.
PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** ECCP Mode Select bits
0000 =Capture/Compare/PWM off (resets ECCP module)
0001 =Unused (reserved)
0010 =Compare mode, toggle output on match (CCP1IF bit is set)
0011 =Unused (reserved)
0100 =Capture mode, every falling edge
0101 =Capture mode, every rising edge
0110 =Capture mode, every 4th rising edge
0111 =Capture mode, every 16th rising edge
1000 =Compare mode, set output on match (CCP1IF bit is set)
1001 =Compare mode, clear output on match (CCP1IF bit is set)
1010 =Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 =Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 or TMR2 and starts an A/D conversion, if the ADC module is enabled)
1100 =PWM mode; P1A active-high; P1B active-high
1101 =PWM mode; P1A active-high; P1B active-low
1110 =PWM mode; P1A active-low; P1B active-high
1111 =PWM mode; P1A active-low; P1B active-low

**FIGURE 11-11: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)**




### 11.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

**FIGURE 11-12: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)**

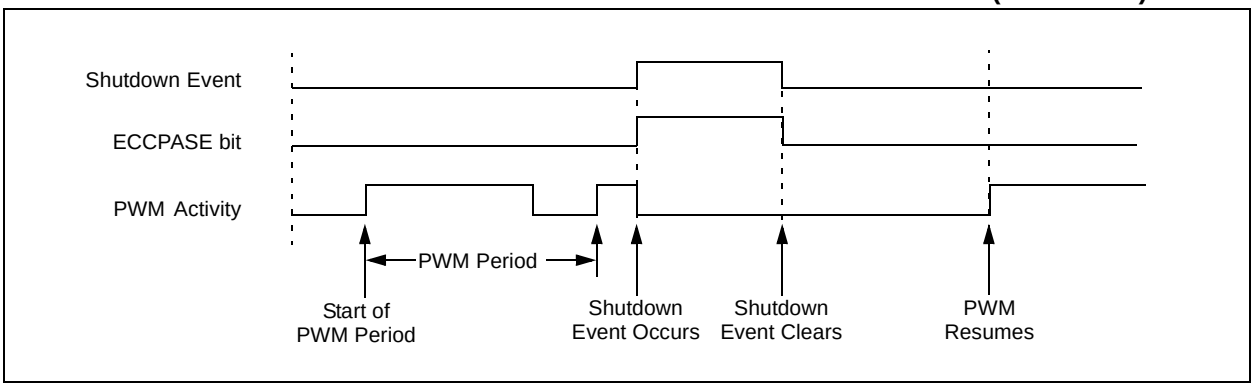


**TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS (PIC12F609/HV609)**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1) | Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out |
|---|---|---|---|---|
| W | — | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| INDF | 00h/80h | xxxx xxxx | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| PCL | 02h/82h | 0000 0000 | 0000 0000 | PC + 1(3) |
| STATUS | 03h/83h | 0001 1xxx | 000q quuu(4) | uuuq quuu(4) |
| FSR | 04h/84h | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| GPIO | 05h | --x0 x000 | --u0 u000 | --uu uuuu |
| PCLATH | 0Ah/8Ah | ---0 0000 | ---0 0000 | ---u uuuu |
| INTCON | 0Bh/8Bh | 0000 0000 | 0000 0000 | uuuu uuuu(2) |
| PIR1 | 0Ch | ----- 0--0 | ---- 0--0 | ---- u--u(2) |
| TMR1L | 0Eh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| TMR1H | 0Fh | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| T1CON | 10h | 0000 0000 | uuuu uuuu | -uuu uuuu |
| VRCON | 19h | 0-00 0000 | 0-00 0000 | u-uu uuuu |
| CMCON0 | 1Ah | 0000 -0-0 | 0000 -0-0 | uuuu -u-u |
| CMCON1 | 1Ch | ---0 0-10 | ---0 0-10 | ---u u-qu |
| OPTION_REG | 81h | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISIO | 85h | --11 1111 | --11 1111 | --uu uuuu |
| PIE1 | 8Ch | ----- 0--0 | ---- 0--0 | ---- u--u |
| PCON | 8Eh | ---- --0x | ---- --uu(1, 5) | ---- --uu |
| OSCTUNE | 90h | ---0 0000 | ---u uuuu | ---u uuuu |
| WPU | 95h | --11 -111 | --11 -111 | --uu -uuu |
| IOC | 96h | --00 0000 | --00 0000 | --uu uuuu |
| ANSEL | 9Fh | ---- 1-11 | ---- 1-11 | ---- q-qq |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 12-6 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**NOTES:**

**NOTES:**

## 16.6 DC Characteristics: PIC12HV609/615 - I (Industrial)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Device Characteristics | Min | Typ† | Max | Units | Conditions | |
| | | | | | | VDD | Note |
| D020 | **Power-down Base Current (IPD)(2,3)** | — | 135 | 200 | µA | 2.0 | WDT, BOR, Comparator, VREF and T1OSC disabled |
| | | — | 210 | 280 | µA | 3.0 | |
| | PIC12HV609/615 | — | 260 | 350 | µA | 4.5 | |
| D021 | | — | 135 | 200 | µA | 2.0 | WDT Current(1) |
| | | — | 210 | 285 | µA | 3.0 | |
| | | — | 265 | 360 | µA | 4.5 | |
| D022 | | — | 215 | 285 | µA | 3.0 | BOR Current(1) |
| | | — | 265 | 360 | µA | 4.5 | |
| D023 | | — | 185 | 270 | µA | 2.0 | Comparator Current(1), single comparator enabled |
| | | — | 265 | 350 | µA | 3.0 | |
| | | — | 320 | 430 | µA | 4.5 | |
| D024 | | — | 165 | 235 | µA | 2.0 | CVREF Current(1) (high range) |
| | | — | 255 | 330 | µA | 3.0 | |
| | | — | 330 | 430 | µA | 4.5 | |
| D025* | | — | 175 | 245 | µA | 2.0 | CVREF Current(1) (low range) |
| | | — | 275 | 350 | µA | 3.0 | |
| | | — | 355 | 450 | µA | 4.5 | |
| D026 | | — | 140 | 205 | µA | 2.0 | T1OSC Current(1), 32.768 kHz |
| | | — | 220 | 290 | µA | 3.0 | |
| | | — | 270 | 360 | µA | 4.5 | |
| D027 | | — | 210 | 280 | µA | 3.0 | A/D Current(1), no conversion in progress |
| | | — | 260 | 350 | µA | 4.5 | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

**3:** Shunt regulator is always on and always draws operating current.

**TABLE 16-2: OSCILLATOR PARAMETERS**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Freq. Tolerance** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| OS06 | TWARM | Internal Oscillator Switch when running(3) | — | — | — | 2 | TOSC | Slowest clock |
| OS07 | INTOSC | Internal Calibrated INTOSC Frequency(2) (4MHz) | ±1% | 3.96 | 4.0 | 4.04 | MHz | VDD = 3.5V, $T_A$ = 25°C |
| | | | ±2% | 3.92 | 4.0 | 4.08 | MHz | 2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C |
| | | | ±5% | 3.80 | 4.0 | 4.2 | MHz | 2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.) |
| OS08 | INTOSC | Internal Calibrated INTOSC Frequency(2) (8MHz) | ±1% | 7.92 | 8.0 | 8.08 | MHz | VDD = 3.5V, $T_A$ = 25°C |
| | | | ±2% | 7.84 | 8.0 | 8.16 | MHz | 2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C |
| | | | ±5% | 7.60 | 8.0 | 8.40 | MHz | 2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.) |
| OS10* | TIOSC ST | INTOSC Oscillator Wake-up from Sleep Start-up Time | — | 5.5 | 12 | 24 | µs | VDD = 2.0V, -40°C to +85°C |
| | | | — | 3.5 | 7 | 14 | µs | VDD = 3.0V, -40°C to +85°C |
| | | | — | 3 | 6 | 11 | µs | VDD = 5.0V, -40°C to +85°C |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

**3:** By design.

**FIGURE 16-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS**

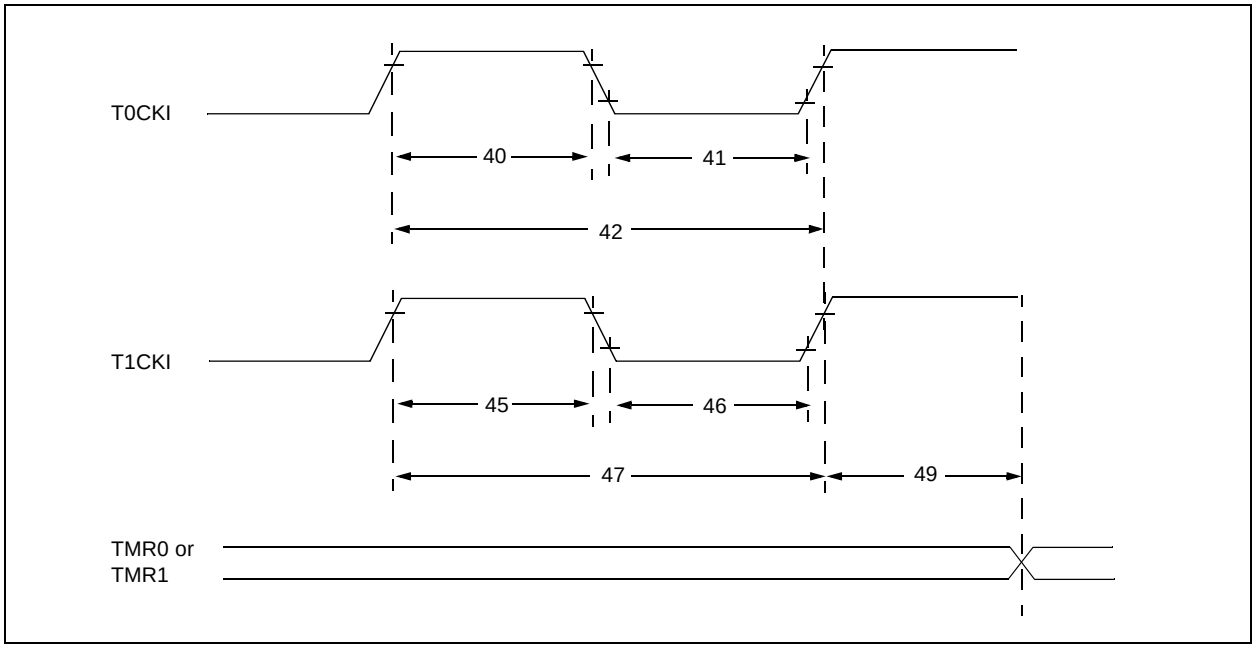



**TABLE 16-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40* | TT0H | T0CKI High Pulse Width | No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | With Prescaler | 10 | — | — | ns | |
| 41* | TT0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | With Prescaler | 10 | — | — | ns | |
| 42* | TT0P | T0CKI Period | | Greater of: 20 or TCY + 40 / N | — | — | ns | N = prescale value (2, 4, ..., 256) |
| 45* | TT1H | T1CKI High Time | Synchronous, No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | Synchronous, with Prescaler | 15 | — | — | ns | |
| | | | Asynchronous | 30 | — | — | ns | |
| 46* | TT1L | T1CKI Low Time | Synchronous, No Prescaler | 0.5 TCY + 20 | — | — | ns | |
| | | | Synchronous, with Prescaler | 15 | — | — | ns | |
| | | | Asynchronous | 30 | — | — | ns | |
| 47* | TT1P | T1CKI Input Period | Synchronous | Greater of: 30 or TCY + 40 / N | — | — | ns | N = prescale value (1, 2, 4, 8) |
| | | | Asynchronous | 60 | — | — | ns | |
| 48 | FT1 | Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN) | | — | 32.768 | — | kHz | |
| 49* | TCKEZTMR1 | Delay from External Clock Edge to Timer Increment | | 2 TOSC | — | 7 TOSC | — | Timers in Sync mode |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 17-8: PIC12F609/615617 IDD EXTRC (4 MHz) vs. VDD**

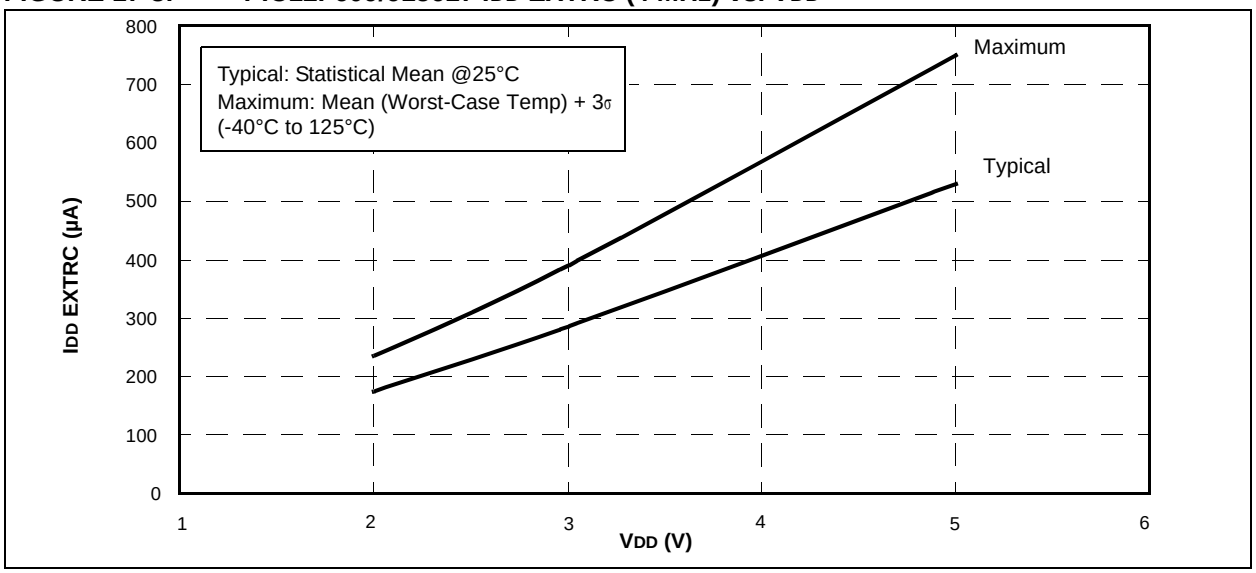



**FIGURE 17-9: PIC12F609/615/617 IDD HS (20 MHz) vs. VDD**

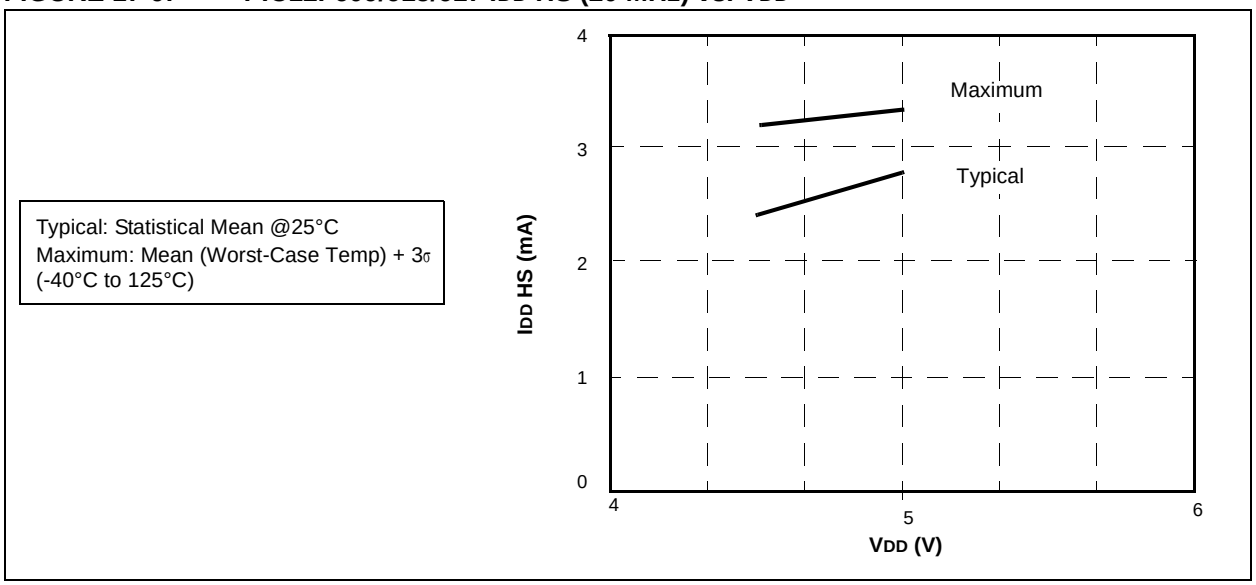


**FIGURE 17-10: PIC12F609/615/617 IPD BASE vs. VDD**

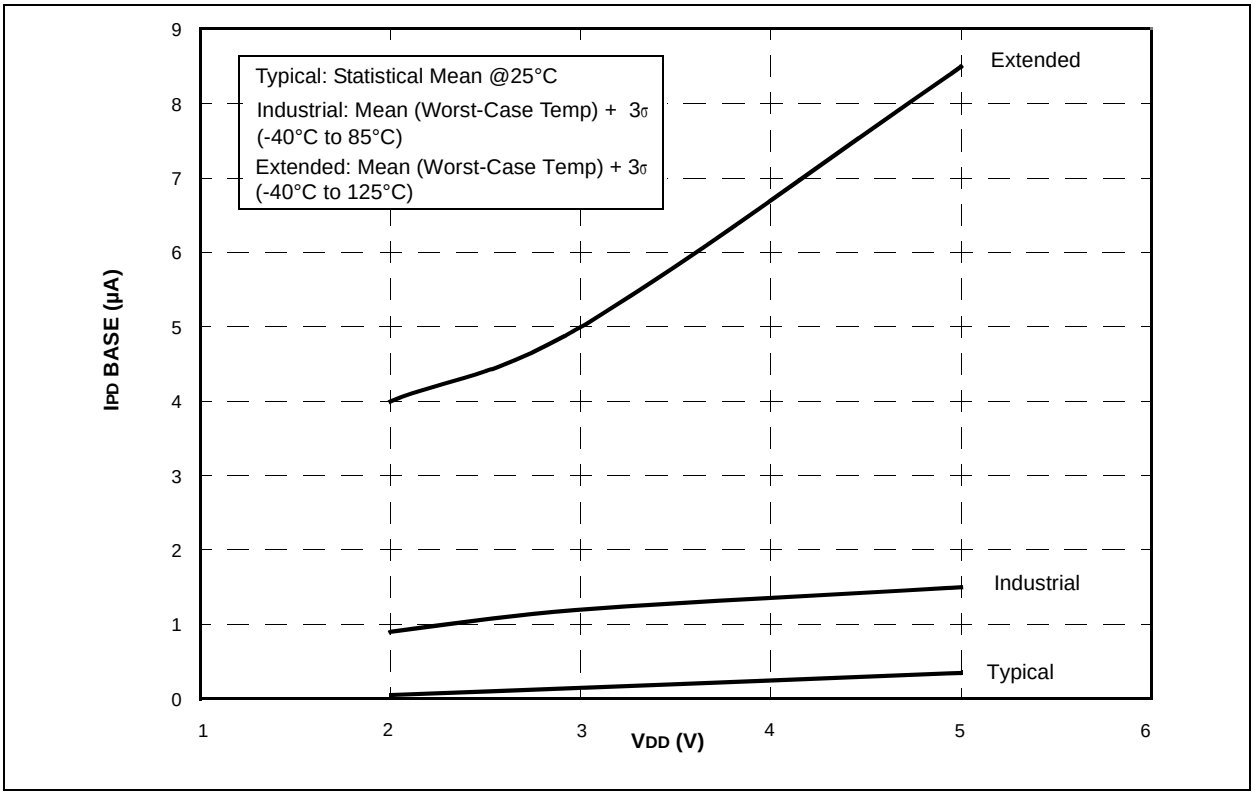



**FIGURE 17-11: PIC12F609/615/617 IPD COMPARATOR (SINGLE ON) vs. VDD**

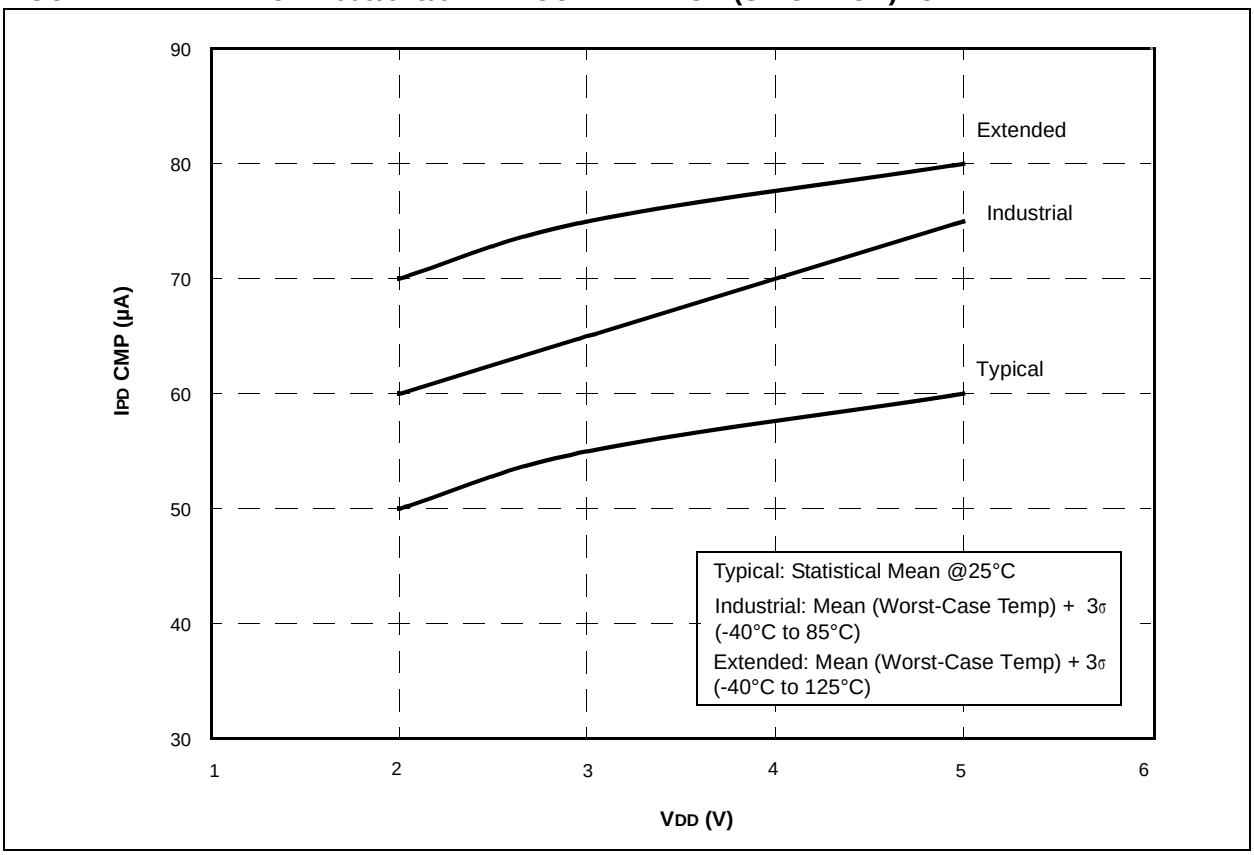


**FIGURE 17-43: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (25°C)**

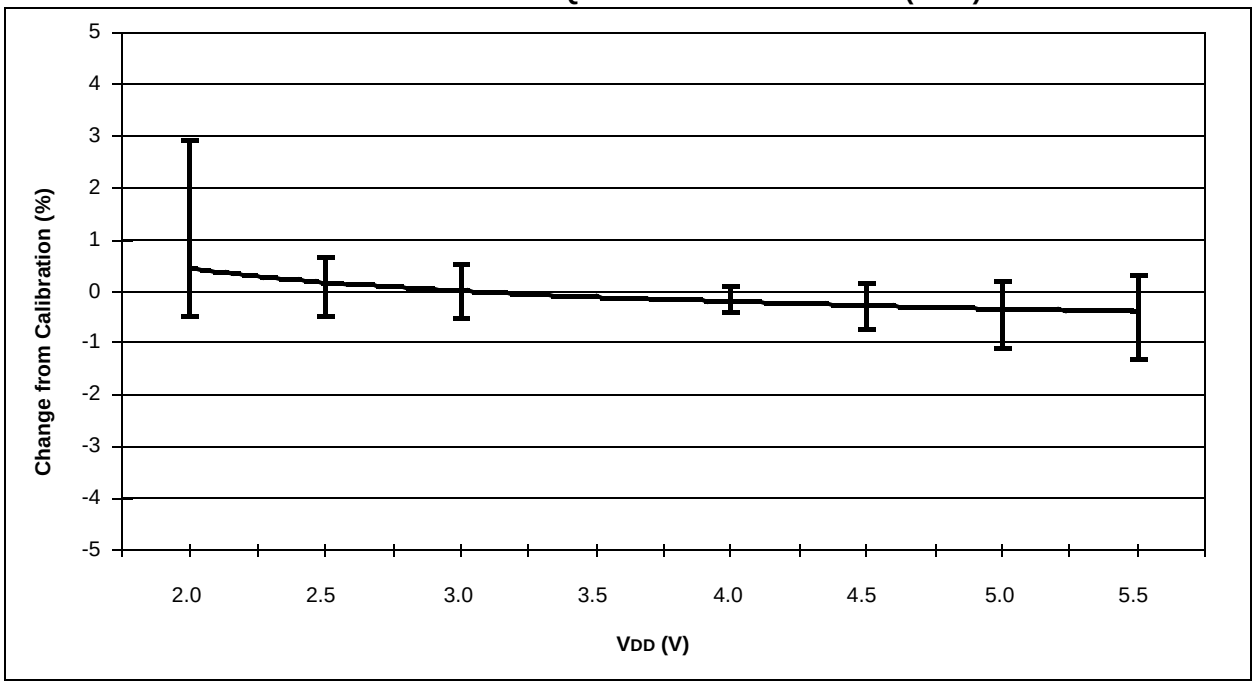
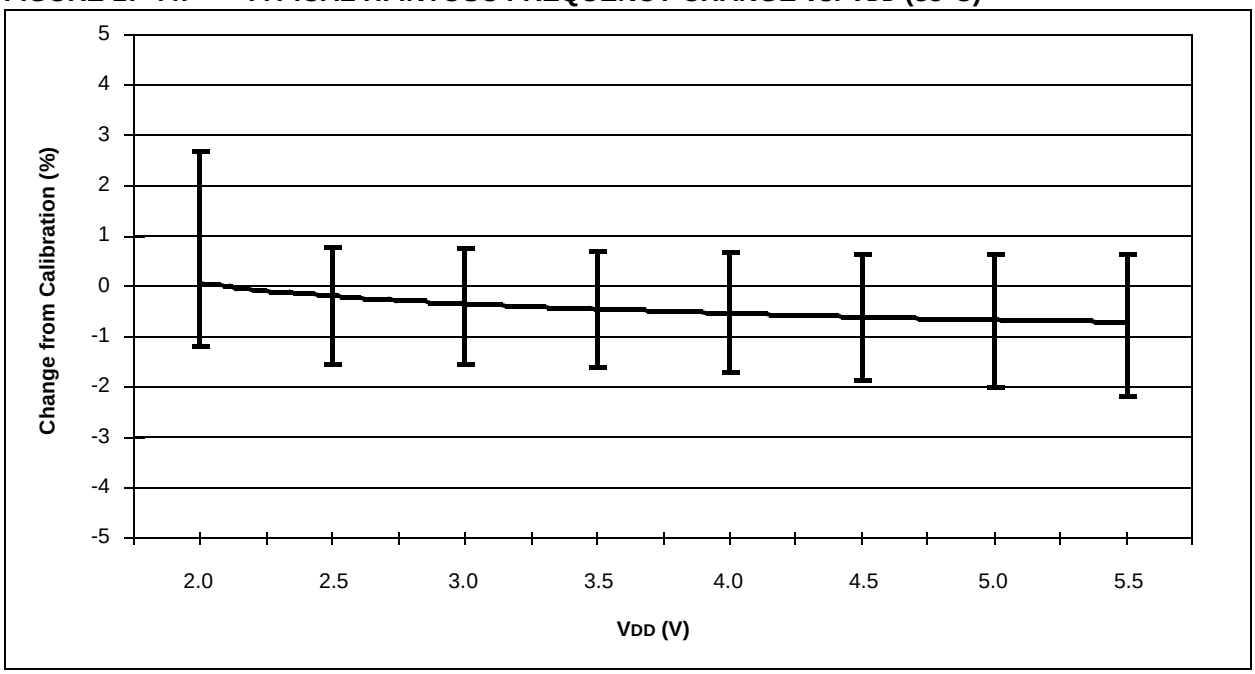



**FIGURE 17-44: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (85°C)**



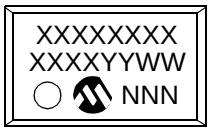
## 18.0 PACKAGING INFORMATION

### 18.1 Package Marking Information

8-Lead PDIP (.300”)


Example


8-Lead SOIC (.150”)



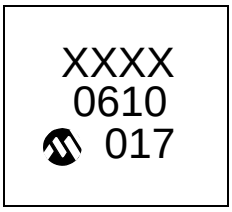

Example


8-Lead MSOP

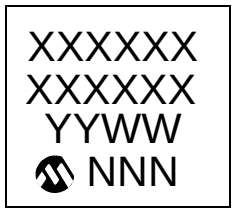

Example


8-Lead DFN (3x3 mm)

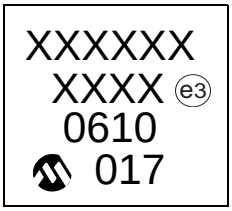

Example




8-Lead DFN (4x4 mm) (for PIC12F609/615/HV609/615 devices only)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ( ) (e3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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