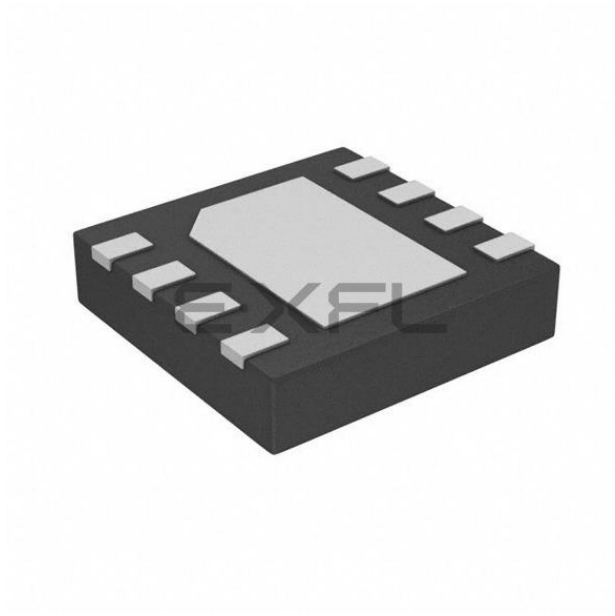

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 5 |
| Program Memory Size | 1.75KB (1K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 8-VDFN Exposed Pad |
| Supplier Device Package | 8-DFN (3x3) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12f609t-i-mf |

### 2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- Timer0/WDT prescaler
- External GP2/INT interrupt
- Timer0
- Weak pull-ups on GPIO

**Note:** To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit to '1' of the OPTION register. See **Section 6.1.3 "Software Programmable Prescaler"**.

**REGISTER 2-2: OPTION_REG: OPTION REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{GPPU}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **$\overline{GPPU}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of GP2/INT pin
0 = Interrupt on falling edge of GP2/INT pin

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on GP2/T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on GP2/T0CKI pin
0 = Increment on low-to-high transition on GP2/T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

| BIT VALUE | TIMER0 RATE | WDT RATE |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

### 2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

| | |
|---|---|
| **Note:** | Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. |

**REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** GP2/INT External Interrupt Enable bit
1 = Enables the GP2/INT external interrupt
0 = Disables the GP2/INT external interrupt

bit 3 **GPIE:** GPIO Change Interrupt Enable bit(1)
1 = Enables the GPIO change interrupt
0 = Disables the GPIO change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = Timer0 register has overflowed (must be cleared in software)
0 = Timer0 register did not overflow

bit 1 **INTF:** GP2/INT External Interrupt Flag bit
1 = The GP2/INT external interrupt occurred (must be cleared in software)
0 = The GP2/INT external interrupt did not occur

bit 0 **GPIF:** GPIO Change Interrupt Flag bit
1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software)
0 = None of the GPIO <5:0> pins have changed state

**Note 1:** IOC register must also be enabled.
**2:** T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.

### 2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset ($\overline{POR}$)
- Brown-out Reset ($\overline{BOR}$)
- Watchdog Timer Reset (WDT)
- External $\overline{MCLR}$ Reset

The PCON register also controls the software enable of the $\overline{BOR}$.

The PCON register bits are shown in Register 2-6.

**REGISTER 2-6: PCON: POWER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0(1) |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | $\overline{POR}$ | $\overline{BOR}$ |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
1 = No Power-on Reset occurred
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
1 = No Brown-out Reset occurred
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

**Note 1:** Reads as '0' if Brown-out Reset is disabled.

### 5.2.4 PIN DESCRIPTIONS AND DIAGRAMS

Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the Comparator or the ADC, refer to the appropriate section in this data sheet.

#### 5.2.4.1 GP0/AN0(1)/CIN+/P1B(1)/ICSPDAT

Figure 5-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog non-inverting input to the comparator
- a PWM output(1)
- In-Circuit Serial Programming data

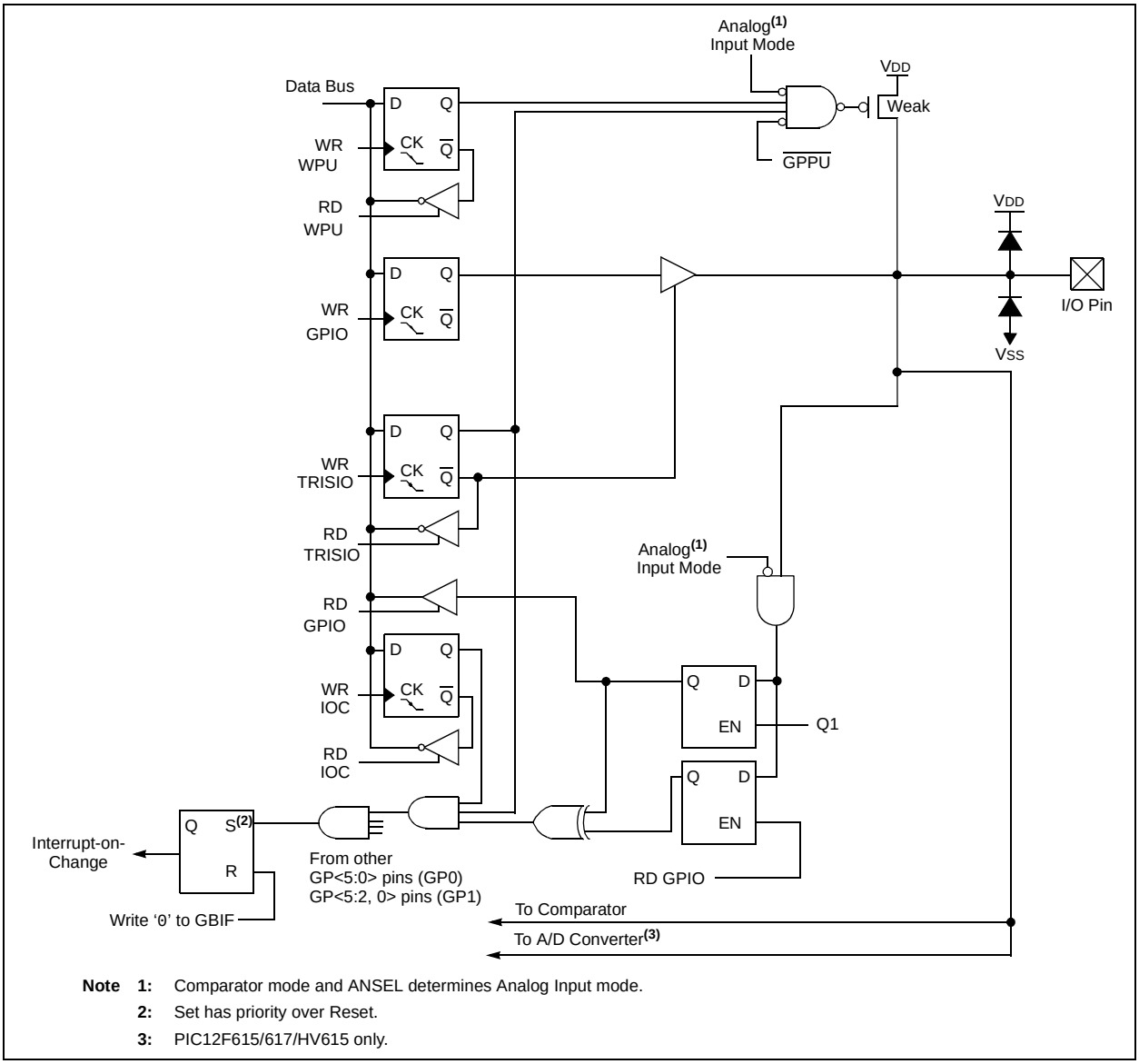
#### 5.2.4.2 GP1/AN1(1)/CIN0-/VREF(1)/ICSPCLK

Figure 5-1 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- an analog inverting input to the comparator
- a voltage reference input for the ADC(1)
- In-Circuit Serial Programming clock

**Note 1:** PIC12F615/617/HV615 only.

**FIGURE 5-1: BLOCK DIAGRAM OF GP<1:0>**




**Note 1:** Comparator mode and ANSEL determines Analog Input mode.
**2:** Set has priority over Reset.
**3:** PIC12F615/617/HV615 only.

**TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ANSEL | — | ADCS2(1) | ADCS1(1) | ADCS0(1) | ANS3 | ANS2(1) | ANS1 | ANS0 | -000 1111 | -000 1111 |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 0000 -0-0 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| IOC | — | — | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | --00 0000 | --00 0000 |
| OPTION_REG | $\overline{\text{GPPU}}$ | INTEDG | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --u0 u000 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |
| WPU | — | — | WPU5 | WPU4 | WPU3 | WPU2 | WPU1 | WPU0 | --11 1111 | --11 -111 |
| T1CON | T1GINV | TMR1GE | TICKPS1 | T1CKPS0 | T1OSCEN | $\overline{\text{T1SYNC}}$ | TMR1CS | TMR1ON | 0000 0000 | uuuu uuuu |
| CCP1CON(1) | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 0-00 0000 |
| APFCON(1) | — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL | ---0 --00 | ---0 --00 |

**Legend:** x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by GPIO.
**Note 1:** PIC12F615/617/HV615 only.

## 7.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or $\overline{T1G}$ pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Time base for the Capture/Compare function
- Special Event Trigger (with ECCP)
- Comparator output synchronization to Timer1 clock

Figure 7-1 is a block diagram of the Timer1 module.

### 7.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

### 7.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is FOSC/4. When TMR1CS = 1, the clock source is supplied externally.

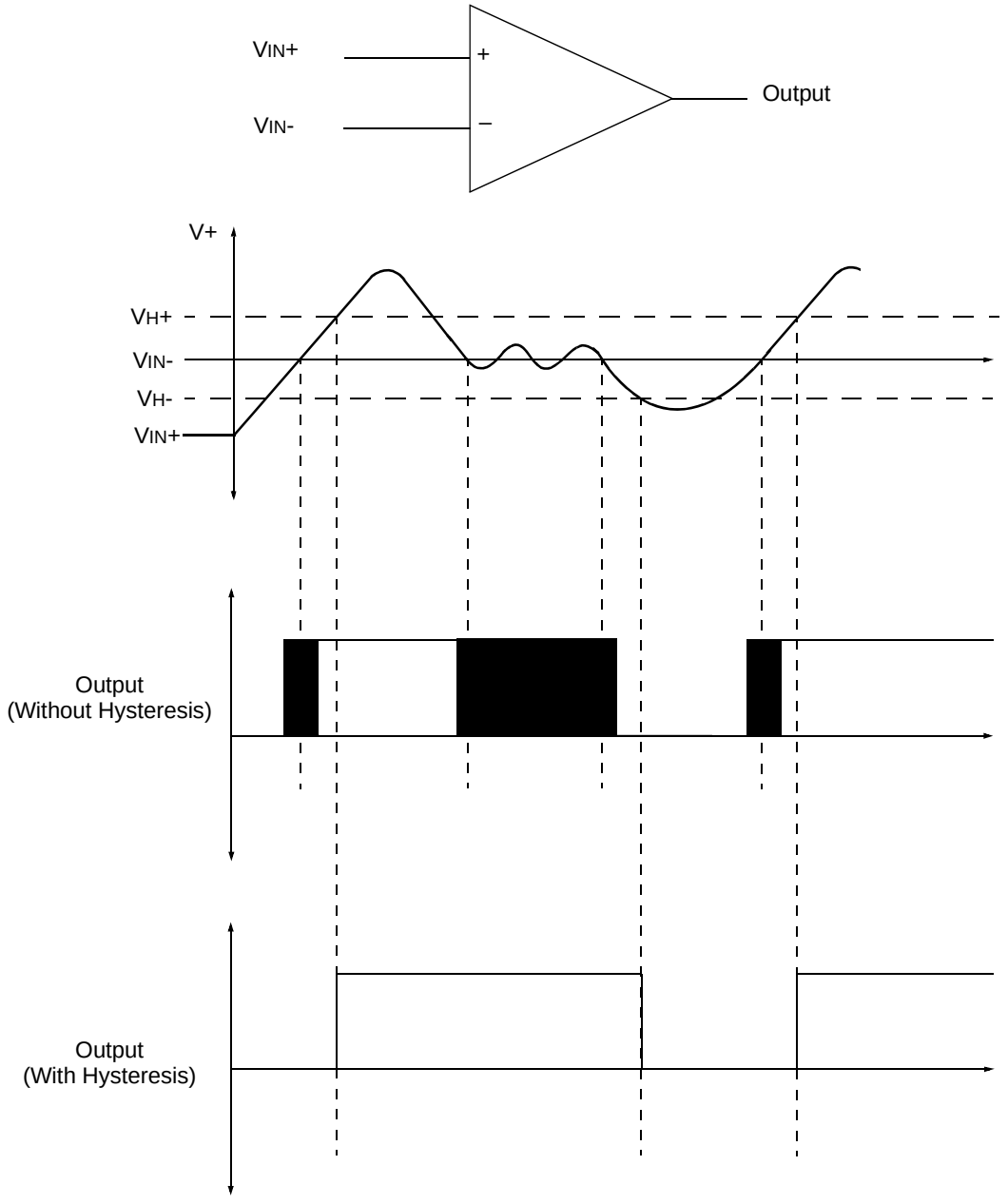
| Clock Source | TMR1CS | T1ACS |
|---|---|---|
| FOSC/4 | 0 | 0 |
| FOSC | 0 | 1 |
| T1CKI pin | 1 | x |

## 9.11 Comparator Hysteresis

Each comparator has built-in hysteresis that is user enabled by setting the CMHYS bit of the CMCON1 register. The hysteresis feature can help filter noise and reduce multiple comparator output transitions when the output is changing state.

Figure 9-7 shows the relationship between the analog input levels and digital output of a comparator with and without hysteresis. The output of the comparator changes from a low state to a high state only when the analog voltage at VIN+ rises above the upper hysteresis threshold (VH+). The output of the comparator changes from a high state to a low state only when the analog voltage at VIN+ falls below the lower hysteresis threshold (VH-).

**FIGURE 9-7: COMPARATOR HYSTERESIS**




**Note:** The black areas of the comparator output represents the uncertainty due to input offsets and response time.

**TABLE 9-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| ANSEL | — | ADCS2(1) | ADCS1(1) | ADCS0(1) | ANS3 | ANS2(1) | ANS1 | ANS0 | -000 1111 | -000 1111 |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -000 | 0000 -000 |
| CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | 0000 0000 | 0000 0000 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 000x | 0000 000x |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |
| VRCON | CMVREN | — | VRR | FVREN | VR3 | VR2 | VR1 | VR0 | 0-00 0000 | 0-00 0000 |

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

**Note 1:** For PIC12F615/617/HV615 only.

### 11.4.2 START-UP CONSIDERATIONS

When any PWM mode is used, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins.

| | |
|---|---|
| **Note:** | When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the OFF state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s). |

The CCP1M<1:0> bits of the CCP1CON register allow the user to choose whether the PWM output signals are active-high or active-low for each PWM output pin (P1A and P1B). The PWM output polarities must be selected before the PWM pin output drivers are enabled. Changing the polarity configuration while the PWM pin output drivers are enable is not recommended since it may result in damage to the application circuits.

The P1A and P1B output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pin output drivers at the same time as the Enhanced PWM modes may cause damage to the application circuit. The Enhanced PWM modes must be enabled in the proper Output mode and complete a full PWM cycle before configuring the PWM pin output drivers. The completion of a full PWM cycle is indicated by the TMR2IF bit of the PIR1 register being set as the second PWM period begins.

### 11.4.3 OPERATION DURING SLEEP

When the device is placed in sleep, the allocated timer will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, it will continue from this state.

**REGISTER 11-3: PWM1CON: ENHANCED PWM CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **PRSEN:** PWM Restart Enable bit

1 = Upon auto-shutdown, the ECCPASE bit clears automatically once the shutdown event goes away; the PWM restarts automatically

0 = Upon auto-shutdown, ECCPASE must be cleared in software to restart the PWM

bit 6-0 **PDC<6:0>:** PWM Delay Count bits

PDCn =Number of FOSC/4 (4 * TOSC) cycles between the scheduled time when a PWM signal **should** transition active and the **actual** time it transitions active

**TABLE 11-7: SUMMARY OF REGISTERS ASSOCIATED WITH PWM**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| APFCON | — | — | — | T1GSEL | — | — | P1BSEL | P1ASEL | ---0 --00 | ---0 --00 |
| CCP1CON(1) | P1M | — | DC1B1 | DC1B0 | CCP1M3 | CCP1M2 | CCP1M1 | CCP1M0 | 0-00 0000 | 0-00 0000 |
| CCPR1L(1) | Capture/Compare/PWM Register 1 Low Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| CCPR1H(1) | Capture/Compare/PWM Register 1 High Byte | | | | | | | | xxxx xxxx | uuuu uuuu |
| CMCON0 | CMON | COUT | CMOE | CMPOL | — | CMR | — | CMCH | 0000 -0-0 | 0000 -0-0 |
| CMCON1 | — | — | — | T1ACS | CMHYS | — | T1GSS | CMSYNC | ---0 0-10 | ---0 0-10 |
| ECCPAS(1) | ECCPASE | ECCPAS2 | ECCPAS1 | ECCPAS0 | PSSAC1 | PSSAC0 | PSSBD1 | PSSBD0 | 0000 0000 | 0000 0000 |
| PWM1CON | PRSEN | PDC6 | PDC5 | PDC4 | PDC3 | PDC2 | PDC1 | PDC0 | 0000 0000 | 0000 0000 |
| INTCON | GIE | PEIE | T0IE | INTE | GPIE | T0IF | INTF | GPIF | 0000 0000 | 0000 0000 |
| PIE1 | — | ADIE(1) | CCP1IE(1) | — | CMIE | — | TMR2IE(1) | TMR1IE | -00- 0-00 | -00- 0-00 |
| PIR1 | — | ADIF(1) | CCP1IF(1) | — | CMIF | — | TMR2IF(1) | TMR1IF | -00- 0-00 | -00- 0-00 |
| T2CON(1) | — | TOUTPS3 | TOUTPS2 | TOUTPS1 | TOUTPS0 | TMR2ON | T2CKPS1 | T2CKPS0 | -000 0000 | -000 0000 |
| TMR2(1) | Timer2 Module Register | | | | | | | | 0000 0000 | 0000 0000 |
| TRISIO | — | — | TRISIO5 | TRISIO4 | TRISIO3 | TRISIO2 | TRISIO1 | TRISIO0 | --11 1111 | --11 1111 |

**Legend:** - = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the PWM.

**Note 1:** For PIC12F615/617/HV615 only.

## 14.0 INSTRUCTION SET SUMMARY

The PIC12F609/615/617/12HV609/615 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode,** which specifies the instruction type and one or more **operands,** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 14-1, while the various opcode fields are summarized in Table 14-1.

Table 14-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

### 14.1 Read-Modify-Write Operations

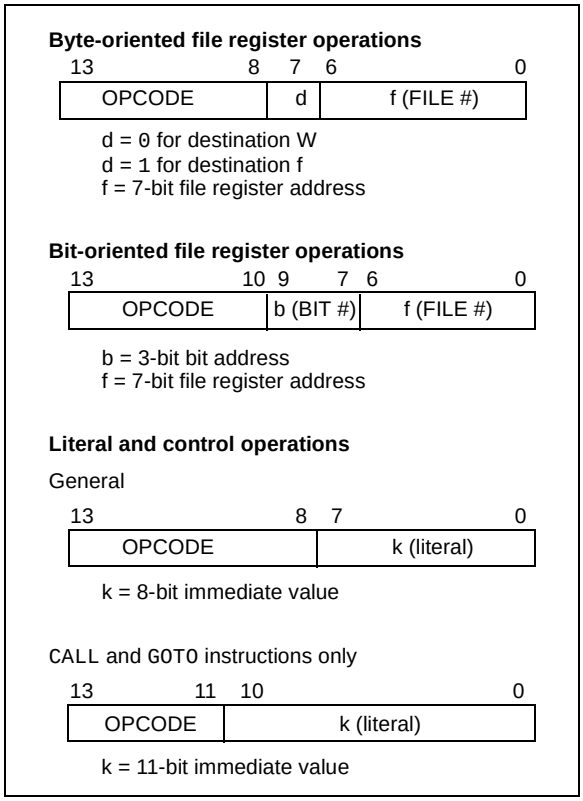
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified, and the result is stored according to either the instruction or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF GPIO instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended consequence of clearing the condition that set the GPIF flag.

**TABLE 14-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1).<br>The assembler will generate code with x = 0.<br>It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select; d = 0: store result in W,<br>d = 1: store result in file register f.<br>Default is d = 1. |
| PC | Program Counter |
| $\overline{TO}$ | Time-out bit |
| C | Carry bit |
| DC | Digit carry bit |
| Z | Zero bit |
| $\overline{PD}$ | Power-down bit |

**FIGURE 14-1: GENERAL FORMAT FOR INSTRUCTIONS**



## 16.5 DC Characteristics: PIC12F609/615/617 - E (Extended)

| DC CHARACTERISTICS | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Device Characteristics | Min | Typ† | Max | Units | Conditions | |
| | | | | | | VDD | Note |
| D020E | **Power-down Base Current (IPD)(2)** PIC12F609/615/617 | — | 0.05 | 4.0 | µA | 2.0 | WDT, BOR, Comparator, VREF and T1OSC disabled |
| | | — | 0.15 | 5.0 | µA | 3.0 | |
| | | — | 0.35 | 8.5 | µA | 5.0 | |
| D021E | | — | 0.5 | 5.0 | µA | 2.0 | WDT Current(1) |
| | | — | 2.5 | 8.0 | µA | 3.0 | |
| | | — | 9.5 | 19 | µA | 5.0 | |
| D022E | | — | 5.0 | 15 | µA | 3.0 | BOR Current(1) |
| | | — | 6.0 | 19 | µA | 5.0 | |
| D023E | | — | 50 | 70 | µA | 2.0 | Comparator Current(1), single comparator enabled |
| | | — | 55 | 75 | µA | 3.0 | |
| | | — | 60 | 80 | µA | 5.0 | |
| D024E | | — | 30 | 40 | µA | 2.0 | CVREF Current(1) (high range) |
| | | — | 45 | 60 | µA | 3.0 | |
| | | — | 75 | 105 | µA | 5.0 | |
| D025E* | | — | 39 | 50 | µA | 2.0 | CVREF Current(1) (low range) |
| | | — | 59 | 80 | µA | 3.0 | |
| | | — | 98 | 130 | µA | 5.0 | |
| D026E | | — | 5.5 | 16 | µA | 2.0 | T1OSC Current(1), 32.768 kHz |
| | | — | 7.0 | 18 | µA | 3.0 | |
| | | — | 8.5 | 22 | µA | 5.0 | |
| D027E | | — | 0.2 | 6.5 | µA | 3.0 | A/D Current(1), no conversion in progress |
| | | — | 0.36 | 10 | µA | 5.0 | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

**2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

## 16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial<br>-40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| | | I/O port: | | | | | |
| D030 | | with TTL buffer | Vss | — | 0.8 | V | 4.5V ≤ VDD ≤ 5.5V |
| D030A | | | Vss | — | 0.15 VDD | V | 2.0V ≤ VDD ≤ 4.5V |
| D031 | | with Schmitt Trigger buffer | Vss | — | 0.2 VDD | V | 2.0V ≤ VDD ≤ 5.5V |
| D032 | | $\overline{MCLR}$, OSC1 (RC mode) | Vss | — | 0.2 VDD | V | **(NOTE 1)** |
| D033 | | OSC1 (XT and LP modes) | Vss | — | 0.3 | V | |
| D033A | | OSC1 (HS mode) | Vss | — | 0.3 VDD | V | |
| | VIH | **Input High Voltage** | | | | | |
| | | I/O ports: | | — | | | |
| D040 | | with TTL buffer | 2.0 | — | VDD | V | 4.5V ≤ VDD ≤ 5.5V |
| D040A | | | 0.25 VDD + 0.8 | — | VDD | V | 2.0V ≤ VDD ≤ 4.5V |
| D041 | | with Schmitt Trigger buffer | 0.8 VDD | — | VDD | V | 2.0V ≤ VDD ≤ 5.5V |
| D042 | | $\overline{MCLR}$ | 0.8 VDD | — | VDD | V | |
| D043 | | OSC1 (XT and LP modes) | 1.6 | — | VDD | V | |
| D043A | | OSC1 (HS mode) | 0.7 VDD | — | VDD | V | |
| D043B | | OSC1 (RC mode) | 0.9 VDD | — | VDD | V | **(NOTE 1)** |
| | IIL | **Input Leakage Current(2,3)** | | | | | |
| D060 | | I/O ports | — | ± 0.1 | ± 1 | µA | VSS ≤ VPIN ≤ VDD,<br>Pin at high-impedance |
| D061 | | GP3/$\overline{MCLR}$(3,4) | — | ± 0.7 | ± 5 | µA | VSS ≤ VPIN ≤ VDD |
| D063 | | OSC1 | — | ± 0.1 | ± 5 | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration |
| D070* | IPUR | **GPIO Weak Pull-up Current(5)** | 50 | 250 | 400 | µA | VDD = 5.0V, VPIN = VSS |
| | VOL | **Output Low Voltage** | — | — | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V,<br>-40°C to +125°C |
| D080 | | I/O ports | — | — | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V,<br>-40°C to +85°C |
| | VOH | **Output High Voltage** | VDD – 0.7 | — | — | V | IOH = -2.5mA, VDD = 4.5V,<br>-40°C to +125°C |
| D090 | | I/O ports(2) | VDD – 0.7 | — | — | V | IOH = -3.0 mA, VDD = 4.5V,<br>-40°C to +85°C |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

**2:** Negative current is defined as current sourced by the pin.

**3:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**4:** This specification applies to GP3/$\overline{MCLR}$ configured as GP3 with the internal weak pull-up disabled.

**5:** This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/$\overline{MCLR}$. When GP3/$\overline{MCLR}$ is configured as $\overline{MCLR}$ reset pin, the weak pull-up is always enabled.

**6:** Applies to PIC12F617 only.

**TABLE 16-12: PIC12F615/617/HV615 A/D CONVERSION REQUIREMENTS**

| **Standard Operating Conditions (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| AD130* | TAD | A/D Clock Period | 1.6 | — | 9.0 | µs | TOSC-based, VREF ≥ 3.0V |
| | | | 3.0 | — | 9.0 | µs | TOSC-based, VREF full range(3) |
| | | A/D Internal RC Oscillator Period | | | | | ADCS<1:0> = 11 (ADRC mode) |
| | | | 3.0 | 6.0 | 9.0 | µs | At VDD = 2.5V |
| | | | 1.6 | 4.0 | 6.0 | µs | At VDD = 5.0V |
| AD131 | TCNV | Conversion Time (not including Acquisition Time)(1) | — | 11 | — | TAD | Set GO/$\overline{\text{DONE}}$ bit to new data in A/D Result register |
| AD132* | TACQ | Acquisition Time | | 11.5 | — | µs | |
| AD133* | TAMP | Amplifier Settling Time | — | — | 5 | µs | |
| AD134 | TGO | Q4 to A/D Clock Start | — | TOSC/2 | — | — | |
| | | | — | TOSC/2 + TCY | — | — | If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed. |

* These parameters are characterized but not tested.

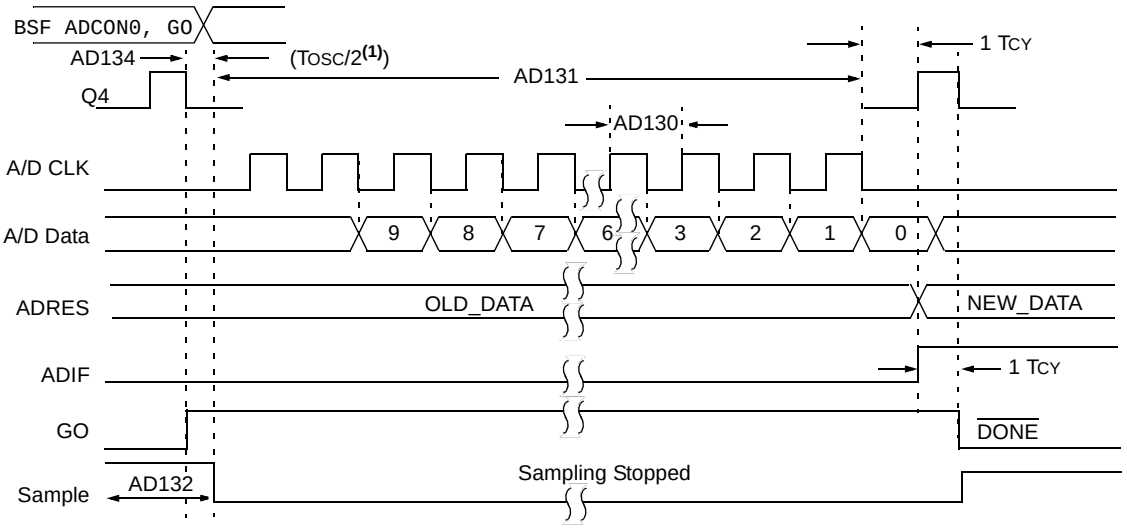
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** ADRESH and ADRESL registers may be read on the following TCY cycle.

**2:** See **Section 10.3 "A/D Acquisition Requirements"** for minimum conditions.

**3:** Full range for PIC12HV609/HV615 powered by the shunt regulator is the 5V regulated voltage.

**FIGURE 16-10: PIC12F615/617/HV615 A/D CONVERSION TIMING (NORMAL MODE)**




**Note 1:** If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

## 16.12 High Temperature Operation

This section outlines the specifications for the PIC12F615 device operating in a temperature range between -40°C and 150°C.(4) The specifications between -40°C and 150°C(4) are identical to those shown in DS41288 and DS80329.

**Note 1:** Writes are **not allowed** for Flash Program Memory above 125°C.

**2:** All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.

**3:** The temperature range indicator in the part number is "H" for -40°C to 150°C.(4)

Example: PIC12F615T-H/ST indicates the device is shipped in a TAPE and reel configuration, in the MSOP package, and is rated for operation from -40°C to 150°C.(4)

**4:** AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

**TABLE 16-13: ABSOLUTE MAXIMUM RATINGS**

| Parameter | Source/Sink | Value | Units |
|---|---|---|---|
| Max. Current: VDD | Source | 20 | mA |
| Max. Current: VSS | Sink | 50 | mA |
| Max. Current: PIN | Source | 5 | mA |
| Max. Current: PIN | Sink | 10 | mA |
| Pin Current: at VOH | Source | 3 | mA |
| Pin Current: at VOL | Sink | 8.5 | mA |
| Port Current: GPIO | Source | 20 | mA |
| Port Current: GPIO | Sink | 50 | mA |
| Maximum Junction Temperature | | 155 | °C |

**Note:** Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

**FIGURE 17-3: PIC12F609/615/617 IDD EC (4 MHz) vs. VDD**

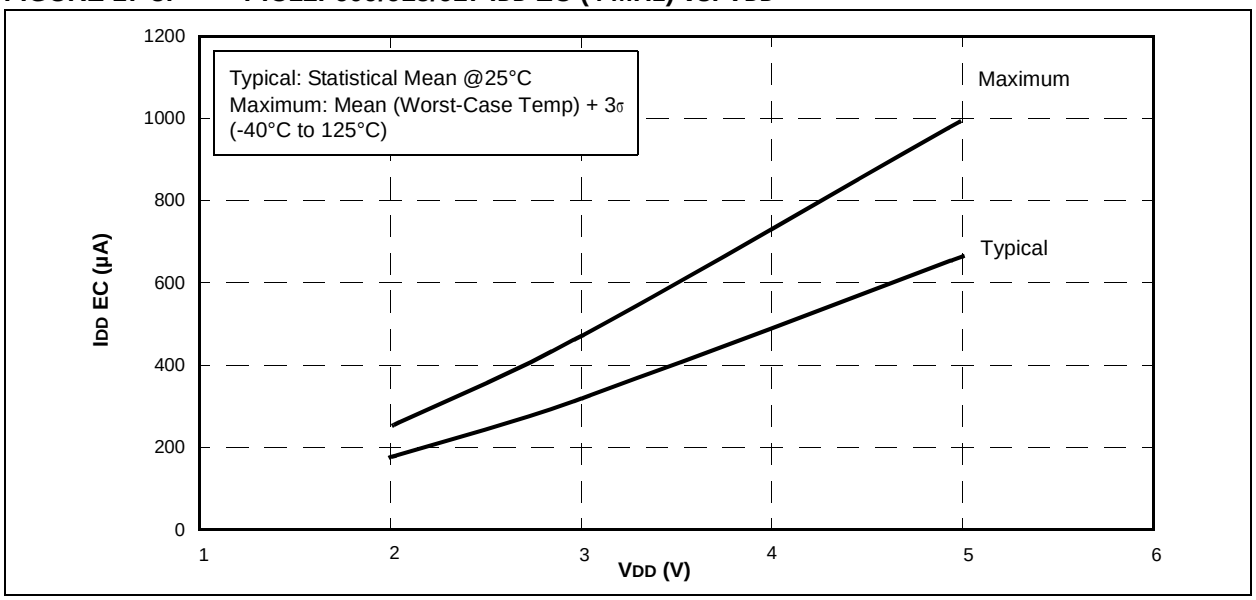



**FIGURE 17-4: PIC12F609/615/617 IDD XT (1 MHz) vs. VDD**

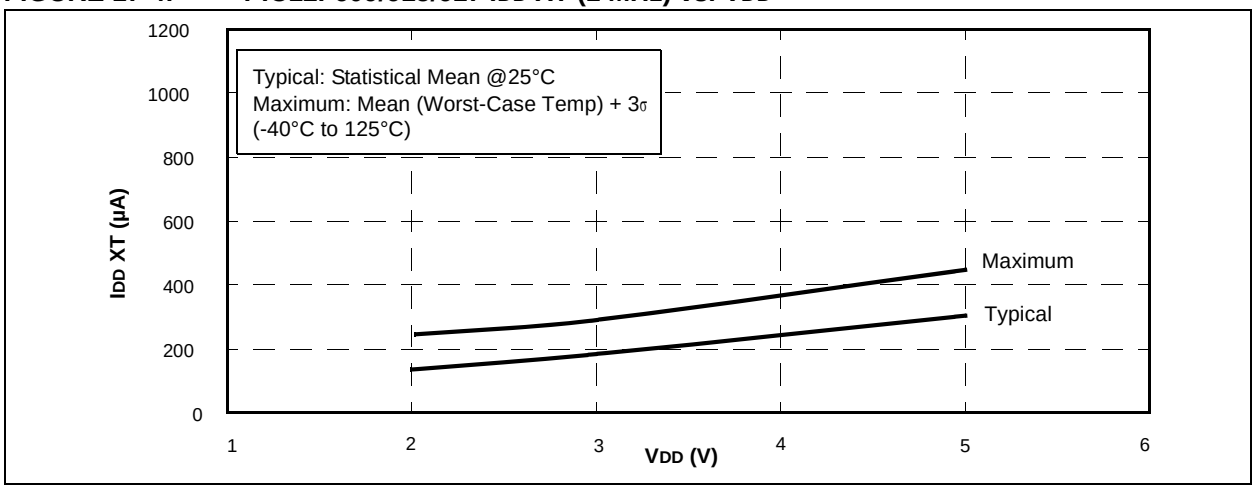



**FIGURE 17-5: PIC12F609/615/617 IDD XT (4 MHz) vs. VDD**

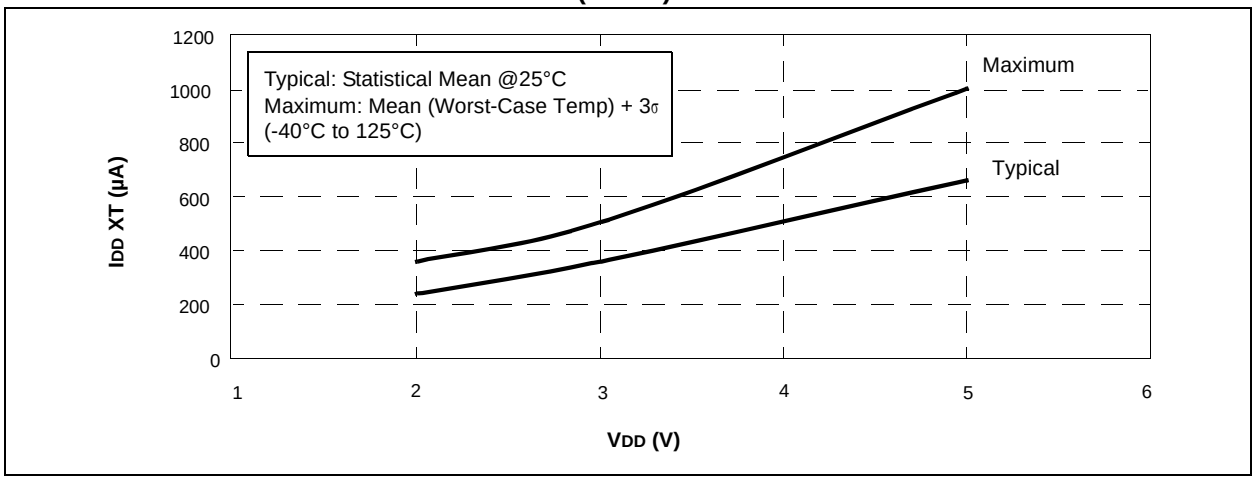


**FIGURE 17-12: PIC12F609/615/617 IPD WDT vs. VDD**

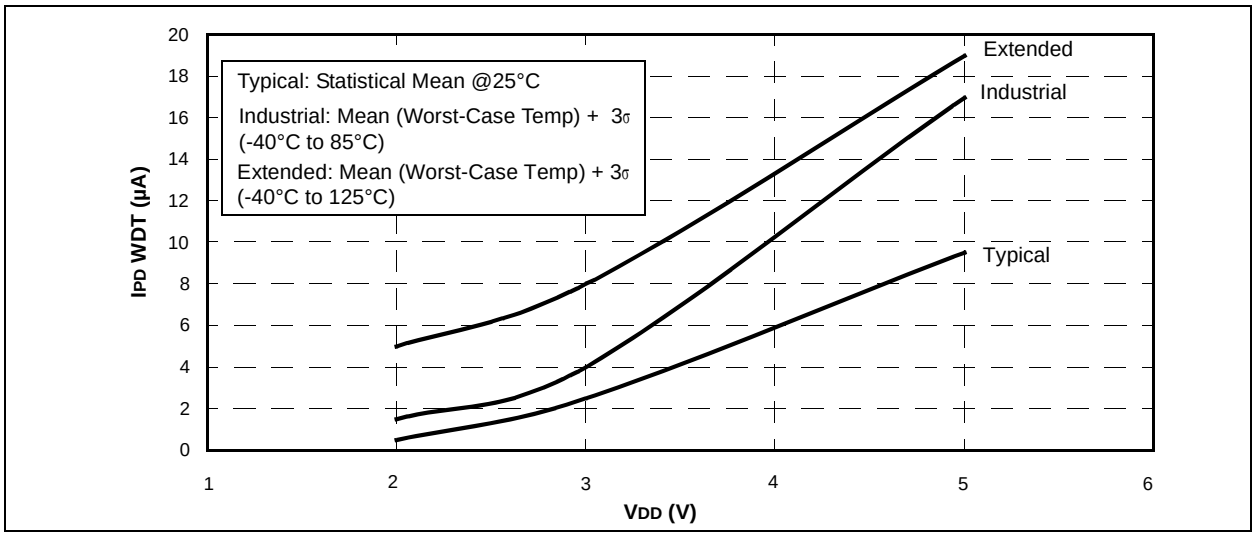



**FIGURE 17-13: PIC12F609/615/617 IPD BOR vs. VDD**

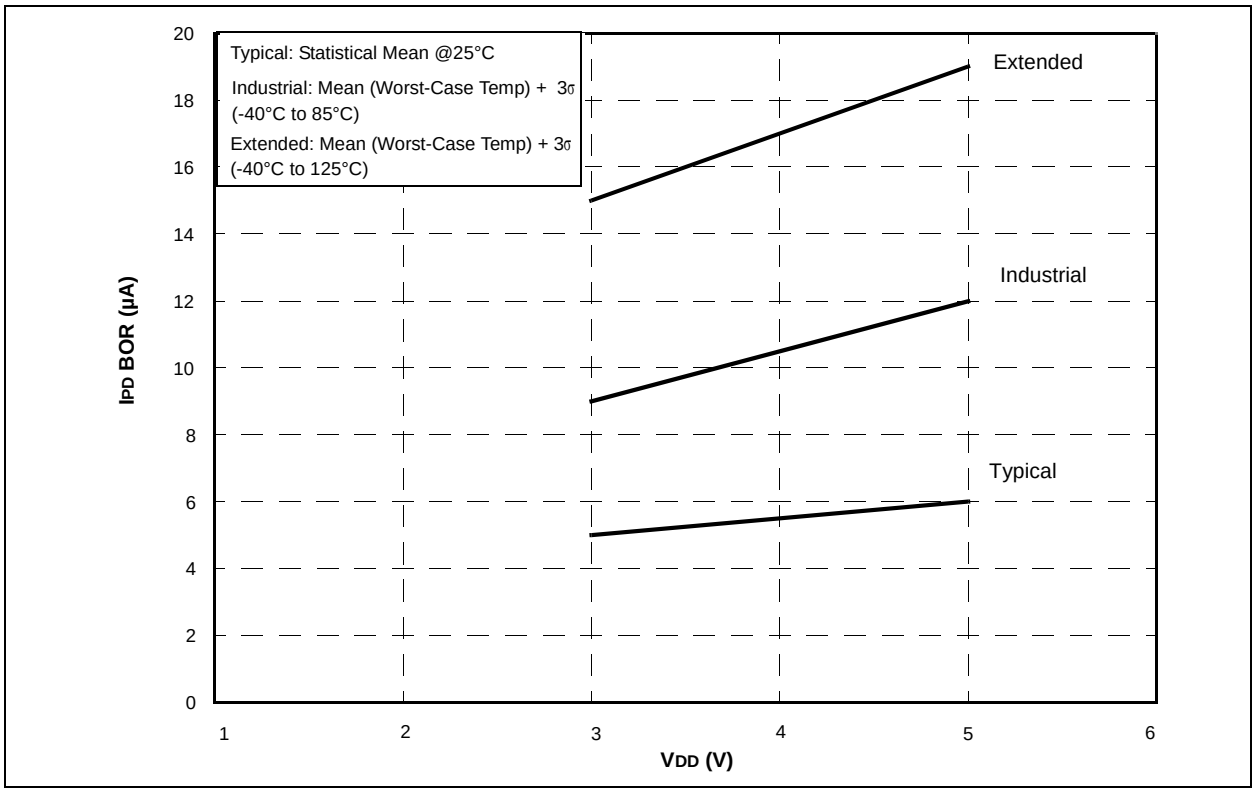


**FIGURE 17-35: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)**

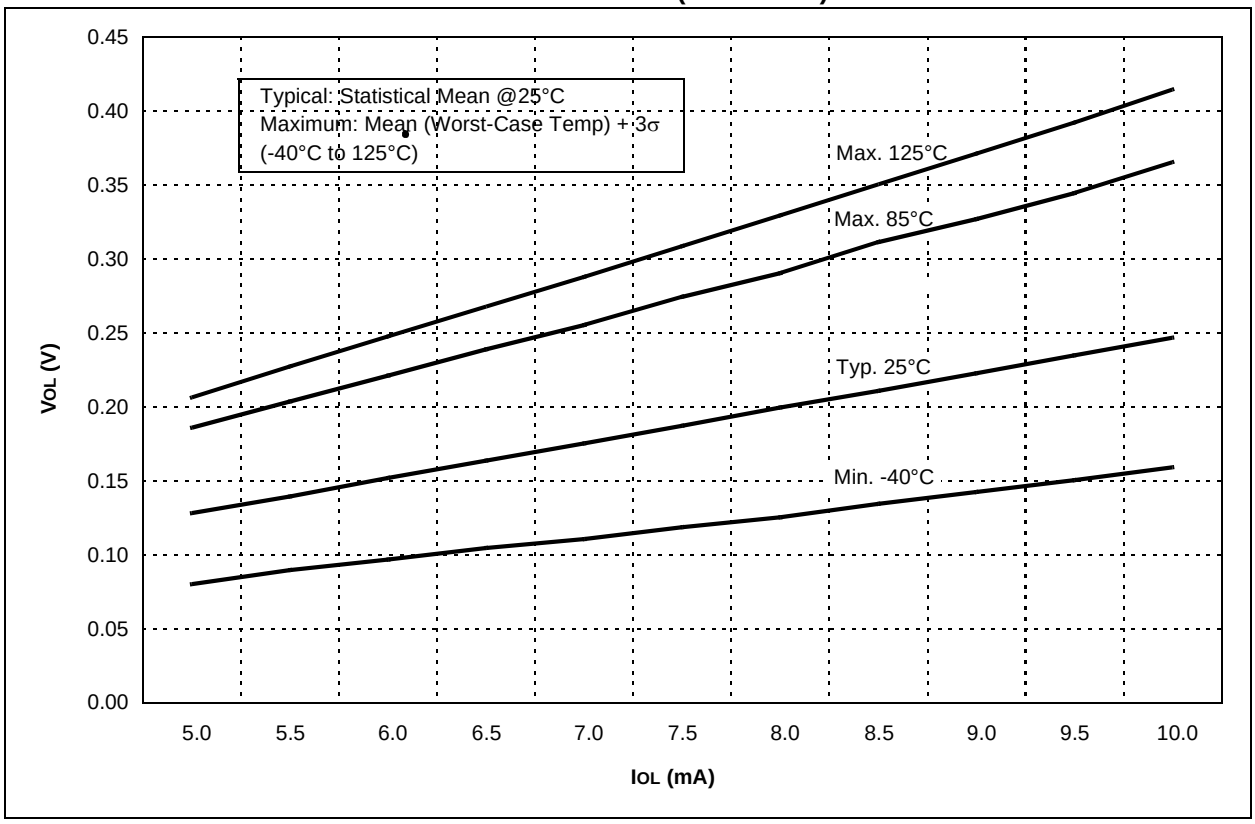
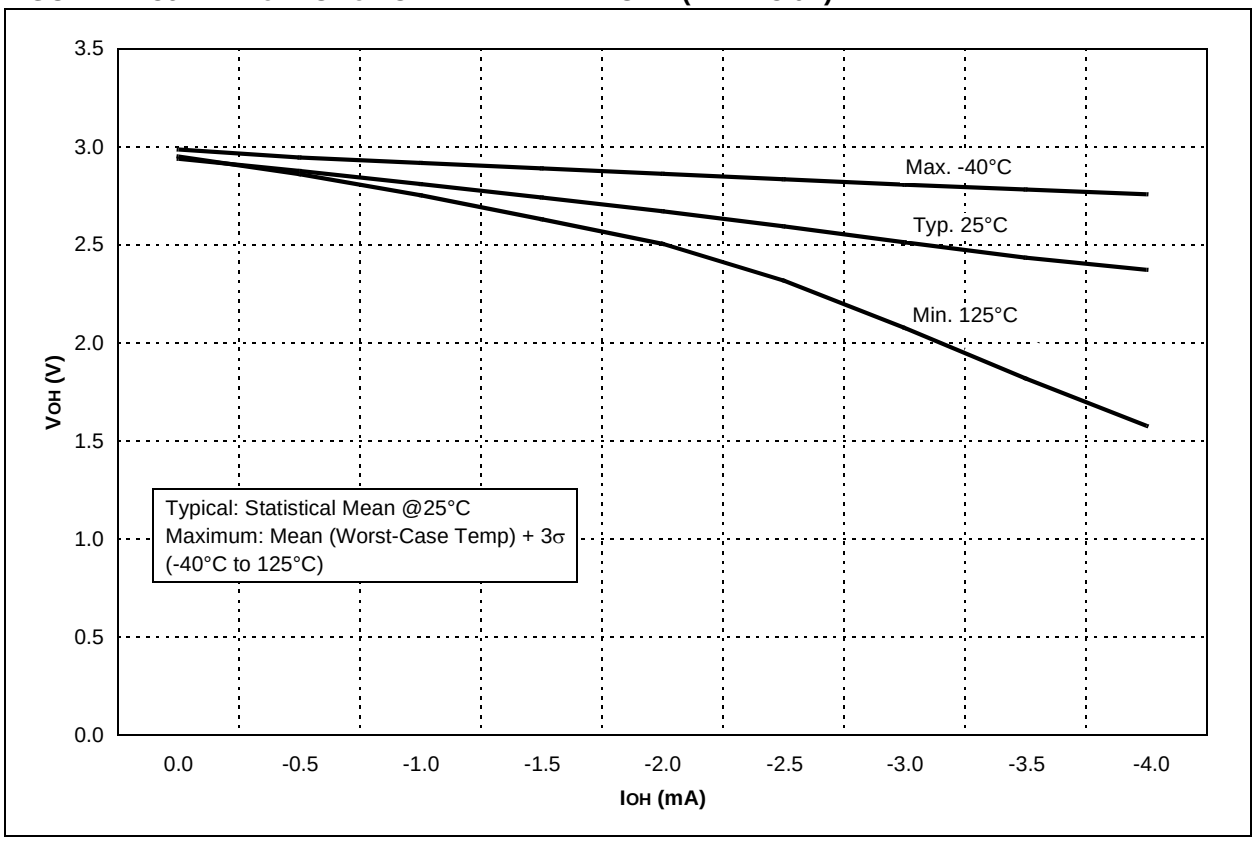



**FIGURE 17-36: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)**



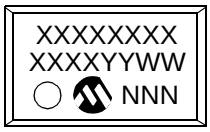
## 18.0 PACKAGING INFORMATION

### 18.1 Package Marking Information

8-Lead PDIP (.300”)


Example


8-Lead SOIC (.150”)



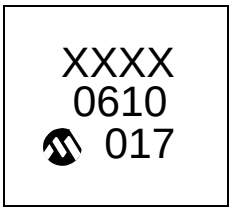

Example


8-Lead MSOP

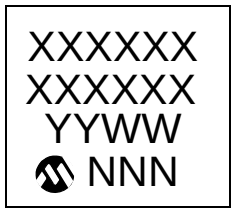

Example


8-Lead DFN (3x3 mm)

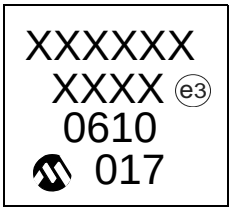

Example




8-Lead DFN (4x4 mm) (for PIC12F609/615/HV609/615 devices only)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ( ) (e3) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | | |
|---|---|---|
| **Device:** | PIC12F609, PIC12F609T(1), PIC12HV609, PIC12HV609T(1), PIC12F615, PIC12F615T(1), PIC12HV615, PIC12HV615T(1), PIC12F617, PIC12F617T(1) | |
| **Temperature Range:** | H = -40°C to +150°C | (High Temp)(3) |
| | I = -40°C to +85°C | (Industrial) |
| | E = -40°C to +125°C | (Extended) |
| **Package:** | P = | Plastic DIP (PDIP) |
| | SN = | 8-lead Small Outline (150 mil) (SOIC) |
| | MS = | Micro Small Outline (MSOP) |
| | MF = | 8-lead Plastic Dual Flat, No Lead (3x3) (DFN) |
| | MD = | 8-lead Plastic Dual Flat, No Lead (4x4)(DFN)(1,2) |
| **Pattern:** | QTP, SQTP or ROM Code; Special Requirements (blank otherwise) | |

**Examples:**

a) PIC12F615-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
b) PIC12F615-I/SN = Industrial Temp., SOIC package, 20 MHz
c) PIC12F615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
d) PIC12F609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
e) PIC12HV615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
f) PIC12HV609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
g) PIC12F617T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
h) PIC12F617-I/P = Industrial Temp., PDIP package, 20 MHz
i) PIC12F615-H/SN = High Temp., SOIC package, 20 MHz

**Note 1:** T = in tape and reel for MSOP, SOIC and DFN packages only.
**2:** Not available for PIC12F617.
**3:** High Temp. available for PIC12F615 only.