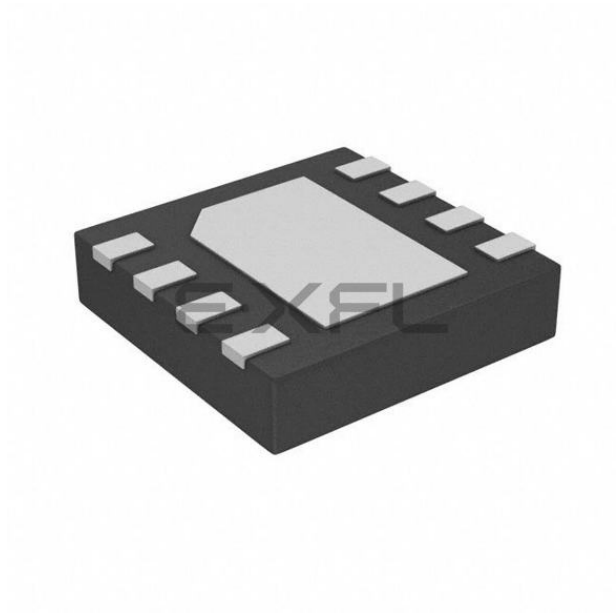


Welcome to E-XFL.COM

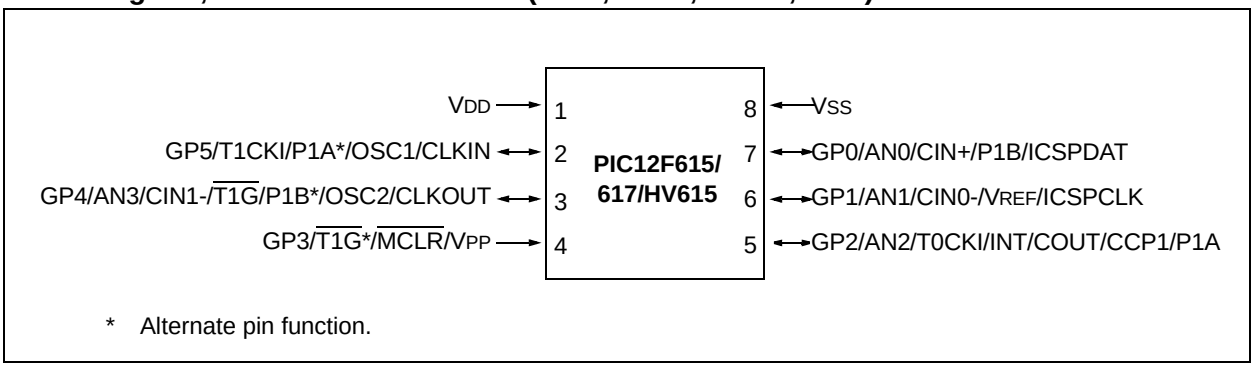
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f615-e-mf

8-Pin Diagram, PIC12F615/617/HV615 (PDIP, SOIC, MSOP, DFN)



* Alternate pin function.

TABLE 2: PIC12F615/617/HV615 PIN SUMMARY (PDIP, SOIC, MSOP, DFN)

I/O	Pin	Analog	Comparators	Timer	CCP	Interrupts	Pull-ups	Basic
GP0	7	AN0	CIN+	—	P1B	IOC	Y	ICSPDAT
GP1	6	AN1	CIN0-	—	—	IOC	Y	ICSPCLK/VREF
GP2	5	AN2	COUT	T0CKI	CCP1/P1A	INT/IOC	Y	—
GP3(1)	4	—	—	T1G*	—	IOC	Y(2)	MCLR/VPP
GP4	3	AN3	CIN1-	T1G	P1B*	IOC	Y	OSC2/CLKOUT
GP5	2	—	—	T1CKI	P1A*	IOC	Y	OSC1/CLKIN
—	1	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	VSS

* Alternate pin function.

Note 1: Input only.

2: Only when pin is configured for external MCLR.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC12F609/615/12HV609/615, and as 128 x 8 in the PIC12F617. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 "Indirect Addressing, INDF and FSR Registers"**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-3: DATA MEMORY MAP OF THE PIC12F609/HV609

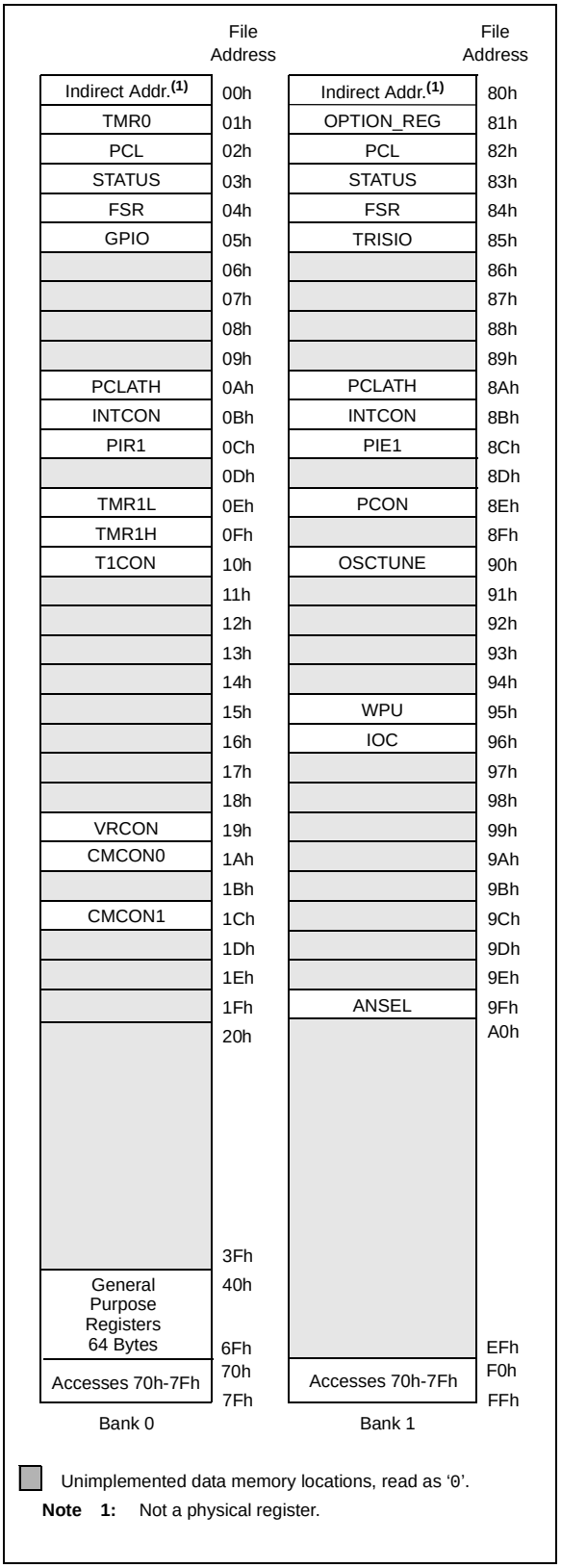
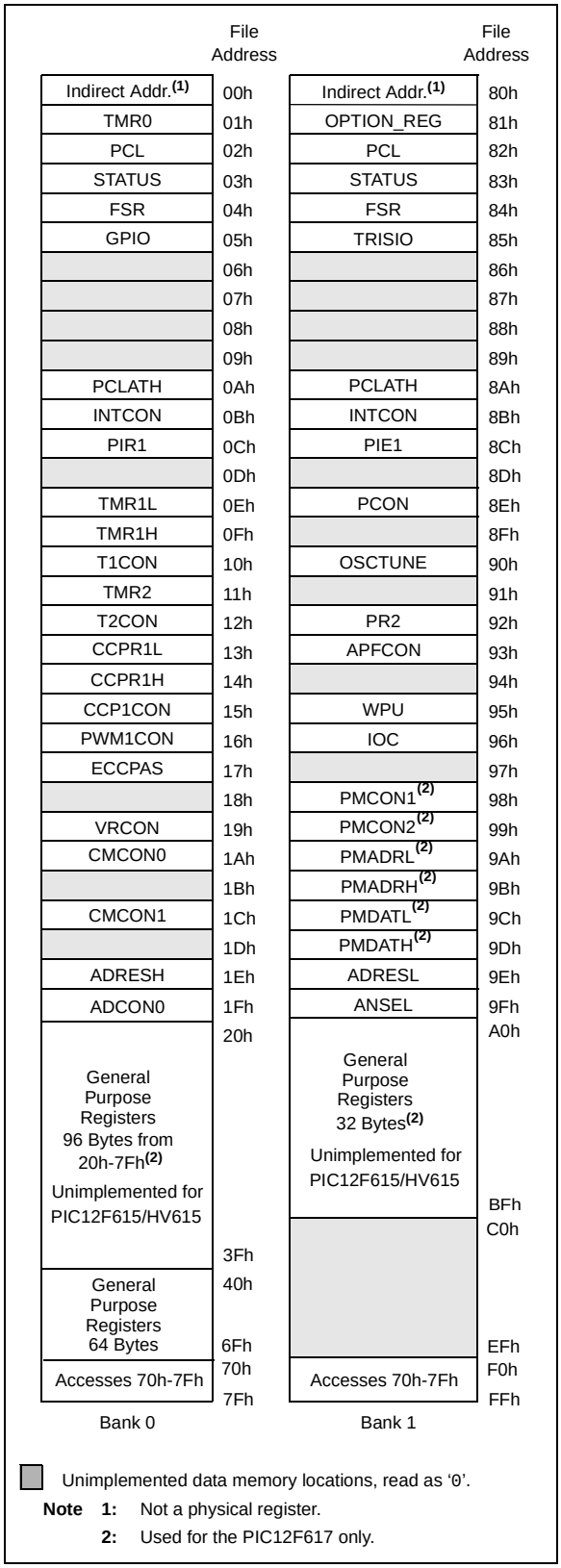


FIGURE 2-4: DATA MEMORY MAP OF THE PIC12F615/617/HV615



Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

2: Used for the PIC12F617 only.

TABLE 2-2: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25, 116
01h	TMR0	Timer0 Module's Register								xxxx xxxx	53, 116
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	25, 116
03h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18, 116
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	25, 116
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--x0 x000	43, 116
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	25, 116
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	20, 116
0Ch	PIR1	—	ADIF	CCP1IF	—	CMIF	—	TMR2IF	TMR1IF	-00- 0-00	22, 116
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 116
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 116
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	62, 116
11h	TMR2(3)	Timer2 Module Register								0000 0000	65, 116
12h	T2CON(3)	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	66, 116
13h	CCPR1L(3)	Capture/Compare/PWM Register 1 Low Byte								XXXX XXXX	90, 116
14h	CCPR1H(3)	Capture/Compare/PWM Register 1 High Byte								XXXX XXXX	90, 116
15h	CCP1CON(3)	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	89, 116
16h	PWM1CON(3)	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000	105, 116
17h	ECCPAS(3)	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000	102, 116
18h	—	Unimplemented								—	—
19h	VRCON	CMVREN	—	VRR	FVREN	VR3	VR2	VR1	VR0	0-00 0000	76, 116
1Ah	CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -0-0	72, 116
1Bh	—					—		—		—	—
1Ch	CMCON1	—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC	---0 0-10	73, 116
1Dh	—	Unimplemented								—	—
1Eh	ADRESH(2, 3)	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	85, 116
1Fh	ADCON0(3)	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	00-0 0000	84, 116

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: Read only register.

3: PIC12F615/617/HV615 only.

TABLE 2-4: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25, 116
81h	OPTION_REG	$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19, 116
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	25, 116
83h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18, 116
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	25, 116
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3(4)	TRISIO2	TRISIO1	TRISIO0	--11 1111	44, 116
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	25, 116
8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF(3)	0000 0000	20, 116
8Ch	PIE1	—	ADIE	CCP1IE	—	CMIE	—	TMR2IE	TMR1IE	-00- 0-00	21, 116
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	23, 116
8Fh	—	Unimplemented								—	—
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	41, 116
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Module Period Register								1111 1111	65, 116
93h	APFCON	—	—	—	T1GSEL	—	—	P1BSEL	P1ASEL	---0 --00	21, 116
94h	—	Unimplemented								—	—
95h	WPU(2)	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	46, 116
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	46, 116
97h	—	Unimplemented								—	—
98h	PMCON1(7)	—	—	—	—	—	WREN	WR	RD	---- -000	29
99h	PMCON2(7)	Program Memory Control Register 2 (not a physical register).								---- ----	—
9Ah	PMADRL(7)	PMADRL7	PMADRL6	PMADRL5	PMADRL4	PMADRL3	PMADRL2	PMADRL1	PMADRL0	0000 0000	28
9Bh	PMADRH(7)	—	—	—	—	—	PMADRH2	PMADRH1	PMADRH0	---- -000	28
9Ch	PMDATL(7)	PMDATL7	PMDATL6	PMDATL5	PMDATL4	PMDATL3	PMDATL2	PMDATL1	PMDATL0	0000 0000	28
9Dh	PMDATH(7)	—	—	Program Memory Data Register High Byte.						--00 0000	28
9Eh	ADRESL(5, 6)	Least Significant 2 bits of the left shifted result or 8 bits of the right shifted result								xxxx xxxx	85, 117
9Fh	ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	45, 117

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: GP3 pull-up is enabled when MCLRE is '1' in the Configuration Word register.

3: $\overline{MCLR}$ and WDT Reset does not affect the previous value data latch. The GPIF bit will clear upon Reset but will set again if the mismatch exists.

4: TRISIO3 always reads as '1' since it is an input only pin.

5: Read only register.

6: PIC12F615/617/HV615 only.

7: PIC12F617 only.

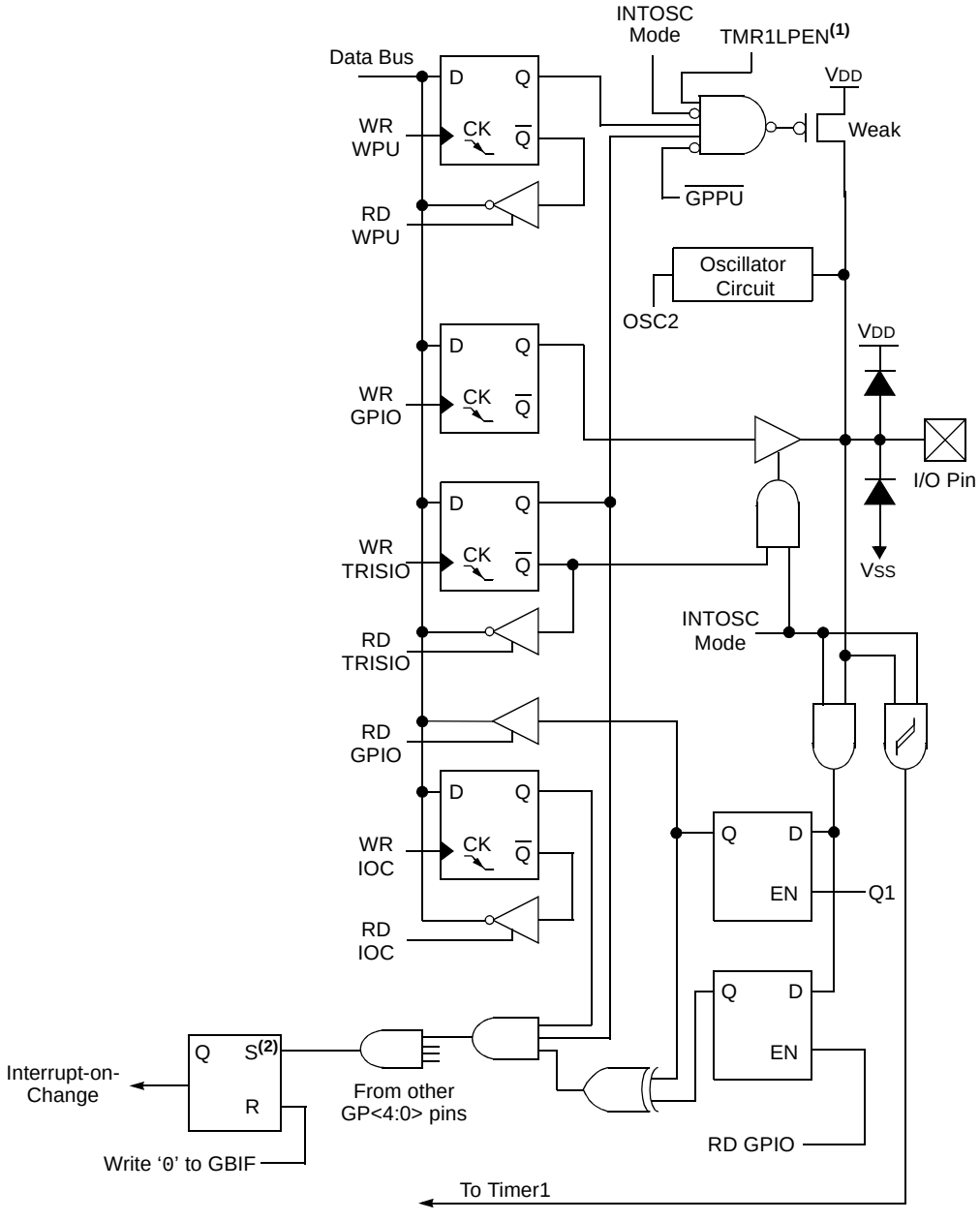
5.2.4.6 GP5/T1CKI/P1A(1, 2)/OSC1/CLKIN

Figure 5-5 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- PWM output, alternate pin(1, 2)
- a crystal/resonator connection
- a clock input

Note 1: Alternate pin function.
2: PIC12F615/617/HV615 only.

FIGURE 5-5: BLOCK DIAGRAM OF GP5



Note 1: Timer1 LP Oscillator enabled.
2: Set has priority over Reset.

7.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

7.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after one or more of the following conditions:

- Timer1 is enabled after POR or BOR Reset
- A write to TMR1H or TMR1L
- T1CKI is high when Timer1 is disabled and when Timer1 is re-enabled T1CKI is low. See Figure 7-2.

7.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

7.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO5 and TRISIO4 bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as '0' and TRISIO5 and TRISIO4 bits read as '1'.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

7.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment.

Note:	In asynchronous counter mode or when using the internal oscillator and T1ACS=1, Timer1 can not be used as a time base for the capture or compare modes of the ECCP module (for PIC12F615/617/HV615 only).

7.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TTMR1L register pair.

REGISTER 8-1: T2CON: TIMER 2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits
0000 =1:1 Postscaler
0001 =1:2 Postscaler
0010 =1:3 Postscaler
0011 =1:4 Postscaler
0100 =1:5 Postscaler
0101 =1:6 Postscaler
0110 =1:7 Postscaler
0111 =1:8 Postscaler
1000 =1:9 Postscaler
1001 =1:10 Postscaler
1010 =1:11 Postscaler
1011 =1:12 Postscaler
1100 =1:13 Postscaler
1101 =1:14 Postscaler
1110 =1:15 Postscaler
1111 =1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits
00 =Prescaler is 1
01 =Prescaler is 4
1x =Prescaler is 16

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	-00- 0-00	-00- 0-00
PR2(1)	Timer2 Module Period Register								1111 1111	1111 1111
TMR2(1)	Holding Register for the 8-bit TMR2 Register								0000 0000	0000 0000
T2CON(1)	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for Timer2 module.
Note 1: For PIC12F615/617/HV615 only.

9.10 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- 16-level voltage range
- Output clamped to VSS
- Ratiometric with VDD
- Fixed Reference (0.6)

The VRCON register (Register 9-3) controls the Voltage Reference module shown in Register 9-6.

9.10.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

9.10.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 9-1: CVREF OUTPUT VOLTAGE

$$VRR = 1 \text{ (low range):}$$
$$CVREF = (VR<3:0>/24) \times VDD$$
$$VRR = 0 \text{ (high range):}$$
$$CVREF = (VDD/4) + (VR<3:0> \times VDD/32)$$

The full range of VSS to VDD cannot be realized due to the construction of the module. See Figure 9-6.

9.10.3 OUTPUT CLAMPED TO VSS

The CVREF output voltage can be set to Vss with no power consumption by configuring VRCON as follows:

- FVREN = 0

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

9.10.4 OUTPUT RATIOMETRIC TO VDD

The comparator voltage reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 16.0 "Electrical Specifications"**.

9.10.5 FIXED VOLTAGE REFERENCE

The fixed voltage reference is independent of VDD, with a nominal output voltage of 0.6V. This reference can be enabled by setting the FVREN bit of the VRCON register to '1'. This reference is always enabled when the HFINTOSC oscillator is active.

9.10.6 FIXED VOLTAGE REFERENCE STABILIZATION PERIOD

When the Fixed Voltage Reference module is enabled, it will require some time for the reference and its amplifier circuits to stabilize. The user program must include a small delay routine to allow the module to settle. See **Section 16.0 "Electrical Specifications"** for the minimum delay requirement.

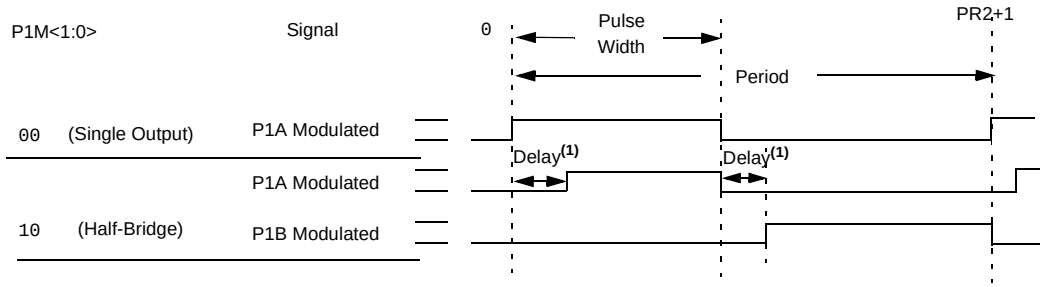
9.10.7 VOLTAGE REFERENCE SELECTION

Multiplexers on the output of the Voltage Reference module enable selection of either the CVREF or fixed voltage reference for use by the comparators.

Setting the CMVREN bit of the VRCON register enables current to flow in the CVREF voltage divider and selects the CVREF voltage for use by the Comparator. Clearing the CMVREN bit selects the fixed voltage for use by the Comparator.

When the CMVREN bit is cleared, current flow in the CVREF voltage divider is disabled minimizing the power drain of the voltage reference peripheral.

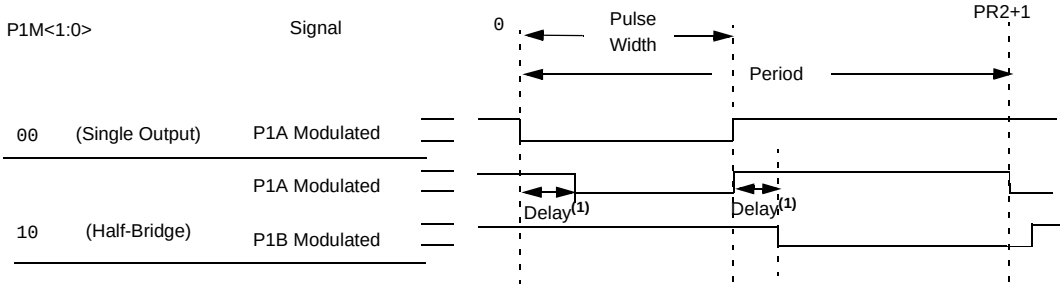
FIGURE 11-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)



Relationships:
- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 11.4.6 "Programmable Dead-Band Delay mode"**).

FIGURE 11-7: EXAMPLE ENHANCED PWM OUTPUT RELATIONSHIPS (ACTIVE-LOW STATE)



Relationships:
- Period = 4 * Tosc * (PR2 + 1) * (TMR2 Prescale Value)
- Pulse Width = Tosc * (CCPR1L<7:0>:CCP1CON<5:4>) * (TMR2 Prescale Value)
- Delay = 4 * Tosc * (PWM1CON<6:0>)

Note 1: Dead-band delay is programmed using the PWM1CON register (**Section 11.4.6 "Programmable Dead-Band Delay mode"**).

15.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

15.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

15.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D101*	COSC2	**Capacitive Loading Specs on Output Pins** OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	
		Program Flash Memory					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Bulk Erase/Write	4.5	—	5.5	V	
D132A	VPEW	VDD for Row Erase/Write(6)	VMIN	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: This specification applies to GP3/MCLR configured as GP3 with the internal weak pull-up disabled.

5: This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/MCLR. When GP3/MCLR is configured as MCLR reset pin, the weak pull-up is always enabled.

6: Applies to PIC12F617 only.

17.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

FIGURE 17-1: PIC12F609/615/617 IDD LP (32 kHz) vs. VDD

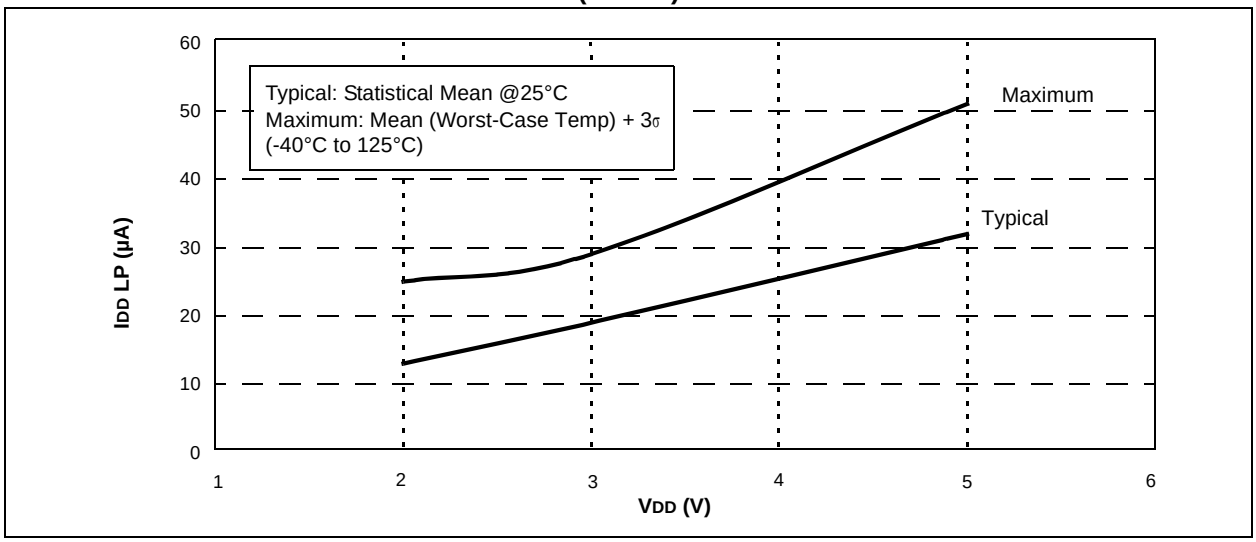


FIGURE 17-2: PIC12F609/615/617 IDD EC (1 MHz) vs. VDD

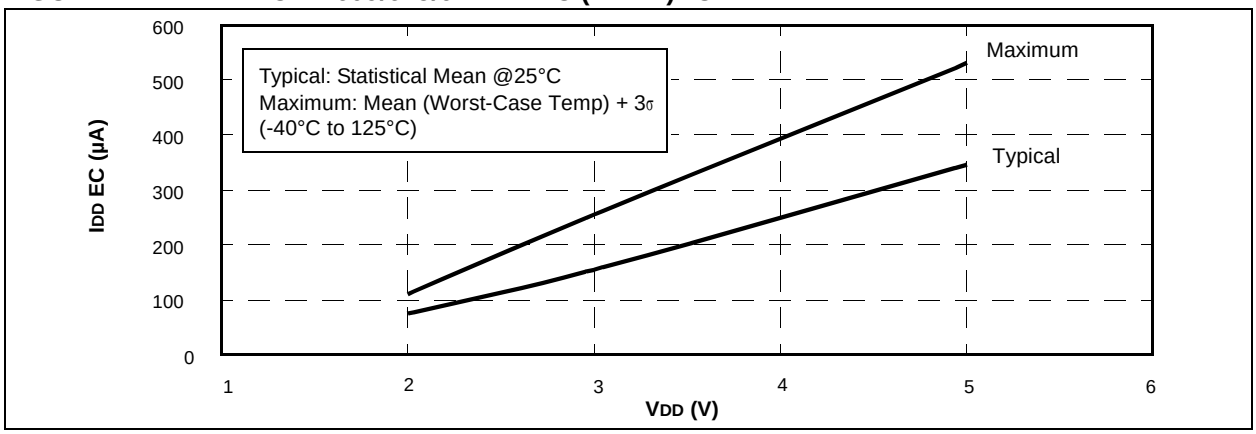


FIGURE 17-16: PIC12F609/615/617 IPD T1OSC vs. VDD

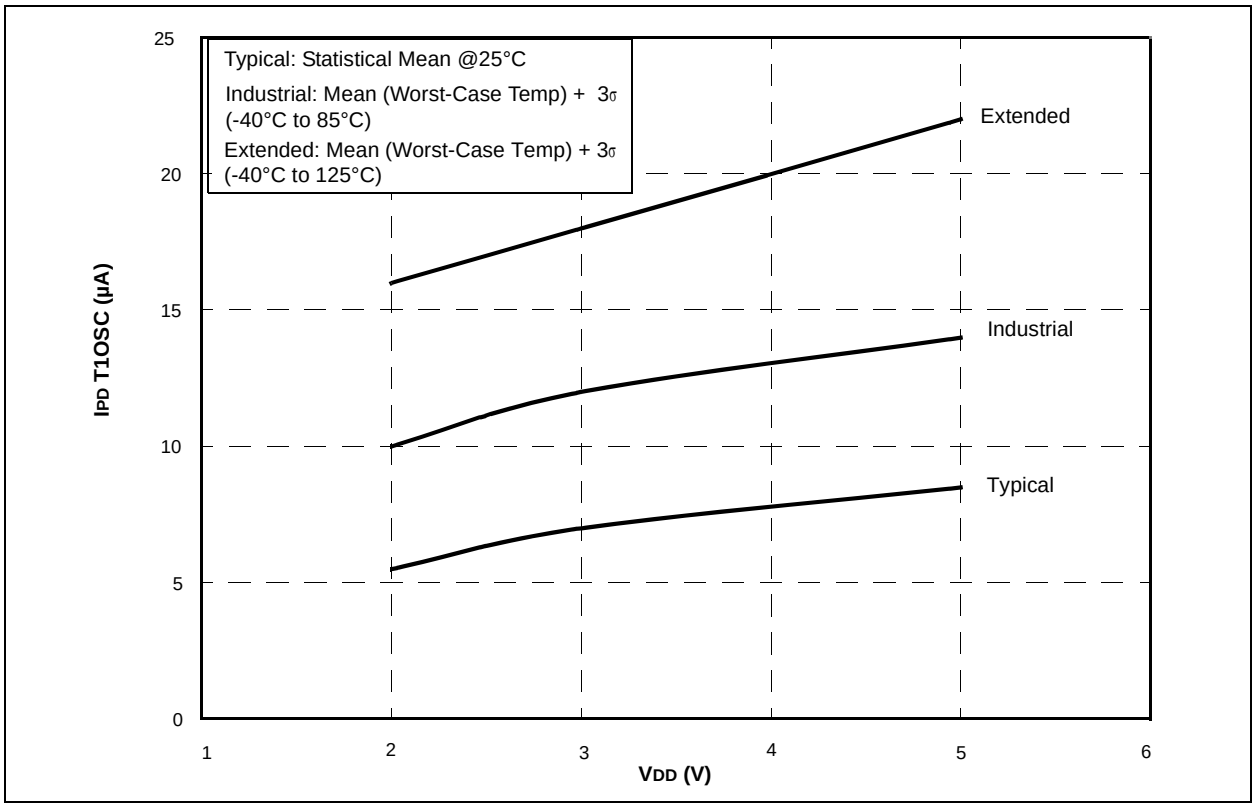


FIGURE 17-17: PIC12F615/617 IPD A/D vs. VDD

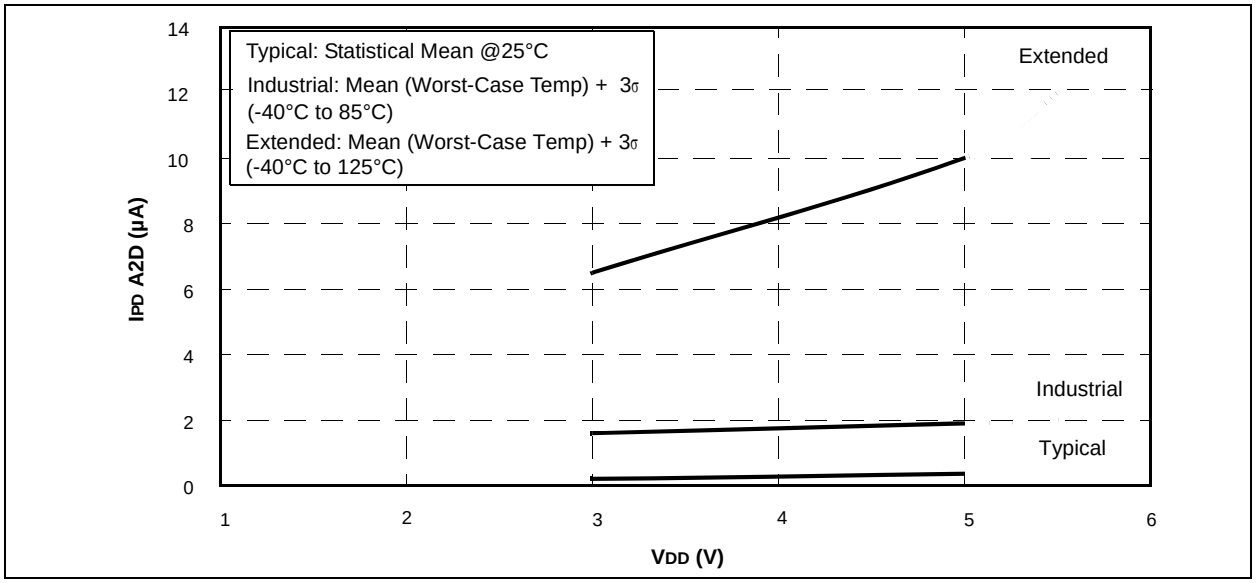


FIGURE 17-21: PIC12HV609/615 IDD XT (1 MHz) vs. VDD

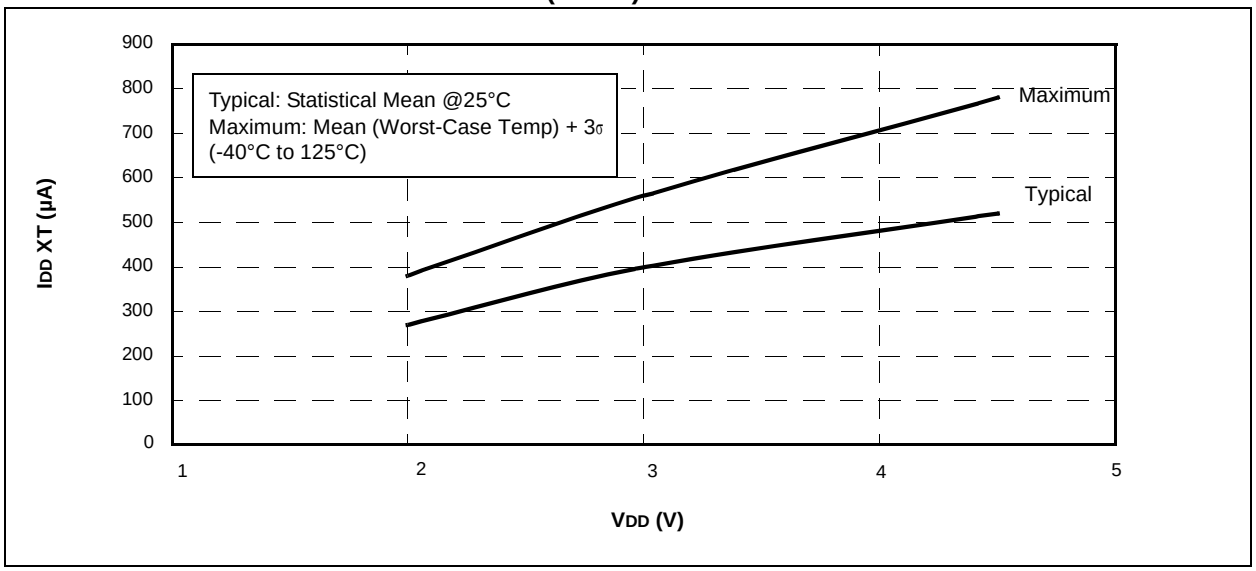


FIGURE 17-22: PIC12HV609/615 IDD XT (4 MHz) vs. VDD

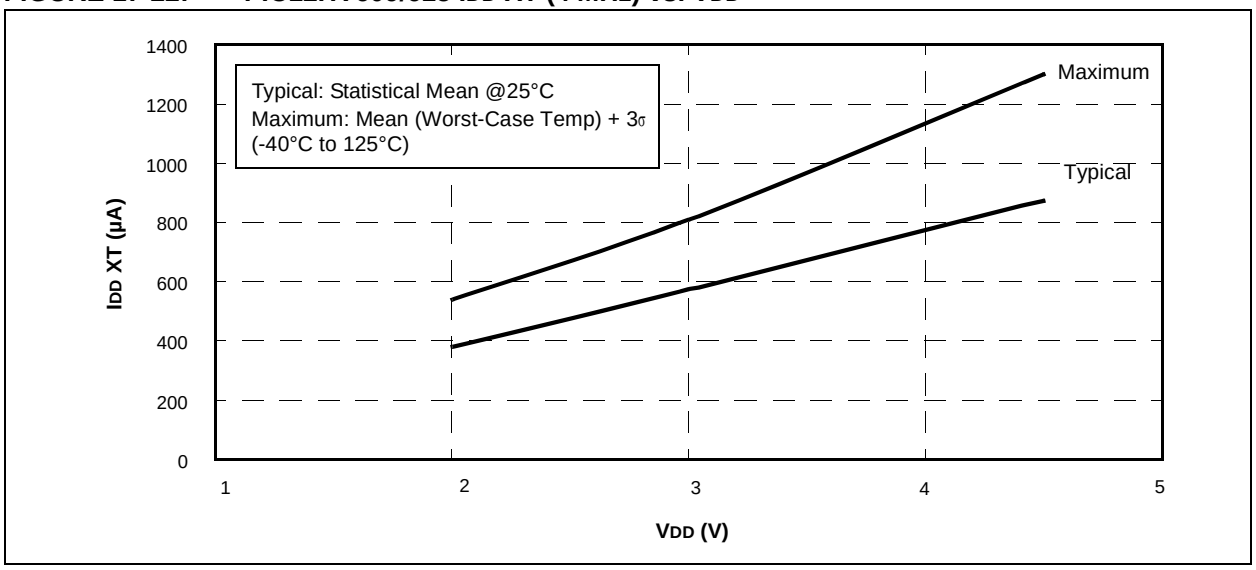


FIGURE 17-23: PIC12HV609/615 IDD INTOSC (4 MHz) vs. VDD

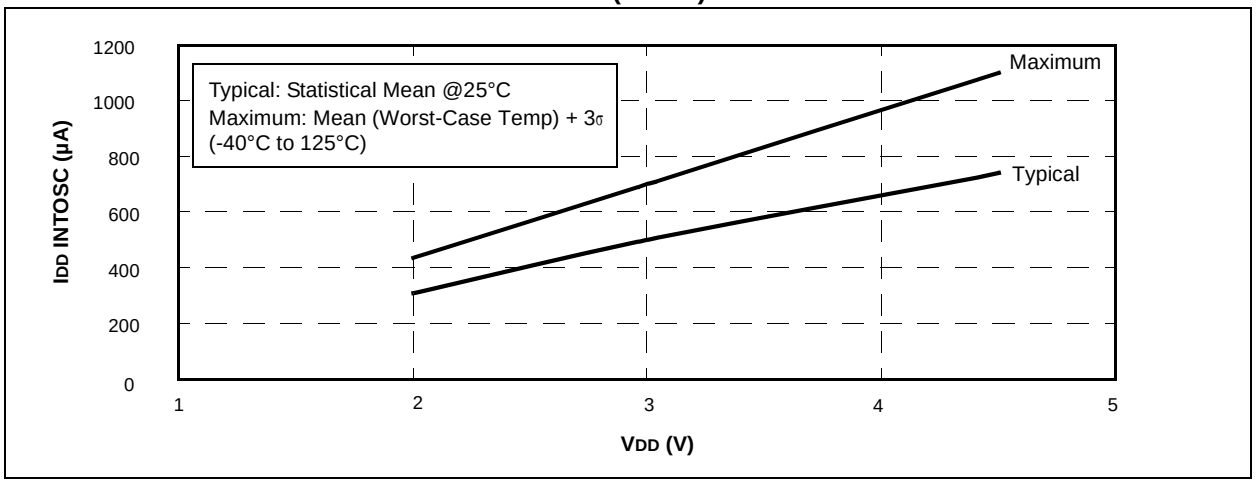


FIGURE 17-33: PIC12HV615 IPD A/D vs. VDD

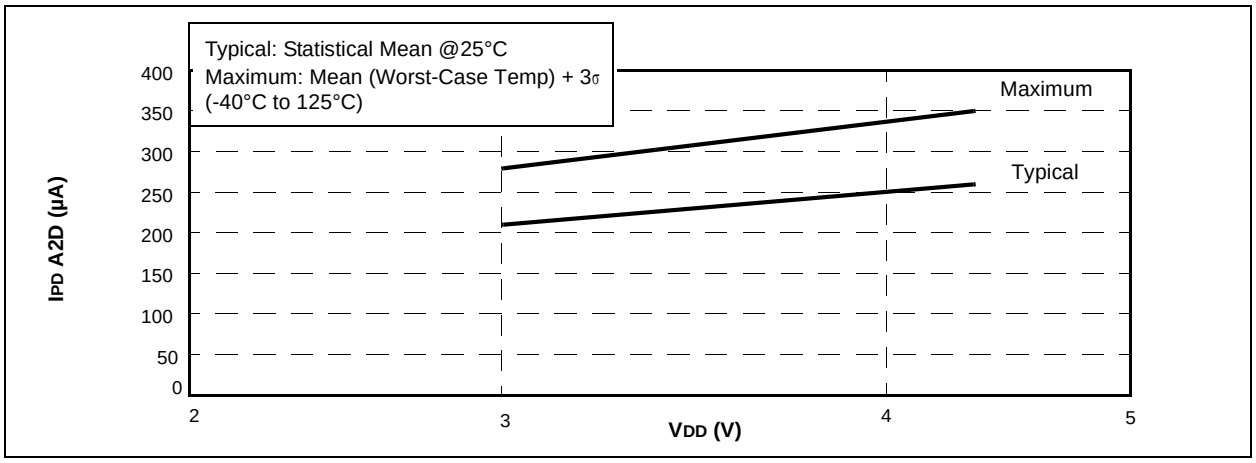


FIGURE 17-34: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

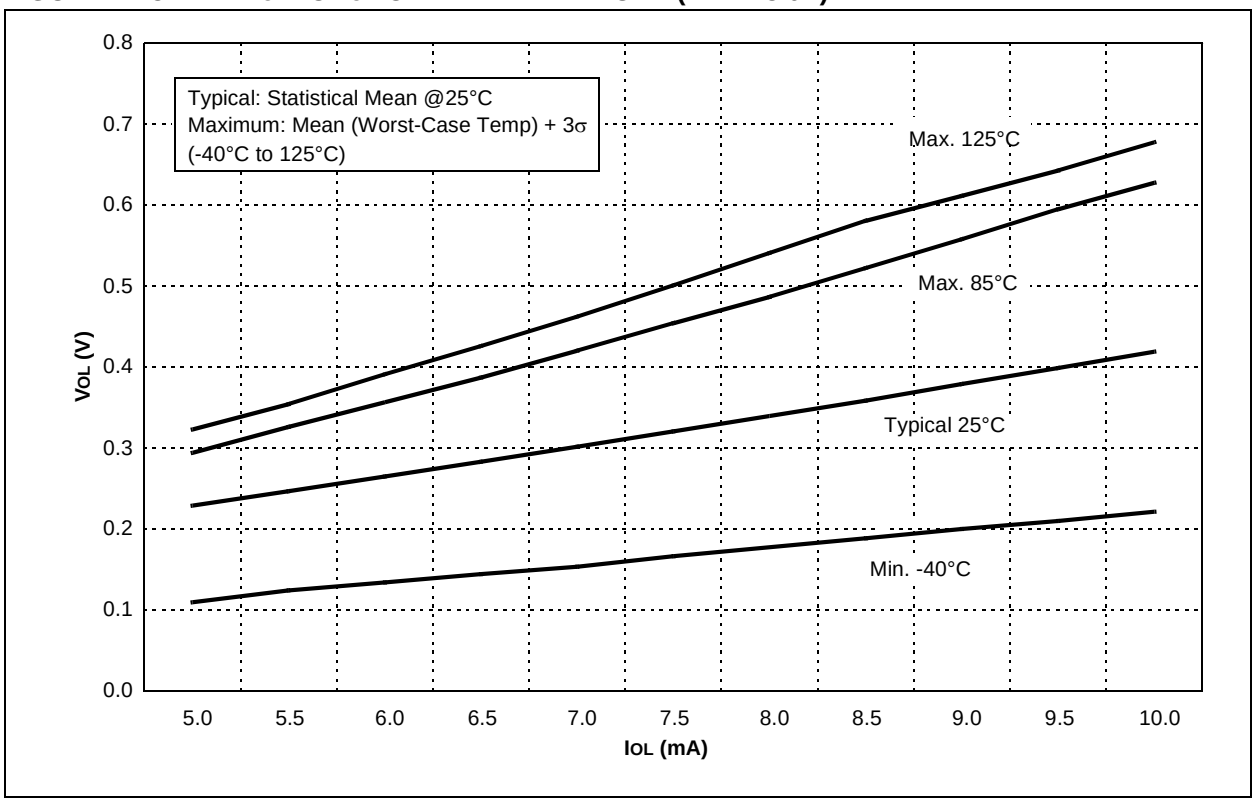


FIGURE 17-37: V_{OH} vs. I_{OH} OVER TEMPERATURE (V_{DD} = 5.0V)

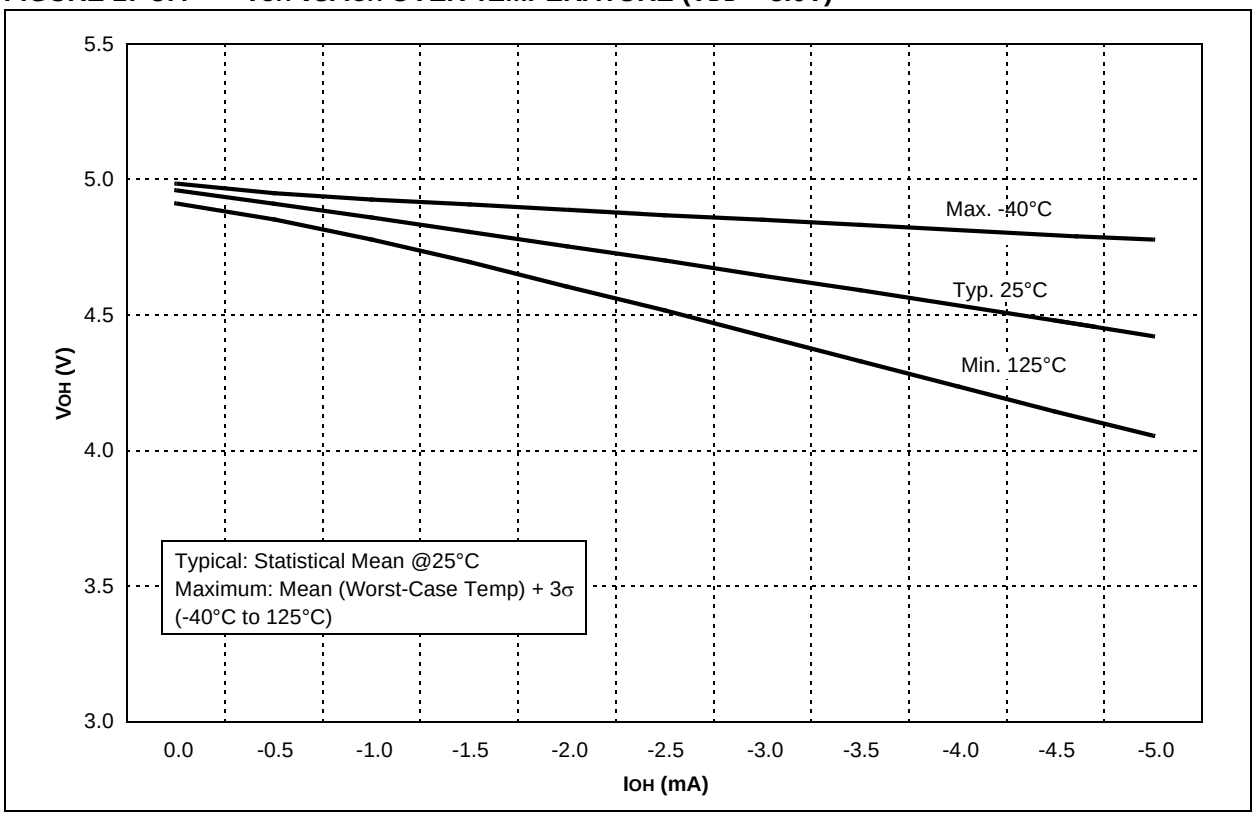
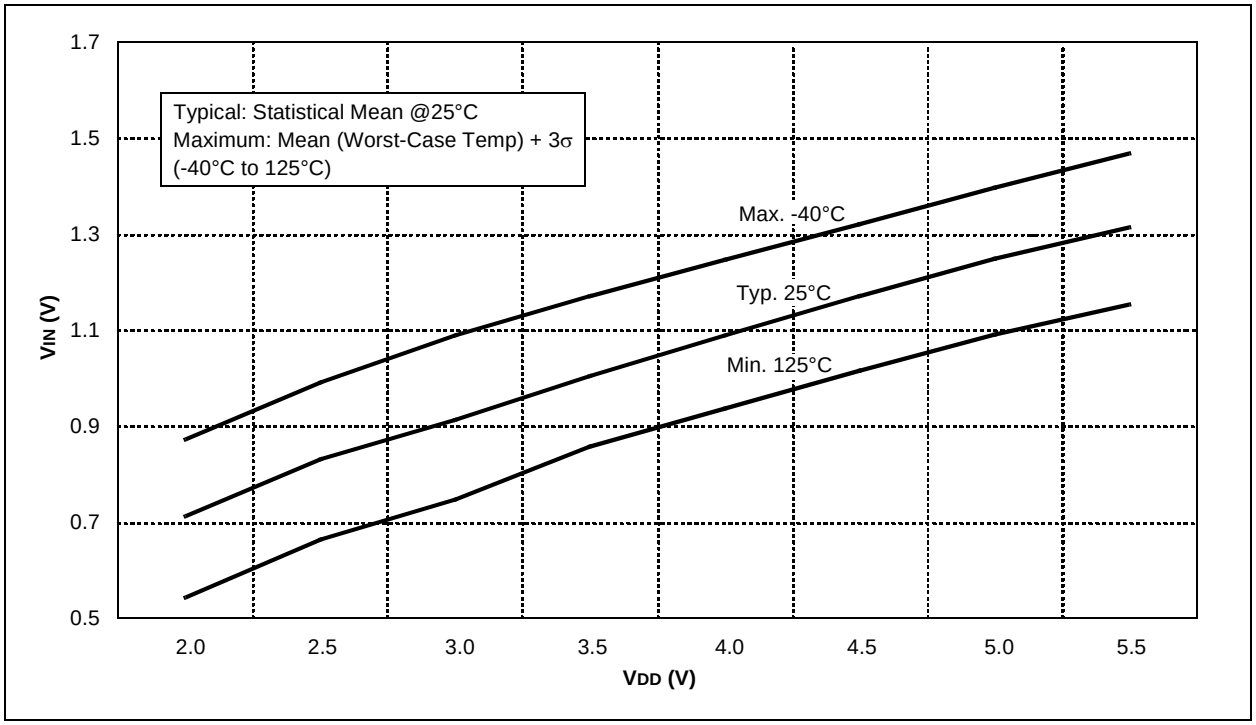


FIGURE 17-38: TTL INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE



INDEX

A

A/D
- Specifications ... 164, 165

Absolute Maximum Ratings ... 143

AC Characteristics
- Industrial and Extended ... 156
- Load Conditions ... 155

ADC
- Acquisition Requirements ... 86
- Associated registers ... 88
- Block Diagram ... 79
- Calculating Acquisition Time ... 86
- Channel Selection ... 80
- Configuration ... 80
- Configuring Interrupt ... 83
- Conversion Clock ... 80
- Conversion Procedure ... 83
- Internal Sampling Switch (RSS) Impedance ... 86
- Interrupts ... 81
- Operation ... 82
- Operation During Sleep ... 82
- Port Configuration ... 80
- Reference Voltage (VREF) ... 80
- Result Formatting ... 82
- Source Impedance ... 86
- Special Event Trigger ... 82
- Starting an A/D Conversion ... 82

ADC (PIC12F615/617/HV615 Only) ... 79

ADCON0 Register ... 84

ADRESH Register (ADFM = 0) ... 85

ADRESH Register (ADFM = 1) ... 85

ADRESL Register (ADFM = 0) ... 85

ADRESL Register (ADFM = 1) ... 85

Analog Input Connection Considerations ... 68

Analog-to-Digital Converter. *See* ADC

ANSEL Register (PIC12F609/HV609) ... 45

ANSEL Register (PIC12F615/617/HV615) ... 45

APFCON Register ... 24

Assembler
- MPASM Assembler ... 140

B

Block Diagrams
- (CCP) Capture Mode Operation ... 90
- ADC ... 79
- ADC Transfer Function ... 87
- Analog Input Model ... 68, 87
- Auto-Shutdown ... 101
- CCP PWM ... 94
- Clock Source ... 37
- Comparator ... 67
- Compare ... 92
- Crystal Operation ... 39
- External RC Mode ... 40
- GP0 and GP1 Pins ... 47
- GP2 Pins ... 48
- GP3 Pin ... 49
- GP4 Pin ... 50
- GP5 Pin ... 51
- In-Circuit Serial Programming Connections ... 125
- Interrupt Logic ... 119
- MCLR Circuit ... 111
- On-Chip Reset Circuit ... 110
- PIC12F609/12HV609 ... 7
- PIC12F615/617/12HV615 ... 8
- PWM (Enhanced) ... 97
- Resonator Operation ... 39
- Timer1 ... 57, 58
- Timer2 ... 65
- TMR0/WDT Prescaler ... 53
- Watchdog Timer ... 122

Brown-out Reset (BOR) ... 112
- Associated Registers ... 113
- Specifications ... 160
- Timing and Characteristics ... 159

C

C Compilers
- MPLAB C18 ... 140
- MPLAB C30 ... 140

Calibration Bits ... 109

Capture Module. *See* Enhanced Capture/Compare/PWM (ECCP)

Capture/Compare/PWM (CCP)
- Associated registers w/ Capture ... 91
- Associated registers w/ Compare ... 93
- Associated registers w/ PWM ... 105
- Capture Mode ... 90
- CCP1 Pin Configuration ... 90
- Compare Mode ... 92
  - CCP1 Pin Configuration ... 92
  - Software Interrupt Mode ... 90, 92
  - Special Event Trigger ... 92
  - Timer1 Mode Selection ... 90, 92
- Prescaler ... 90
- PWM Mode ... 94
  - Duty Cycle ... 95
  - Effects of Reset ... 96
  - Example PWM Frequencies and Resolutions, 20 MHZ ... 95
  - Example PWM Frequencies and Resolutions, 8 MHz ... 95
  - Operation in Sleep Mode ... 96
  - Setup for Operation ... 96
  - System Clock Frequency Changes ... 96
- PWM Period ... 95
- Setup for PWM Operation ... 96

CCP1CON (Enhanced) Register ... 89

Clock Sources
- External Modes ... 38
  - EC ... 38
  - HS ... 39
  - LP ... 39
  - OST ... 38
  - RC ... 40
  - XT ... 39
- Internal Modes ... 40
  - INTOSC ... 40
  - INTOSCIO ... 40

CMCON0 Register ... 72

CMCON1 Register ... 73

Code Examples
- A/D Conversion ... 83
- Assigning Prescaler to Timer0 ... 54
- Assigning Prescaler to WDT ... 54
- Changing Between Capture Prescalers ... 90
- Indirect Addressing ... 25

Initializing GPIO 43
Saving Status and W Registers in RAM 121
Writing to Flash Program Memory 34
Code Protection 124
Comparator 67
Associated registers 78
Control 69
Gating Timer1 73
Operation During Sleep 71
Overview 67
Response Time 69
Synchronizing COUT w/Timer1 73
Comparator Hysteresis 77
Comparator Voltage Reference (CVREF) 74
Effects of a Reset 71
Comparator Voltage Reference (CVREF)
Response Time 69
Comparator Voltage Reference (CVREF)
Specifications 163
Comparators
C2OUT as T1 Gate 60
Effects of a Reset 71
Specifications 162
Compare Module. *See* Enhanced Capture/Compare/
PWM (ECCP) (PIC12F615/617/HV615 only)
CONFIG Register 108
Configuration Bits 107
CPU Features 107
Customer Change Notification Service 209
Customer Notification Service 209
Customer Support 209

D

Data EEPROM Memory
Associated Registers 35
Data Memory 11
DC and AC Characteristics
Graphs and Tables 171
DC Characteristics
Extended and Industrial 152
Industrial and Extended 145
Development Support 139
Device Overview 7

E

ECCP. *See* Enhanced Capture/Compare/PWM
ECCPAS Register 102
EEDAT Register 28
EEDATH Register 28
Effects of Reset
PWM mode 96
Electrical Specifications 143
Enhanced Capture/Compare/PWM (ECCP)
Enhanced PWM Mode 97
Auto-Restart 103
Auto-shutdown 101
Half-Bridge Application 99
Half-Bridge Application Examples 104
Half-Bridge Mode 99
Output Relationships (Active-High and
Active-Low) 98
Output Relationships Diagram 98
Programmable Dead Band Delay 104
Shoot-through Current 104
Start-up Considerations 100
Specifications 162
Timer Resources 89
Enhanced Capture/Compare/PWM
(PIC12F615/617/HV615 Only) 89
Errata 6

F

Firmware Instructions 129
Flash Program Memory Self Read/Self Write
Control (For PIC12F617 only) 27
Fuses. *See* Configuration Bits

G

General Purpose Register File 12
GPIO 43
Additional Pin Functions 44
ANSEL Register 44
Interrupt-on-Change 44
Weak Pull-Ups 44
Associated registers 52
GP0 47
GP1 47
GP2 48
GP3 49
GP4 50
GP5 51
Pin Descriptions and Diagrams 47
Specifications 158
GPIO Register 43

H

High Temperature Operation 167

I

ID Locations 124
In-Circuit Debugger 125
In-Circuit Serial Programming (ICSP) 125
Indirect Addressing, INDF and FSR registers 25
Instruction Format 129
Instruction Set 129
ADDLW 131
ADDWF 131
ANDLW 131
ANDWF 131
MOVF 134
BCF 131
BSF 131
BTFSC 131
BTFSS 132
CALL 132
CLRF 132
CLRW 132
CLRWDT 132
COMF 132
DECF 132
DECFSZ 133
GOTO 133
INCF 133
INCFSZ 133
IORLW 133
IORWF 133
MOVLW 134
MOVWF 134
NOP 134
RETFIE 135
RETLW 135
RETURN 135

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/05/10