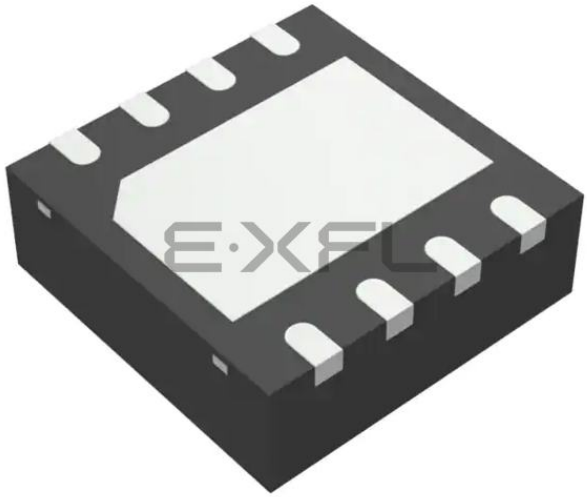

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f615-h-md

TABLE 2-1: PIC12F609/HV609 SPECIA L FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25, 115
01h	TMR0	Timer0 Module s Register								xxxx xxxx	53, 115
02h	PCL	Program Counter s (PC) Least Significant Byte								0000 0000	25, 115
03h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18, 115
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	25, 115
05h	GPIO			GP5	GP4	GP3	GP2	GP1	GP0	--x0 x000	43, 115
06h		Unimplemented									
07h		Unimplemented									
08h		Unimplemented									
09h		Unimplemented									
0Ah	PCLATH				Write Buffer for upper 5 bits of Program Counter					---0 0000	25, 115
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	20, 115
0Ch	PIR1					CMIF			TMR1IF	---- 0--0	22, 115
0Dh		Unimplemented									
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 115
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 115
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	62, 115
11h		Unimplemented									
12h		Unimplemented									
13h		Unimplemented									
14h		Unimplemented									
15h		Unimplemented									
16h		Unimplemented									
17h		Unimplemented									
18h		Unimplemented									
19h	VRCON	CMVREN		VRR	FVREN	VR3	VR2	VR1	VR0	0-00 0000	76, 116
1Ah	CMCON0	CMON	COUT	CMOE	CMPOL		CMR		CMCH	0000 -0-0	72, 116
1Bh											
1Ch	CMCON1				T1ACS	CMHYS		T1GSS	CMSYNC	---0 0-10	73, 116
1Dh		Unimplemented									
1Eh		Unimplemented									
1Fh		Unimplemented									

Legend: = Unimplemented locations read as 0 , u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: Read only register.

9.8 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See Section 7.0 Timer1 Module with Gate Control for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

9.9 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 7-1) for more information.

REGISTER 9-2: CMCON1: COMPARATOR CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0
			T1ACS	CMHYS		T1GSS	CMSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as 0	
-n = Value at POR	1 = Bit is set	0 = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: Read as 0

bit 4 T1ACS: Timer1 Alternate Clock Select bit
1 = Timer 1 Clock Source is System Clock (FOSC)
0 = Timer 1 Clock Source is Instruction Clock (FOSC\4)

bit 3 CMHYS: Comparator Hysteresis Select bit
1 = Comparator Hysteresis enabled
0 = Comparator Hysteresis disabled

bit 2 Unimplemented: Read as 0

bit 1 T1GSS: Timer1 Gate Source Select bit(1)
1 = Timer 1 Gate Source is $\overline{T1G}$ pin (pin should be configured as digital input)
0 = Timer 1 Gate Source is comparator output

bit 0 CMSYNC: Comparator Output Synchronization bit(2)
1 = Output is synchronized with falling edge of Timer1 clock
0 = Output is asynchronous

Note 1: Refer to Section 7.6 Timer1 Gate .
2: Refer to Figure 9-2.

11.3.1 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 11-1.

EQUATION 11-1: PWM PERIOD

$$PWM\ Period = [(PR2 + 1) \times 4 \times T_{OSC}] \times (TMR2\ Prescale\ Value)$$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

Note:	The Timer2 postscaler (see Section 8.1 Timer2 Operation) is not used in the determination of the PWM frequency.

11.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the DC1B<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 11-2 is used to calculate the PWM pulse width.

Equation 11-3 is used to calculate the PWM duty cycle ratio.

EQUATION 11-2: PULSE WIDTH

$$Pulse\ Width = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \times T_{OSC} \times (TMR2\ Prescale\ Value)$$

EQUATION 11-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{CCPR1L{:}CCP1CON\langle 5{:}4\rangle}{4\,(PR2 + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 11-3).

11.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 11-4.

EQUATION 11-4: PWM RESOLUTION

$$Resolution = \frac{\log[4\,(PR2 + 1)]}{\log(2)}\ bits$$

Note:	If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 11-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (F OSC = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 11-5: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (F OSC = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1

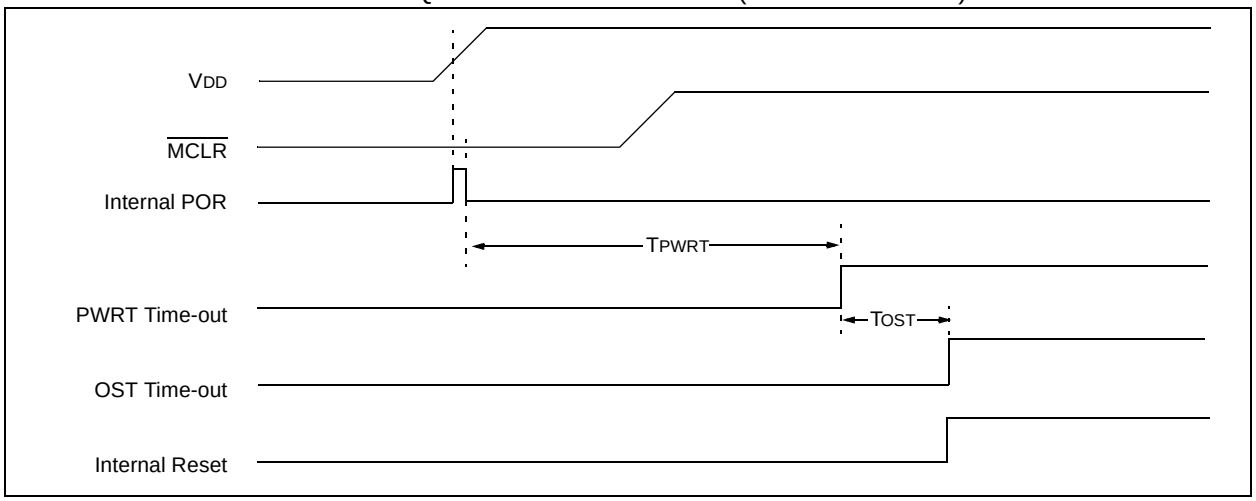


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 2

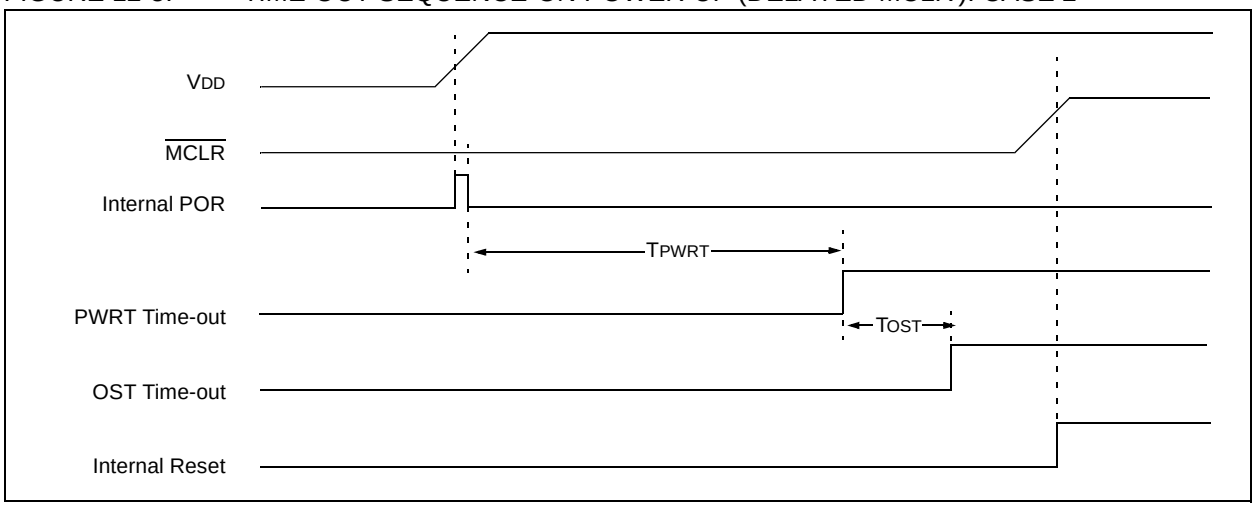
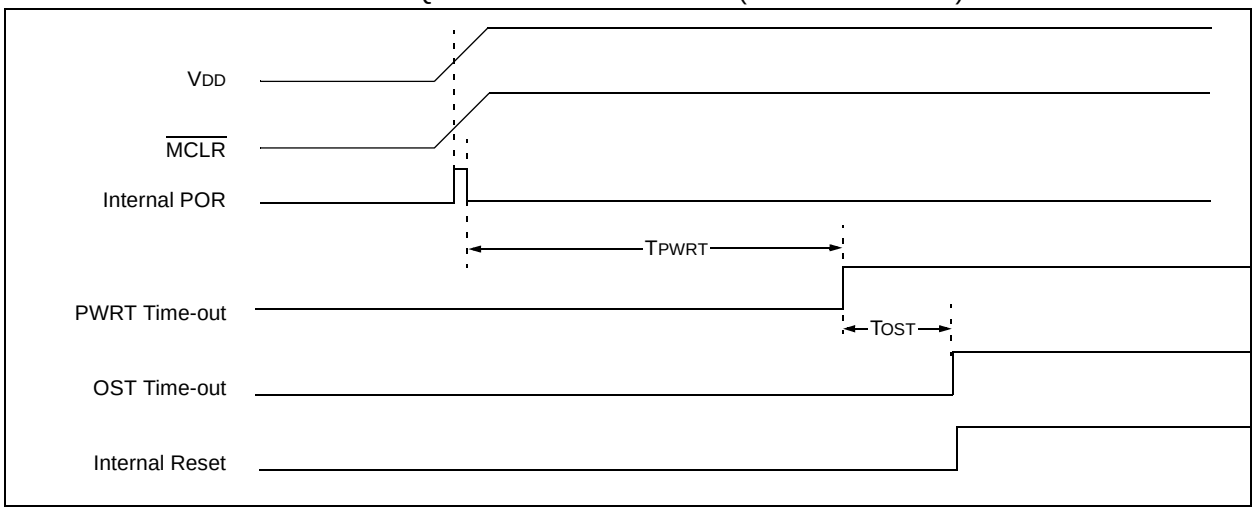


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD)



NOTES:

DECFSZ	Decrement f, Skip if 0
Syntax:	[*label*] DECFSZ f,d
Operands:	0 df d127 d [0,1]
Operation:	(f) - 1 o (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register f are decremented. If d is 0 , the result is placed in the W register. If d is 1 , the result is placed back in register f . If the result is 1 , the next instruction is executed. If the result is 0 , then a NOPis executed instead, making it a two-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[*label*] GOTO k
Operands:	0 dk d2047
Operation:	k o PC<10:0> PCLATH<4:3> o PC<12:11>
Status Affected:	None
Description:	GOTOis an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTOis a two-cycle instruction.

INCF	Increment f
Syntax:	[*label*] INCF f,d
Operands:	0 df d127 d [0,1]
Operation:	(f) + 1 o (destination)
Status Affected:	Z
Description:	The contents of register f are incremented. If d is 0 , the result is placed in the W register. If d is 1 , the result is placed back in register f .

INCFSZ	Increment f, Skip if 0
Syntax:	[*label*] INCFSZ f,d
Operands:	0 df d127 d [0,1]
Operation:	(f) + 1 o (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register f are incremented. If d is 0 , the result is placed in the W register. If d is 1 , the result is placed back in register f . If the result is 1 , the next instruction is executed. If the result is 0 , a NOPis executed instead, making it a two-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[*label*] IORLW k
Operands:	0 dk d255
Operation:	(W) .OR. k o (W)
Status Affected:	Z
Description:	The contents of the W register are OR ed with the eight-bit literal k . The result is placed in the W register.

IORWF	Inclusive OR W with f
Syntax:	[*label*] IORWF f,d
Operands:	0 df d127 d [0,1]
Operation:	(W) .OR. (f) o (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register f . If d is 0 , the result is placed in the W register. If d is 1 , the result is placed back in register f .

TABLE 16-14: DC CHARACTERISTICS FOR I_{DD} SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						V_{DD}	Note
D010	Supply Current (I_{DD})	µA		13	58	2.0	I_{DD} LP OSC (32 kHz)
				19	67	3.0	
				32	92	5.0	
D011		µA		135	316	2.0	I_{DD} XT OSC (1 MHz)
				185	400	3.0	
				300	537	5.0	
D012		µA		240	495	2.0	I_{DD} XT OSC (4 MHz)
				360	680	3.0	
		mA		0.660	1.20	5.0	
D013		µA		75	158	2.0	I_{DD} EC OSC (1 MHz)
				155	338	3.0	
				345	792	5.0	
D014		µA		185	357	2.0	I_{DD} EC OSC (4 MHz)
				325	625	3.0	
		mA		0.665	1.30	5.0	
D016		µA		245	476	2.0	I_{DD} INTOSC (4 MHz)
				360	672	3.0	
				620	1.10	5.0	
D017		µA		395	757	2.0	I_{DD} INTOSC (8 MHz)
		mA		0.620	1.20	3.0	
				1.20	2.20	5.0	
D018		µA		175	332	2.0	I_{DD} EXTRC (4 MHz)
				285	518	3.0	
				530	972	5.0	
D019		mA		2.20	4.10	4.5	I_{DD} HS OSC (20 MHz)
				2.80	4.80	5.0	

FIGURE 17-45: TYPICAL HFIN TOSC FREQUENCY CHANGE vs. VDD (125°C)

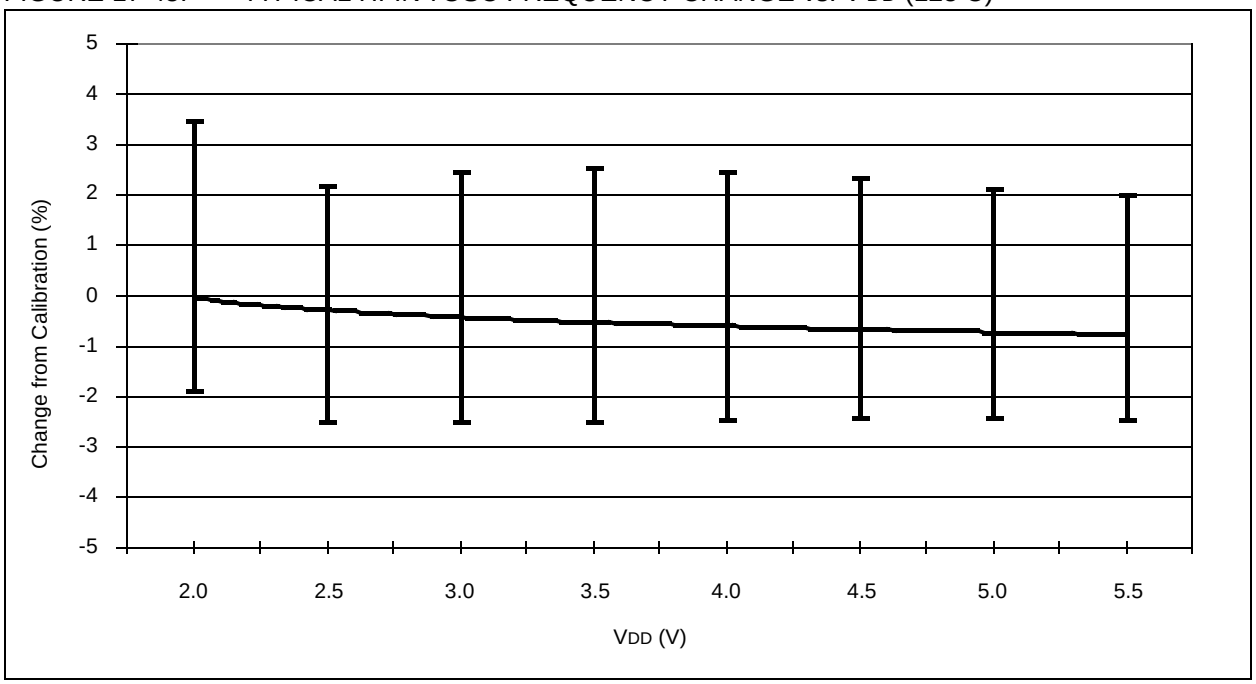


FIGURE 17-46: TYPICAL HFIN TOSC FREQUENCY CHANGE vs. VDD (-40°C)

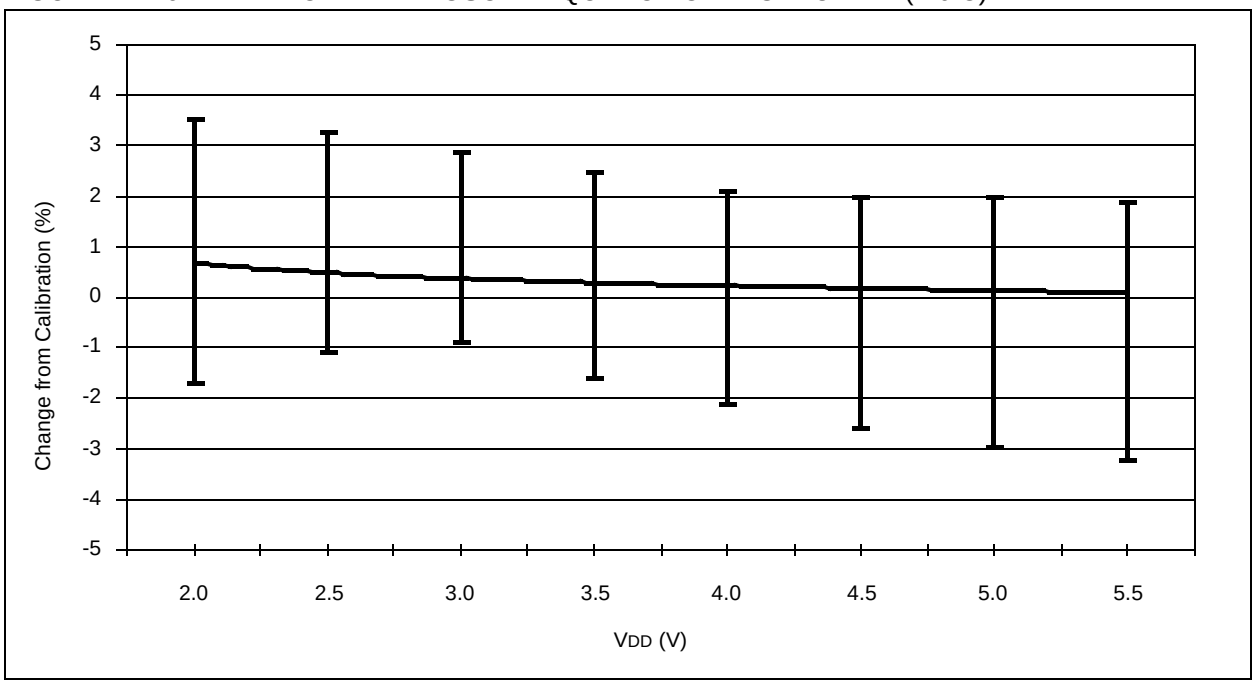


FIGURE 17-52: COMPARATOR RESPONSE TIME (FALLING EDGE)

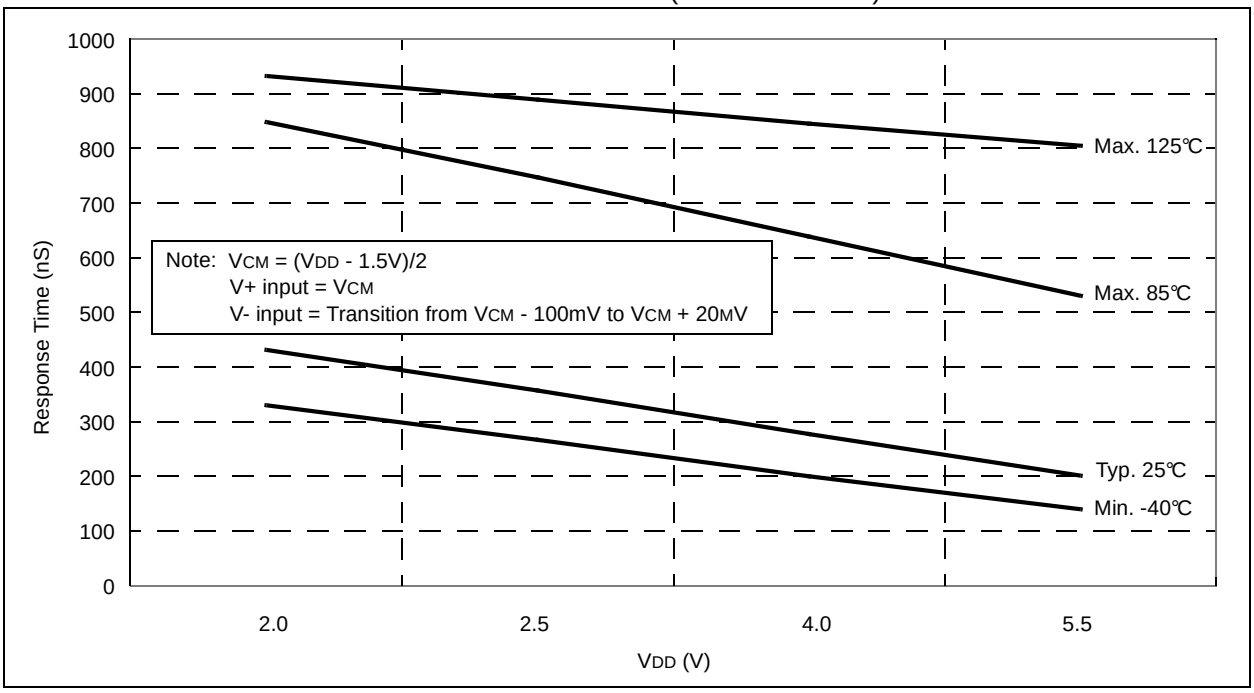


FIGURE 17-53: WDT TIME-OUT PERIOD vs. VDD OVER TEMPERATURE