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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f615-h-sn

1.0 DEVICE OVERVIEW

The PIC12F609/615/617/12HV609/615 devices are covered by this data sheet. They are available in 8-pin PDIP, SOIC, MSOP and DFN packages.

Block Diagrams and pinout descriptions of the devices are as follows:

- PIC12F609/HV609 (Figure 1-1, Table 1-1)
- PIC12F615/617/HV615 (Figure 1-2, Table 1-2)

FIGURE 1-1: PIC12F609/HV609 BLOCK DIAGRAM

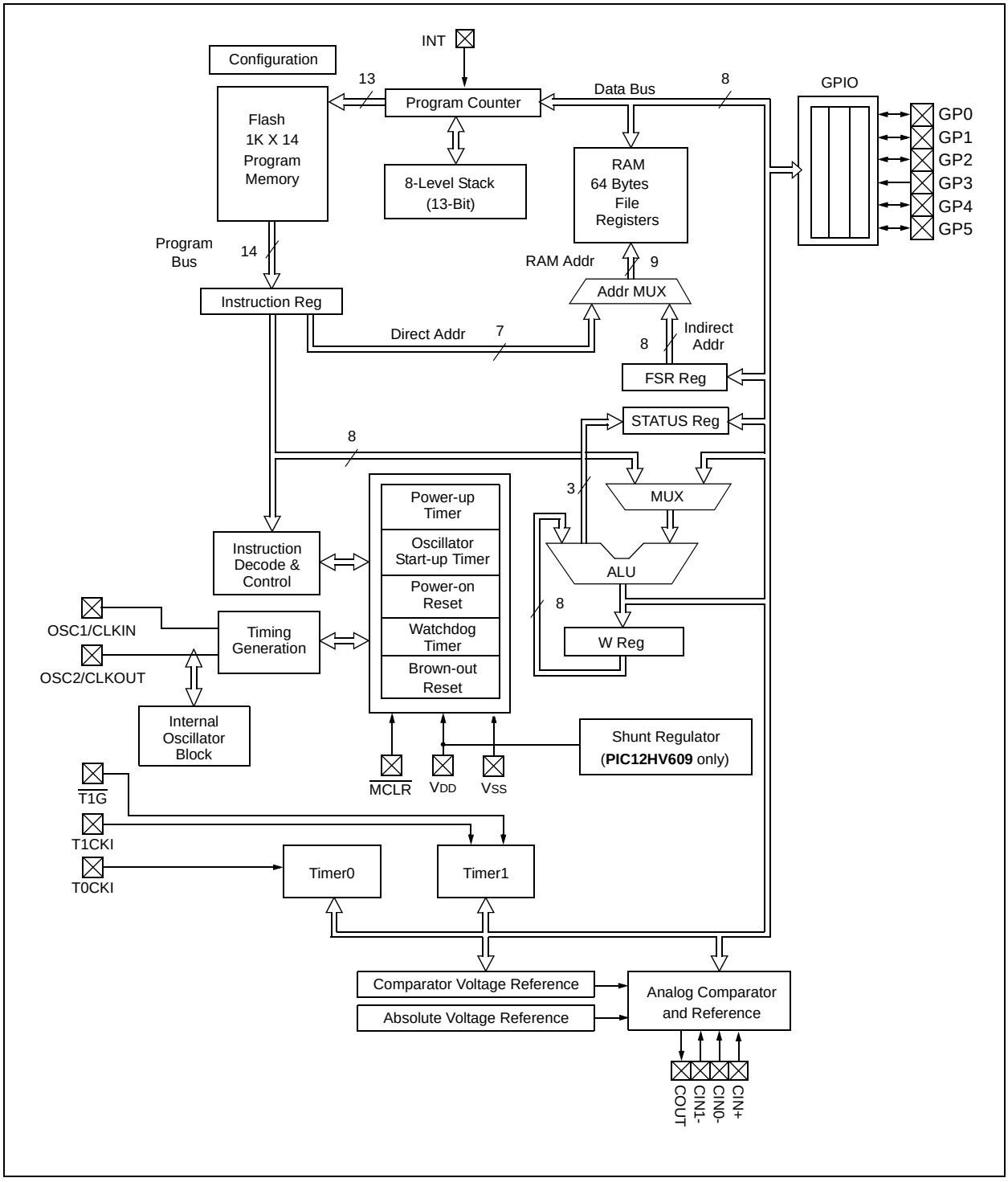


TABLE 2-2: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25, 116
01h	TMR0	Timer0 Module's Register								xxxx xxxx	53, 116
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	25, 116
03h	STATUS	IRP(1)	RP1(1)	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18, 116
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	25, 116
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--x0 x000	43, 116
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					---0 0000	25, 116
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	20, 116
0Ch	PIR1	—	ADIF	CCP1IF	—	CMIF	—	TMR2IF	TMR1IF	-00- 0-00	22, 116
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 116
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 116
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	62, 116
11h	TMR2(3)	Timer2 Module Register								0000 0000	65, 116
12h	T2CON(3)	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	66, 116
13h	CCPR1L(3)	Capture/Compare/PWM Register 1 Low Byte								XXXX XXXX	90, 116
14h	CCPR1H(3)	Capture/Compare/PWM Register 1 High Byte								XXXX XXXX	90, 116
15h	CCP1CON(3)	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	89, 116
16h	PWM1CON(3)	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000	105, 116
17h	ECCPAS(3)	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000	102, 116
18h	—	Unimplemented								—	—
19h	VRCON	CMVREN	—	VRR	FVREN	VR3	VR2	VR1	VR0	0-00 0000	76, 116
1Ah	CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -0-0	72, 116
1Bh	—					—		—		—	—
1Ch	CMCON1	—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC	---0 0-10	73, 116
1Dh	—	Unimplemented								—	—
1Eh	ADRESH(2, 3)	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	85, 116
1Fh	ADCON0(3)	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	00-0 0000	84, 116

Legend: – = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: Read only register.

3: PIC12F615/617/HV615 only.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the Reset status
- the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS,` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `'000u u1uu'` (where u = unchanged).

It is recommended, therefore, that only `BCF, BSF, SWAPF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 14.0 "Instruction Set Summary"**.

Note 1:	Bits IRP and RP1 of the STATUS register are not used by the PIC12F609/615/617/12HV609/615 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
2:	The C and DC bits operate as a $\overline{Borrow}$ and Digit $\overline{Borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IRP:** This bit is reserved and should be maintained as '0'

bit 6 **RP1:** This bit is reserved and should be maintained as '0'

bit 5 **RP0:** Register Bank Select bit (used for direct addressing)
1 = Bank 1 (80h – FFh)
0 = Bank 0 (00h – 7Fh)

bit 4 **$\overline{TO}$:** Time-out bit
1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$:** Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{Borrow}$ bit (`ADDWF, ADDLW, SUBLW, SUBWF` instructions), For $\overline{Borrow}$, the polarity is reversed.
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{Borrow}$ bit(1) (`ADDWF, ADDLW, SUBLW, SUBWF` instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For $\overline{Borrow}$, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF, RLF`) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.2.2.5 PIR1 Register

The PIR1 register contains the Peripheral Interrupt flag bits, as shown in Register 2-5.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIF:** A/D Interrupt Flag bit(1)
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started

bit 5 **CCP1IF:** CCP1 Interrupt Flag bit(1)
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Unused in this mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CMIF:** Comparator Interrupt Flag bit
1 = Comparator output has changed (must be cleared in software)
0 = Comparator output has not changed

bit 2 **Unimplemented:** Read as '0'

bit 1 **TMR2IF:** Timer2 to PR2 Match Interrupt Flag bit(1)
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed

Note 1: PIC12F615/617/HV615 only. PIC12F609/HV609 unimplemented, read as '0'.

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2(1)	ADCS1(1)	ADCS0(1)	ANS3	ANS2(1)	ANS1	ANS0	-000 1111	-000 1111
CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -0-0	0000 -0-0
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--u0 u000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
WPU	—	—	WPU5	WPU4	WPU3	WPU2	WPU1	WPU0	--11 1111	--11 -111
T1CON	T1GINV	TMR1GE	TICKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
CCP1CON(1)	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	0-00 0000
APFCON(1)	—	—	—	T1GSEL	—	—	P1BSEL	P1ASEL	---0 --00	---0 --00

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by GPIO.
Note 1: PIC12F615/617/HV615 only.

REGISTER 6-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{\text{GPPU}}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TMR0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000x
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

NOTES:

REGISTER 9-1: CMCON0: COMPARATOR CONTROL REGISTER 0

R/W-0	R-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0
CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CMON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 6 **COUT:** Comparator Output bit
If C1POL = 1 (inverted polarity):
COUT = 0 when $CMV_{IN}+ > CMV_{IN}-$
COUT = 1 when $CMV_{IN}+ < CMV_{IN}-$
If C1POL = 0 (non-inverted polarity):
COUT = 1 when $CMV_{IN}+ > CMV_{IN}-$
COUT = 0 when $CMV_{IN}+ < CMV_{IN}-$

bit 5 **CMOE:** Comparator Output Enable bit
1 = COUT is present on the COUT pin(1)
0 = COUT is internal only

bit 4 **CMPOL:** Comparator Output Polarity Select bit
1 = COUT logic is inverted
0 = COUT logic is not inverted

bit 3 **Unimplemented:** Read as '0'

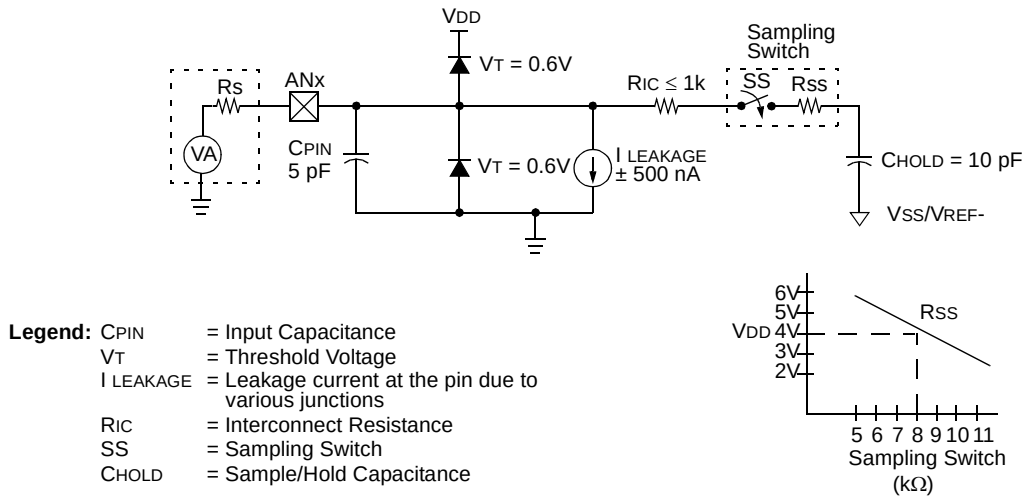
bit 2 **CMR:** Comparator Reference Select bit (non-inverting input)
1 = $CMV_{IN}+$ connects to CMV_{REF} output
0 = $CMV_{IN}+$ connects to CIN+ pin

bit 1 **Unimplemented:** Read as '0'

bit 0 **CMCH:** Comparator C1 Channel Select bit
0 = $CMV_{IN}-$ pin of the Comparator connects to CIN0-
1 = $CMV_{IN}-$ pin of the Comparator connects to CIN1-

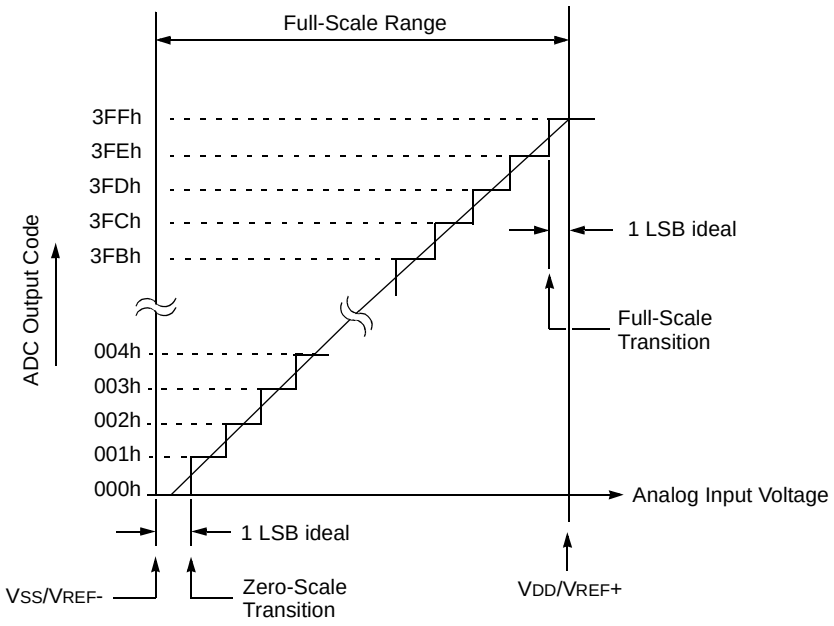
Note 1: Comparator output requires the following three conditions: CMOE = 1, CMON = 1 and corresponding port TRIS bit = 0.

FIGURE 10-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
VT = Threshold Voltage
I LEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
SS = Sampling Switch
CHOLD = Sample/Hold Capacitance

FIGURE 10-5: ADC TRANSFER FUNCTION



11.4 PWM (Enhanced Mode)

The Enhanced PWM Mode can generate a PWM signal on up to four different output pins with up to 10-bits of resolution. It can do this through four different PWM output modes:

- Single PWM
- Half-Bridge PWM

To select an Enhanced PWM mode, the P1M bits of the CCP1CON register must be set appropriately.

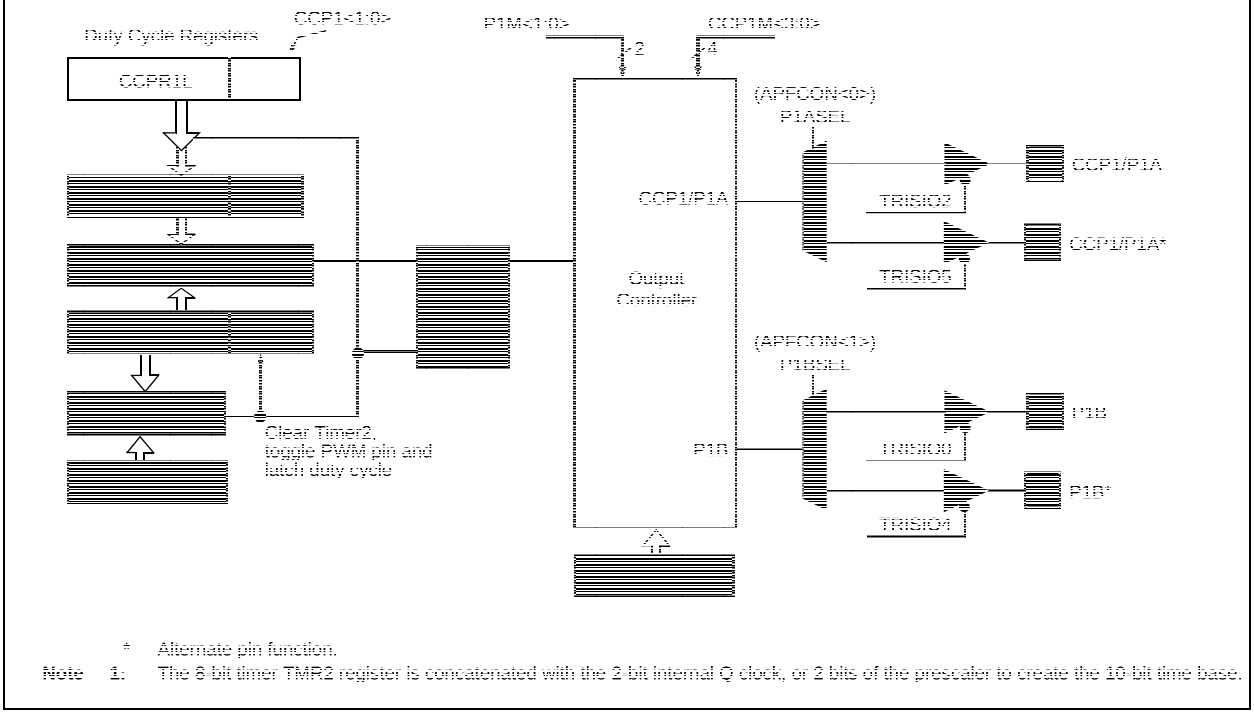
The PWM outputs are multiplexed with I/O pins and are designated P1A and P1B. The polarity of the PWM pins is configurable and is selected by setting the CCP1M bits in the CCP1CON register appropriately.

Table 11-6 shows the pin assignments for each Enhanced PWM mode.

Figure 11-5 shows an example of a simplified block diagram of the Enhanced PWM module.

Note:	To prevent the generation of an incomplete waveform when the PWM is first enabled, the ECCP module waits until the start of a new PWM period before generating a PWM signal.

FIGURE 11-5: EXAMPLE SIMPLIFIED BLOCK DIAGRAM OF THE ENHANCED PWM MODE



* Alternate pin function.

Note 1: The 8 bit timer TMR2 register is concatenated with the 2 bit internal Q clock, or 2 bits of the prescaler to create the 10 bit time base.

Note 1:	The TRIS register value for each PWM output must be configured appropriately.
2:	Clearing the CCP1CON register will relinquish ECCP control of all PWM output pins.
3:	Any pin not used by an Enhanced PWM mode is available for alternate pin functions.

TABLE 11-6: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	P1M<1:0>	CCP1/P1A	P1B
Single	00	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes

NOTES:

14.2 Instruction Descriptions

ADDLW	Add literal and W
Syntax:	[*label*] ADDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) + k → (W)
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded, and a NOP is executed instead, making this a two-cycle instruction.

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - 1 → (destination);
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction.

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 2047$

Operation: k → PC<10:0>
PCLATH<4:3> → PC<12:11>

Status Affected: None

Description: GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (destination)

Status Affected: Z

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) + 1 → (destination),
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.
If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction.

IORLW **Inclusive OR literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → (W)

Status Affected: Z

Description: The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .OR. (f) → (destination)

Status Affected: Z

Description: Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

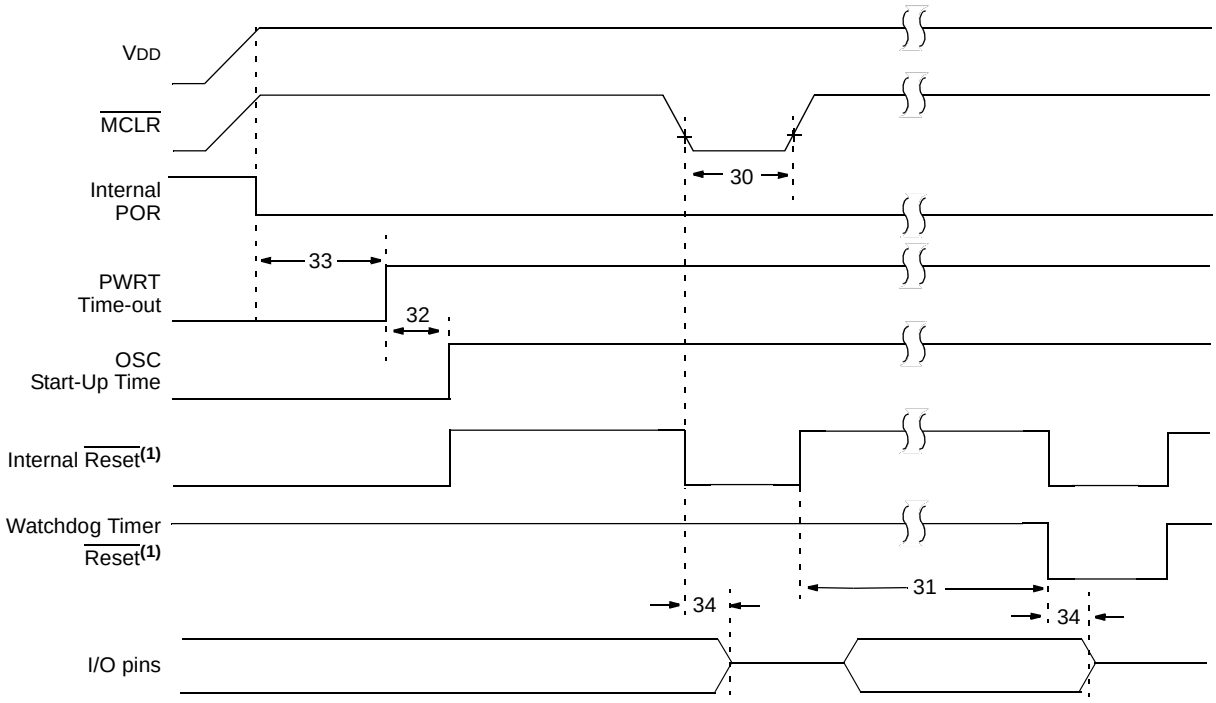
RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
Example:	`RETFIE` After Interrupt PC = TOS GIE = 1

RETLW	Return with literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2

Example:	`CALL TABLE;W contains`
	`;table offset`
	`;value`
	`GOTO DONE`
	`TABLE`
	•
	•
	`ADDWF PC ;W = offset`
	`RETLW k1 ;Begin table`
	`RETLW k2 ;`
	•
	•
	•
	`RETLW kn ;End of table`
	`DONE`
	Before Instruction
	W = 0x07
	After Instruction
	W = value of k8

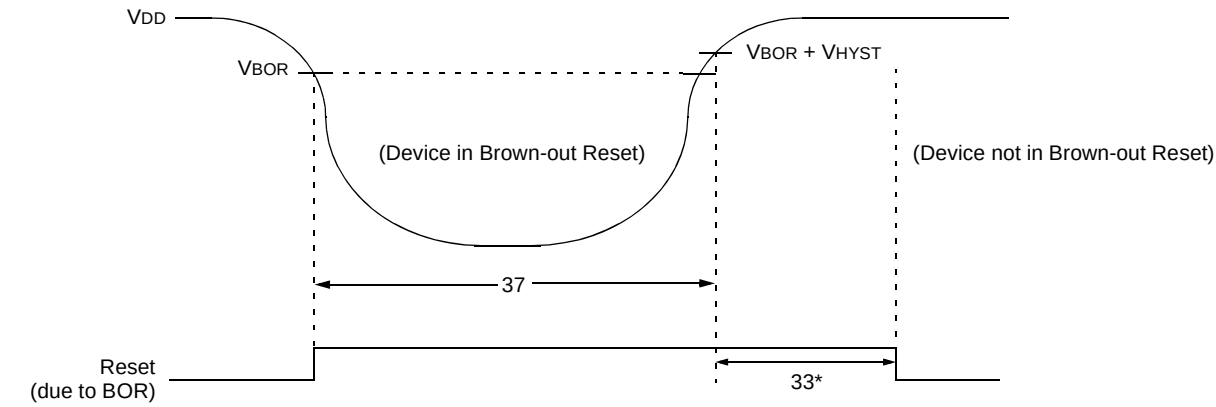
RETURN	Return from Subroutine
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

FIGURE 16-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

FIGURE 16-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS



* 64 ms delay only if PWRTE bit in the Configuration Word register is programmed to '0'.

TABLE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2 5	— —	— —	μs μs	VDD = 5V, -40°C to +85°C VDD = 5V, -40°C to +125°C
31*	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	20 20	30 35	ms ms	VDD = 5V, -40°C to +85°C VDD = 5V, -40°C to +125°C
32	TOST	Oscillation Start-up Timer Period(1, 2)	—	1024	—	TOSC	**(NOTE 3)**
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	2.0	μs	
35	VBOR	Brown-out Reset Voltage	2.0	2.15	2.3	V	**(NOTE 4)**
36*	VHYST	Brown-out Reset Hysteresis	—	100	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	μs	VDD ≤ VBOR

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

TABLE 16-11: PIC12F615/617/HV615 A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	±1	LSb	VREF = 5.12V(5)
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V(5)
AD04	EOFF	Offset Error	—	+1.5	+2.0	LSb	VREF = 5.12V(5)
AD07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.12V(5)
AD06 AD06A	VREF	Reference Voltage(3)	2.2 2.5	—	— VDD	V	 Absolute minimum to ensure 1 LSb accuracy
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	IREF	VREF Input Current(3)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

5: VREF = 5V for PIC12HV615.

TABLE 16-14: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						VDD	Note
D010	Supply Current (IDD)	μA	—	13	58	2.0	IDD LP OSC (32 kHz)
			—	19	67	3.0	
			—	32	92	5.0	
D011		μA	—	135	316	2.0	IDD XT OSC (1 MHz)
			—	185	400	3.0	
			—	300	537	5.0	
D012		μA	—	240	495	2.0	IDD XT OSC (4 MHz)
			—	360	680	3.0	
		mA	—	0.660	1.20	5.0	
D013		μA	—	75	158	2.0	IDD EC OSC (1 MHz)
			—	155	338	3.0	
			—	345	792	5.0	
D014		μA	—	185	357	2.0	IDD EC OSC (4 MHz)
			—	325	625	3.0	
		mA	—	0.665	1.30	5.0	
D016		μA	—	245	476	2.0	IDD INTOSC (4 MHz)
			—	360	672	3.0	
			—	620	1.10	5.0	
D017		μA	—	395	757	2.0	IDD INTOSC (8 MHz)
		mA	—	0.620	1.20	3.0	
			—	1.20	2.20	5.0	
D018		μA	—	175	332	2.0	IDD EXTRC (4 MHz)
			—	285	518	3.0	
			—	530	972	5.0	
D019		mA	—	2.20	4.10	4.5	IDD HS OSC (20 MHz)
			—	2.80	4.80	5.0	

FIGURE 17-8: PIC12F609/615617 IDD EXTRC (4 MHz) vs. VDD

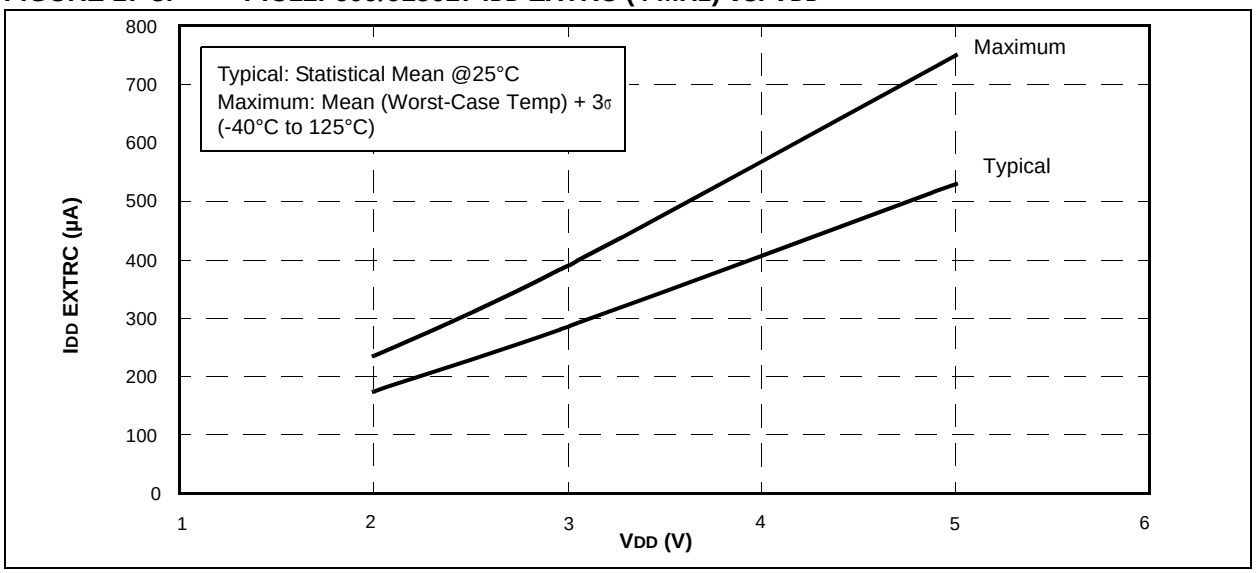
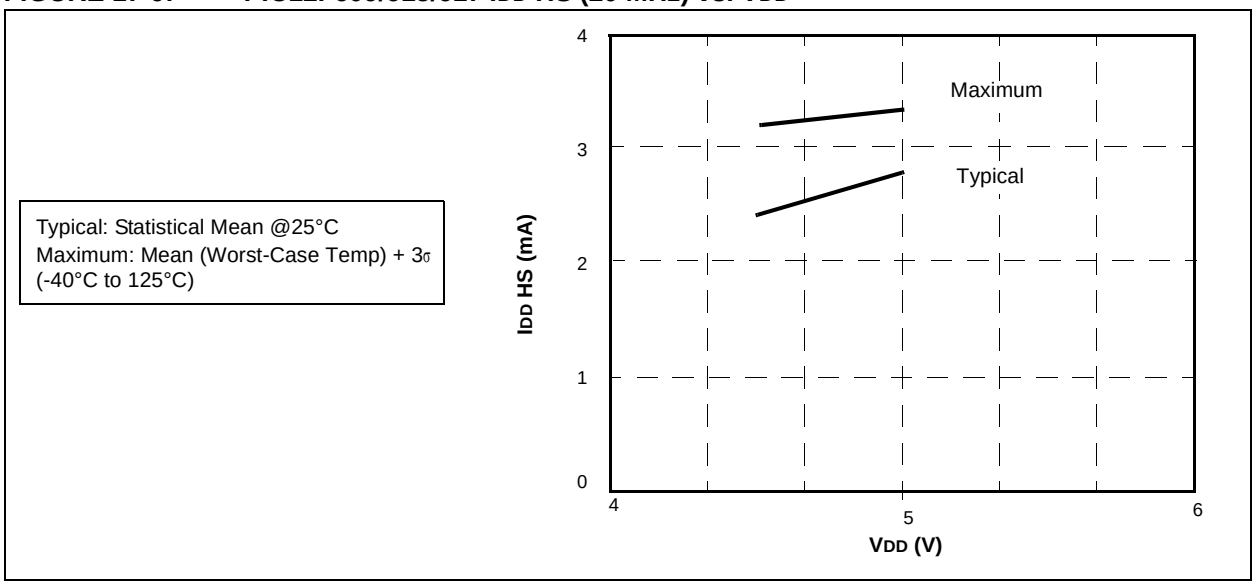
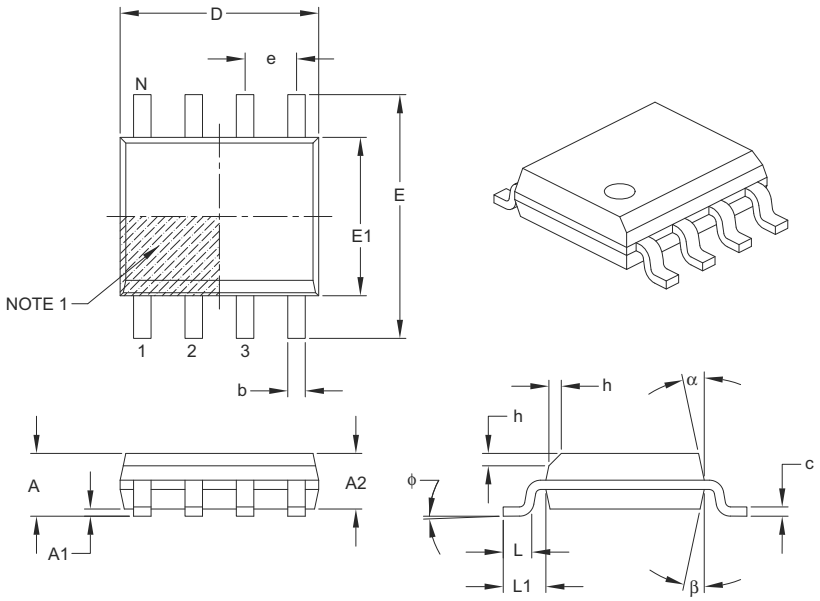


FIGURE 17-9: PIC12F609/615/617 IDD HS (20 MHz) vs. VDD



8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B