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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (4x4)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12f615t-i-md">https://www.e-xfl.com/product-detail/microchip-technology/pic12f615t-i-md</a>

# PIC12F609/615/617/12HV609/615

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# PIC12F609/615/617/12HV609/615

## 7.12 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 7-1, is used to control Timer1 and select the various features of the Timer1 module.

**REGISTER 7-1: T1CON: TIMER 1 CONTROL REGISTER**

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV <sup>(1)</sup>	TMR1GE <sup>(2)</sup>	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7      **T1GINV:** Timer1 Gate Invert bit<sup>(1)</sup>  
1 = Timer1 gate is active-high (Timer1 counts when gate is high)  
0 = Timer1 gate is active-low (Timer1 counts when gate is low)
- bit 6      **TMR1GE:** Timer1 Gate Enable bit<sup>(2)</sup>  
If TMR1ON = 0:  
This bit is ignored  
If TMR1ON = 1:  
1 = Timer1 is on if Timer1 gate is active  
0 = Timer1 is on
- bit 5-4    **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits  
11 = 1:8 Prescale Value  
10 = 1:4 Prescale Value  
01 = 1:2 Prescale Value  
00 = 1:1 Prescale Value
- bit 3      **T1OSCEN:** LP Oscillator Enable Control bit  
If INTOSC without CLKOUT oscillator is active:  
1 = LP oscillator is enabled for Timer1 clock  
0 = LP oscillator is off  
For all other system clock modes:  
This bit is ignored. LP oscillator is disabled.
- bit 2      **T1SYNC:** Timer1 External Clock Input Synchronization Control bit  
TMR1CS = 1:  
1 = Do not synchronize external clock input  
0 = Synchronize external clock input  
TMR1CS = 0:  
This bit is ignored. Timer1 uses the internal clock
- bit 1      **TMR1CS:** Timer1 Clock Source Select bit  
1 = External clock from T1CKI pin (on the rising edge)  
0 = Internal clock (FOSC/4) or system clock (FOSC)<sup>(3)</sup>
- bit 0      **TMR1ON:** Timer1 On bit  
1 = Enables Timer1  
0 = Stops Timer1

**Note 1:** T1GINV bit inverts the Timer1 gate logic, regardless of source.

**2:** TMR1GE bit must be set to use either  $\overline{T1G}$  pin or COUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.

**3:** See T1ACS bit in CMCON1 register.

## 9.6 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in the **Section 16.0 “Electrical Specifications”**. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. The comparator is turned off by clearing the CMON bit of the CMCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CMIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the *SLEEP* instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the Interrupt Service Routine.

## 9.7 Effects of a Reset

A device Reset forces the CMCON1 register to its Reset state. This sets the comparator and the voltage reference to the OFF state.

## 10.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- Port configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

### 10.1.1 PORT CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding port section for more information.

<b>Note:</b>	Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.
--------------	---

### 10.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 10.2 “ADC Operation”** for more information.

### 10.1.3 ADC VOLTAGE REFERENCE

The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either VDD or an external voltage source. The negative voltage reference is always connected to the ground reference.

### 10.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ANSEL register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 10-3.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 16.0 “Electrical Specifications”** for more information. Table 10-1 gives examples of appropriate ADC clock selections.

<b>Note:</b>	Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.
--------------	---

## 10.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
  - Disable pin output driver (See TRIS register)
  - Configure pin as analog
2. Configure the ADC module:
  - Select ADC conversion clock
  - Configure voltage reference
  - Select ADC input channel
  - Select result format
  - Turn on ADC module
3. Configure ADC interrupt (optional):
  - Clear ADC interrupt flag
  - Enable ADC interrupt
  - Enable peripheral interrupt
  - Enable global interrupt<sup>(1)</sup>
4. Wait the required acquisition time<sup>(2)</sup>.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
  - Polling the GO/DONE bit
  - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**2:** See **Section 10.3 “A/D Acquisition Requirements”**.

## EXAMPLE 10-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and GP0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL  TRISIO      ;
BSF      TRISIO,0     ;Set GP0 to input
BANKSEL  ANSEL        ;
MOVLW    B'01110001'  ;ADC Frc clock,
IORWF    ANSEL        ; and GP0 as analog
BANKSEL  ADCON0       ;
MOVLW    B'10000001'  ;Right justify,
MOVWF    ADCON0       ;Vdd Vref, AN0, On
CALL     SampleTime   ;Acquisiton delay
BSF      ADCON0,GO    ;Start conversion
BTFSC    ADCON0,GO    ;Is conversion done?
GOTO     $-1          ;No, test again
BANKSEL  ADRESH       ;
MOVF     ADRESH,W     ;Read upper 2 bits
MOVWF    RESULTHI     ;Store in GPR space
BANKSEL  ADRESL       ;
MOVF     ADRESL,W     ;Read lower 8 bits
MOVWF    RESULTLO     ;Store in GPR space
```

# PIC12F609/615/617/12HV609/615

## REGISTER 10-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits  
Upper 8 bits of 10-bit conversion result

## REGISTER 10-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits  
Lower 2 bits of 10-bit conversion result

bit 5-0 **Unimplemented**: Read as '0'

## REGISTER 10-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Unimplemented**: Read as '0'

bit 1-0 **ADRES<9:8>**: ADC Result Register bits  
Upper 2 bits of 10-bit conversion result

## REGISTER 10-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits  
Lower 8 bits of 10-bit conversion result



## 10.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 10-4. The source impedance (Rs) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 10-4.

**The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed),

an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 10-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

### EQUATION 10-1: ACQUISITION TIME EXAMPLE

*Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD*

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)] \end{aligned}$$

*The value for TC can be approximated with the following equations:*

$$V_{APPLIED} \left( 1 - \frac{1}{2047} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left( 1 - e^{\frac{-T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left( 1 - e^{\frac{-T_C}{RC}} \right) = V_{APPLIED} \left( 1 - \frac{1}{2047} \right) \quad ;\text{combining [1] and [2]}$$

*Solving for TC:*

$$\begin{aligned} T_C &= -CHOLD(R_{IC} + R_{SS} + R_S) \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

*Therefore:*

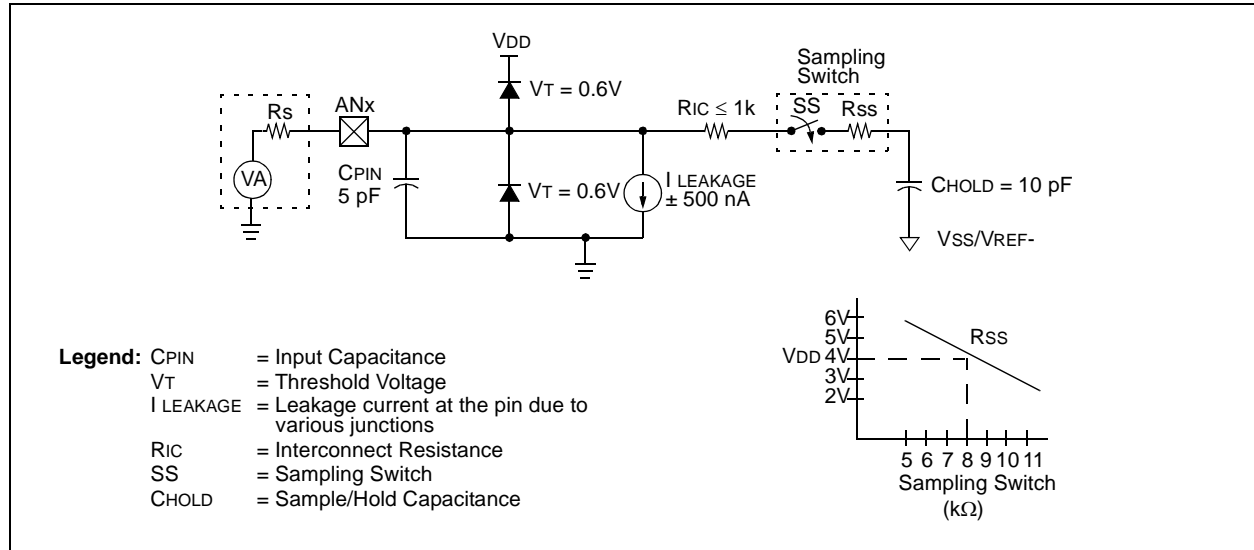
$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.37\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\ &= 4.67\mu s \end{aligned}$$

**Note 1:** The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

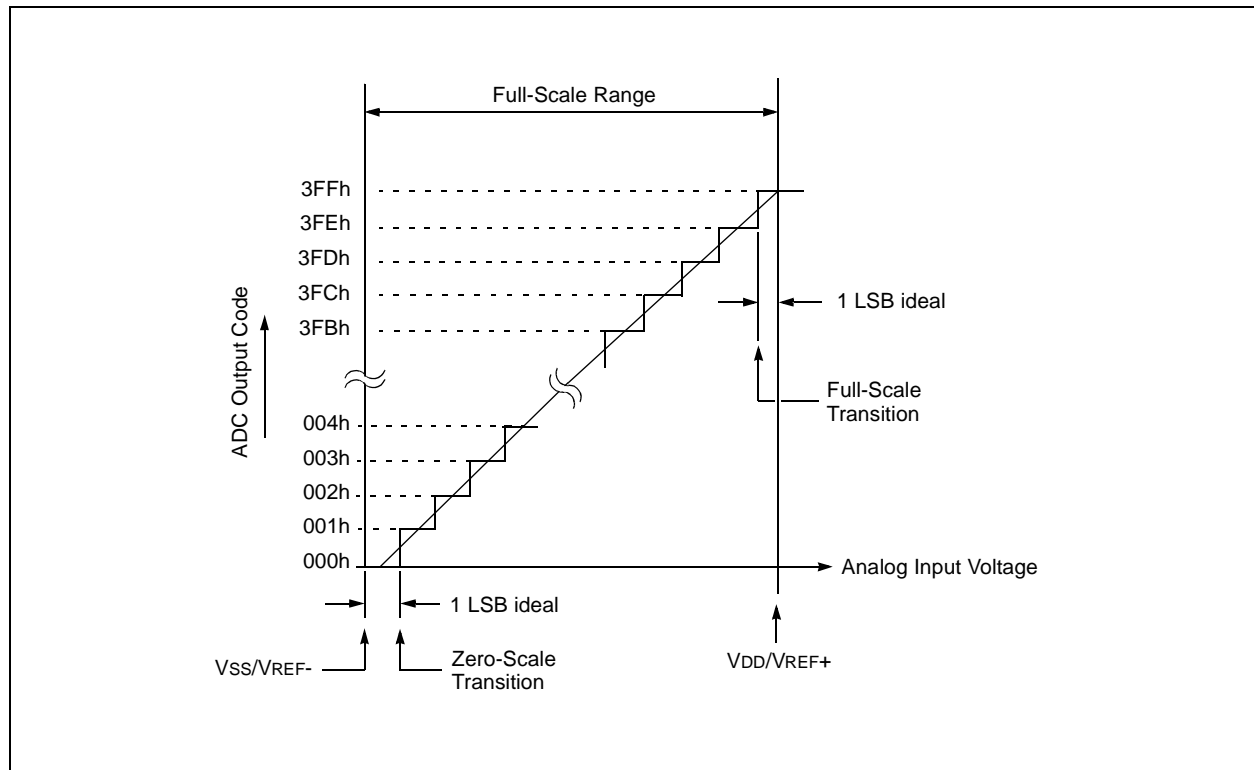
**2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.

**3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

**FIGURE 10-4: ANALOG INPUT MODEL**



**FIGURE 10-5: ADC TRANSFER FUNCTION**



# PIC12F609/615/617/12HV609/615

## 11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

**Note:** Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

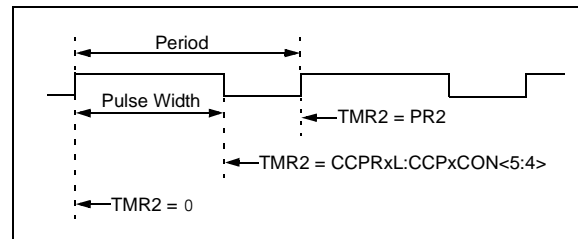
Figure 11-3 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

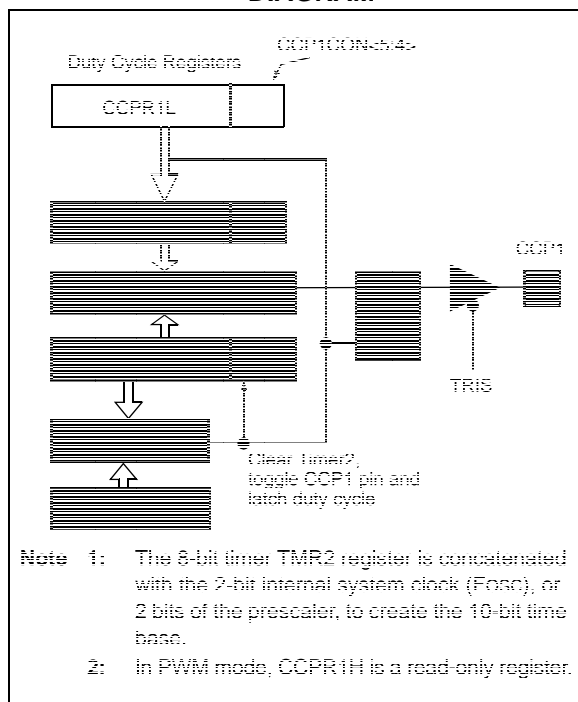
For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 11.3.7 “Setup for PWM Operation”**.

The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

**FIGURE 11-4: CCP PWM OUTPUT**



**FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM**



# PIC12F609/615/617/12HV609/615

## REGISTER 11-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7      **ECCPASE:** ECCP Auto-Shutdown Event Status bit  
1 = A shutdown event has occurred; ECCP outputs are in shutdown state  
0 = ECCP outputs are operating
- bit 6-4    **ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits  
000 = Auto-Shutdown is disabled  
001 = Comparator output change  
010 = Auto-Shutdown is disabled  
011 = Comparator output change<sup>(1)</sup>  
100 = V<sub>IL</sub> on INT pin  
101 = V<sub>IL</sub> on INT pin or Comparator change  
110 = V<sub>IL</sub> on INT pin<sup>(1)</sup>  
111 = V<sub>IL</sub> on INT pin or Comparator change
- bit 3-2    **PSSAC<1:0>:** Pin P1A Shutdown State Control bits  
00 = Drive pin P1A to '0'  
01 = Drive pin P1A to '1'  
1x = Pin P1A tri-state
- bit 1-0    **PSSBD<1:0>:** Pin P1B Shutdown State Control bits  
00 = Drive pin P1B to '0'  
01 = Drive pin P1B to '1'  
1x = Pin P1B tri-state

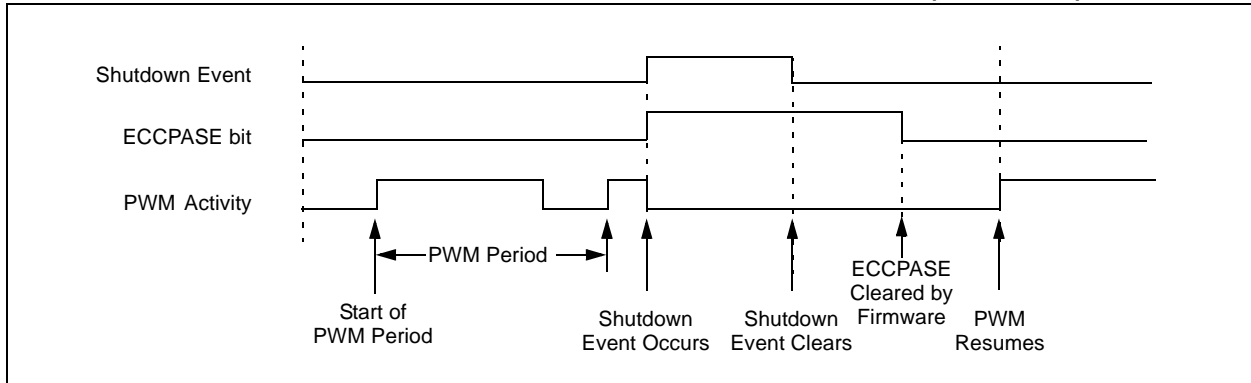
**Note 1:** If CMSYNC is enabled, the shutdown will be delayed by Timer1.

**Note 1:** The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

**2:** Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

**3:** Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.

**FIGURE 11-11: PWM AUTO-SHUTDOWN WITH FIRMWARE RESTART (PRSEN = 0)**

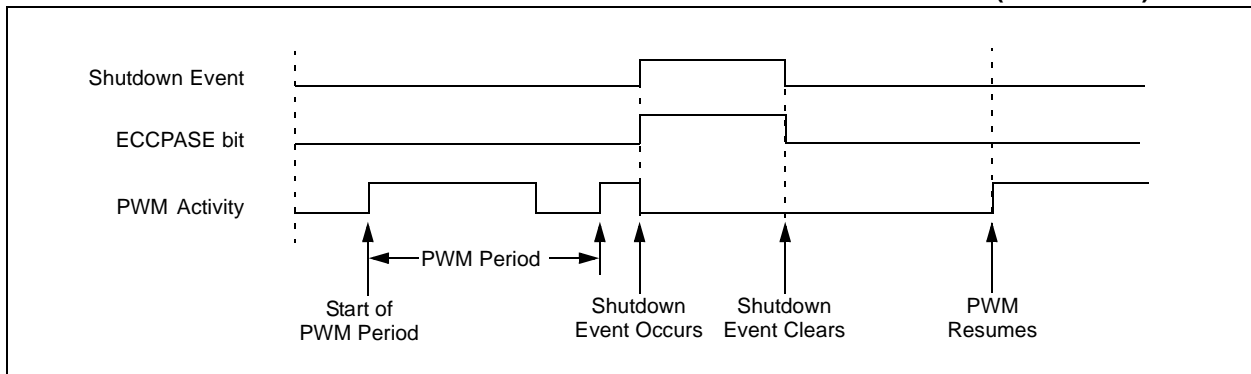


## 11.4.5 AUTO-RESTART MODE

The Enhanced PWM can be configured to automatically restart the PWM signal once the auto-shutdown condition has been removed. Auto-restart is enabled by setting the PRSEN bit in the PWM1CON register.

If auto-restart is enabled, the ECCPASE bit will remain set as long as the auto-shutdown condition is active. When the auto-shutdown condition is removed, the ECCPASE bit will be cleared via hardware and normal operation will resume.

**FIGURE 11-12: PWM AUTO-SHUTDOWN WITH AUTO-RESTART ENABLED (PRSEN = 1)**



# PIC12F609/615/617/12HV609/615

## REGISTER 12-1: CONFIG: CONFIGURATION WORD REGISTER (ADDRESS: 2007h) FOR PIC12F609/615/HV609/615 ONLY

U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	BOREN1 <sup>(1)</sup>	BOREN0 <sup>(1)</sup>	IOSCFS	$\overline{CP}$ <sup>(2)</sup>	MCLRE <sup>(3)</sup>	$\overline{PWRT}$	WDTE	FOSC2	FOSC1	FOSC0
bit 13												bit 0	

### Legend:

R = Readable bit	W = Writable bit	P = Programmable	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 13-10 **Unimplemented:** Read as '1'

bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits<sup>(1)</sup>  
 11 = BOR enabled  
 10 = BOR enabled during operation and disabled in Sleep  
 0x = BOR disabled

bit 7 **IOSCFS:** Internal Oscillator Frequency Select bit  
 1 = 8 MHz  
 0 = 4 MHz

bit 6  **$\overline{CP}$ :** Code Protection bit<sup>(2)</sup>  
 1 = Program memory code protection is disabled  
 0 = Program memory code protection is enabled

bit 5 **MCLRE:**  $\overline{MCLR}$  Pin Function Select bit<sup>(3)</sup>  
 1 =  $\overline{MCLR}$  pin function is  $\overline{MCLR}$   
 0 =  $\overline{MCLR}$  pin function is digital input,  $\overline{MCLR}$  internally tied to VDD

bit 4 **PWRT:** Power-up Timer Enable bit  
 1 = PWRT disabled  
 0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit  
 1 = WDT enabled  
 0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits  
 111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN  
 110 = RCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN  
 101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN  
 100 = INTOSCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN  
 011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN  
 010 = HS oscillator: High-speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN  
 001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN  
 000 = LP oscillator: Low-power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

- Note** 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.  
 2: The entire program memory will be erased when the code protection is turned off.  
 3: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

# PIC12F609/615/617/12HV609/615

---

**DECFSZ      Decrement f, Skip if 0**

---

Syntax:        [ *label* ] DECFSZ f,d

Operands:      $0 \leq f \leq 127$   
                  $d \in [0,1]$

Operation:      $(f) - 1 \rightarrow (\text{destination});$   
                 skip if result = 0

Status Affected: None

Description:    The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.  
                 If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a two-cycle instruction.

---

**INCFSZ      Increment f, Skip if 0**

---

Syntax:        [ *label* ] INCFSZ f,d

Operands:      $0 \leq f \leq 127$   
                  $d \in [0,1]$

Operation:      $(f) + 1 \rightarrow (\text{destination});$   
                 skip if result = 0

Status Affected: None

Description:    The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.  
                 If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a two-cycle instruction.

---

**GOTO        Unconditional Branch**

---

Syntax:        [ *label* ] GOTO k

Operands:      $0 \leq k \leq 2047$

Operation:      $k \rightarrow \text{PC}<10:0>$   
                  $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$

Status Affected: None

Description:    GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

---

**IORLW       Inclusive OR literal with W**

---

Syntax:        [ *label* ] IORLW k

Operands:      $0 \leq k \leq 255$

Operation:      $(W) .\text{OR. } k \rightarrow (W)$

Status Affected: Z

Description:    The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

---

**INCF        Increment f**

---

Syntax:        [ *label* ] INCF f,d

Operands:      $0 \leq f \leq 127$   
                  $d \in [0,1]$

Operation:      $(f) + 1 \rightarrow (\text{destination})$

Status Affected: Z

Description:    The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

---

**IORWF       Inclusive OR W with f**

---

Syntax:        [ *label* ] IORWF f,d

Operands:      $0 \leq f \leq 127$   
                  $d \in [0,1]$

Operation:      $(W) .\text{OR. } (f) \rightarrow (\text{destination})$

Status Affected: Z

Description:    Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

# PIC12F609/615/617/12HV609/615

<b>MOVF</b>	<b>Move f</b>
Syntax:	[ <i>label</i> ] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If d = 0, destination is W register. If d = 1, the destination is file register 'f' itself. d = 1 is useful to test a file register since Status flag Z is affected.
Words:	1
Cycles:	1
Example:	<pre>MOVF    FSR, 0</pre> <p>After Instruction</p> <p>W = value in FSR register</p> <p>Z = 1</p>

<b>MOVLW</b>	<b>Move literal to W</b>
Syntax:	[ <i>label</i> ] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	<pre>MOVLW    0x5A</pre> <p>After Instruction</p> <p>W = 0x5A</p>

<b>MOVWF</b>	<b>Move W to f</b>
Syntax:	[ <i>label</i> ] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	<pre>MOVW    OPTION F</pre> <p>Before Instruction</p> <p>OPTION = 0xFF W = 0x4F</p> <p>After Instruction</p> <p>OPTION = 0x4F W = 0x4F</p>

<b>NOP</b>	<b>No Operation</b>
Syntax:	[ <i>label</i> ] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	<pre>NOP</pre>



# PIC12F609/615/617/12HV609/615

## RLF Rotate Left f through Carry

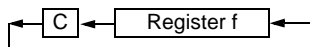
Syntax: [label] RLF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110 0110  
C = 0

After Instruction

REG1 = 1110 0110  
W = 1100 1100  
C = 1

## SLEEP Enter Sleep mode

Syntax: [label] SLEEP

Operands: None

Operation: 00h → WDT,  
0 → WDT prescaler,  
1 →  $\overline{TO}$ ,  
0 →  $\overline{PD}$

Status Affected:  $\overline{TO}$ ,  $\overline{PD}$

Description: The power-down Status bit,  $\overline{PD}$  is cleared. Time-out Status bit,  $\overline{TO}$  is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

## RRF Rotate Right f through Carry

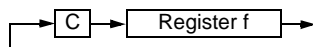
Syntax: [label] RRF f,d

Operands:  $0 \leq f \leq 127$   
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



## SUBLW Subtract W from literal

Syntax: [label] SUBLW k

Operands:  $0 \leq k \leq 255$

Operation:  $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

Result	Condition
C = 0	$W > k$
C = 1	$W \leq k$
DC = 0	$W<3:0> > k<3:0>$
DC = 1	$W<3:0> \leq k<3:0>$

## 15.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 15.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 15.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

# PIC12F609/615/617/12HV609/615

## 16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature      -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D101*	COSC2	<b>Capacitive Loading Specs on Output Pins</b> OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	Cio	All I/O pins	—	—	50	pF	
		<b>Program Flash Memory</b>					
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	Ed	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Bulk Erase/Write	4.5	—	5.5	V	
D132A	VPEW	VDD for Row Erase/Write <sup>(6)</sup>	VMIN	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 4:** This specification applies to GP3/MCLR configured as GP3 with the internal weak pull-up disabled.
- 5:** This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/MCLR. When GP3/MCLR is configured as MCLR reset pin, the weak pull-up is always enabled.
- 6:** Applies to PIC12F617 only.

## 16.12 High Temperature Operation

This section outlines the specifications for the PIC12F615 device operating in a temperature range between -40°C and 150°C.<sup>(4)</sup> The specifications between -40°C and 150°C<sup>(4)</sup> are identical to those shown in DS41288 and DS80329.

**Note 1:** Writes are **not allowed** for Flash Program Memory above 125°C.

**2:** All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.

**3:** The temperature range indicator in the part number is "H" for -40°C to 150°C.<sup>(4)</sup>

Example: PIC12F615T-H/ST indicates the device is shipped in a TAPE and reel configuration, in the MSOP package, and is rated for operation from -40°C to 150°C.<sup>(4)</sup>

**4:** AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

**TABLE 16-13: ABSOLUTE MAXIMUM RATINGS**

Parameter	Source/Sink	Value	Units
Max. Current: VDD	Source	20	mA
Max. Current: VSS	Sink	50	mA
Max. Current: PIN	Source	5	mA
Max. Current: PIN	Sink	10	mA
Pin Current: at VOH	Source	3	mA
Pin Current: at VOL	Sink	8.5	mA
Port Current: GPIO	Source	20	mA
Port Current: GPIO	Sink	50	mA
Maximum Junction Temperature		155	°C

**Note:** Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

# PIC12F609/615/617/12HV609/615

**TABLE 16-18: OSCILLATOR PARAMETERS FOR PIC12F615-H (High Temp.)**

Param No.	Sym	Characteristic	Frequency Tolerance	Units	Min	Typ	Max	Conditions
OS08	INTOSC	Int. Calibrated INTOSC Freq. <sup>(1)</sup>	±10%	MHz	7.2	8.0	8.8	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ 150°C

**Note 1:** To ensure these oscillator frequency tolerances, Vdd and Vss must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

**TABLE 16-19: COMPARATOR SPECIFICATIONS FOR PIC12F615-H (High Temp.)**

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
CM01	Vos	Input Offset Voltage	mV	—	±5	±20	(VDD - 1.5)/2