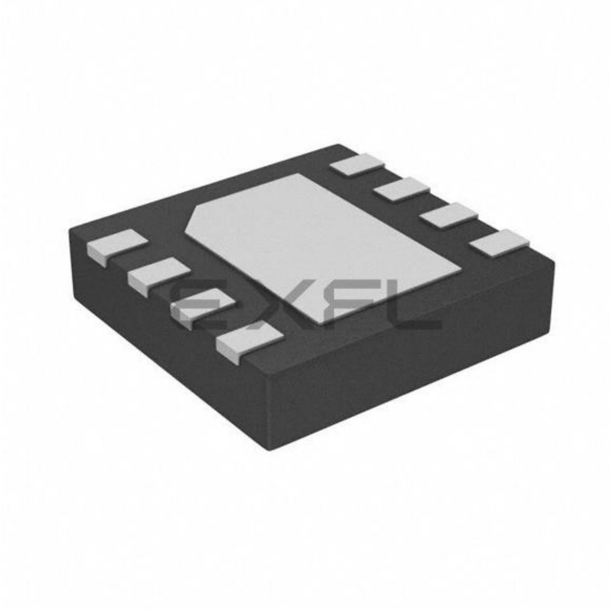

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f615t-i-mf

2.2.1 GENERAL PURPOSE REGISTER FILE

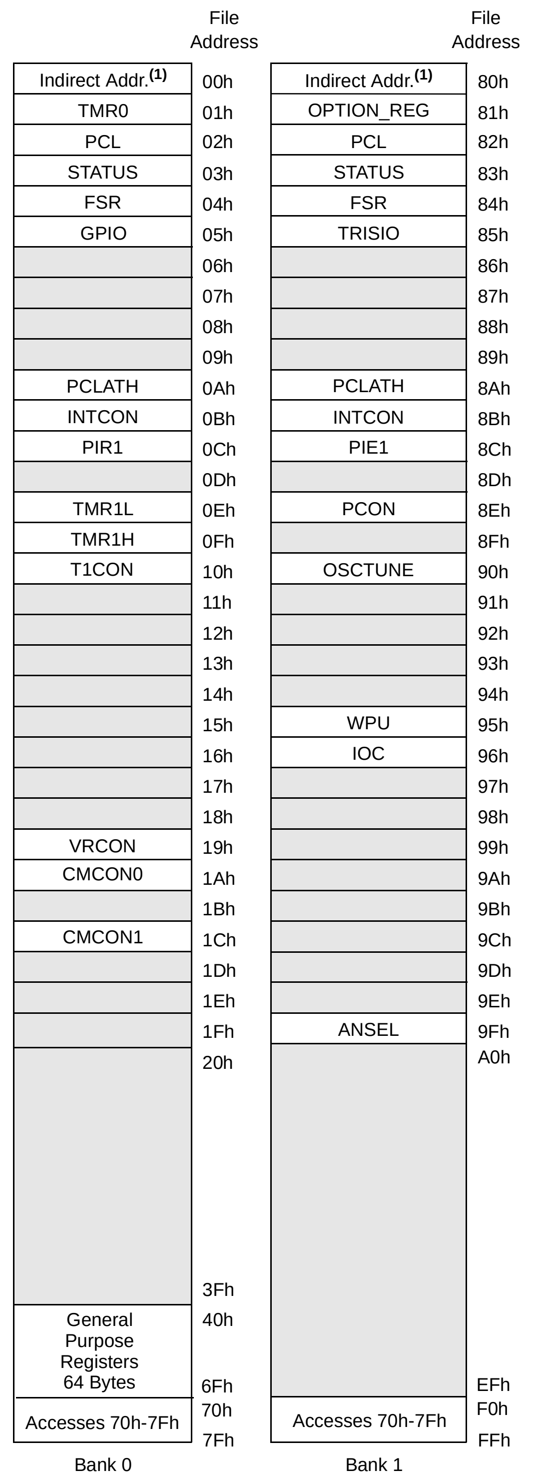
The register file is organized as 64 x 8 in the PIC12F609/615/12HV609/615, and as 128 x 8 in the PIC12F617. Each register is accessed, either directly or indirectly, through the File Select Register (FSR) (see **Section 2.4 “Indirect Addressing, INDF and FSR Registers”**).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-3: DATA MEMORY MAP OF THE PIC12F609/HV609



Bank 0	File Address	Bank 1	File Address
Indirect Addr.(1)	00h	Indirect Addr.(1)	80h
TMR0	01h	OPTION_REG	81h
PCL	02h	PCL	82h
STATUS	03h	STATUS	83h
FSR	04h	FSR	84h
GPIO	05h	TRISIO	85h
▨	06h	▨	86h
▨	07h	▨	87h
▨	08h	▨	88h
▨	09h	▨	89h
PCLATH	0Ah	PCLATH	8Ah
INTCON	0Bh	INTCON	8Bh
PIR1	0Ch	PIE1	8Ch
▨	0Dh	▨	8Dh
TMR1L	0Eh	PCON	8Eh
TMR1H	0Fh	▨	8Fh
T1CON	10h	OSCTUNE	90h
▨	11h	▨	91h
▨	12h	▨	92h
▨	13h	▨	93h
▨	14h	▨	94h
▨	15h	WPU	95h
▨	16h	IOC	96h
▨	17h	▨	97h
▨	18h	▨	98h
VRCON	19h	▨	99h
CMCON0	1Ah	▨	9Ah
▨	1Bh	▨	9Bh
CMCON1	1Ch	▨	9Ch
▨	1Dh	▨	9Dh
▨	1Eh	▨	9Eh
▨	1Fh	ANSEL	9Fh
▨	20h 3Fh	▨	A0h EFh
General Purpose Registers 64 Bytes	40h 6Fh		
Accesses 70h-7Fh	70h 7Fh	Accesses 70h-7Fh	F0h FFh
Bank 0		Bank 1	

▨ Unimplemented data memory locations, read as ‘0’.

Note 1: Not a physical register.

4.2 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two selectable clock frequencies: 4 MHz and 8 MHz

The system clock can be selected between external or internal clock sources via the FOSC<2:0> bits of the Configuration Word register.

4.3 External Clock Modes

4.3.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 4-1.

TABLE 4-1: OSCILLATOR DELAY EXAMPLES

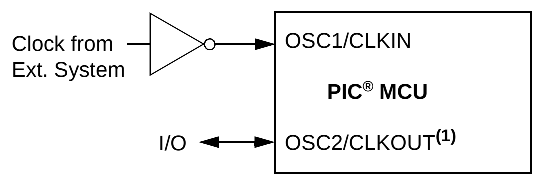
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	INTOSC	125 kHz to 8 MHz	Oscillator Warm-Up Delay (T_{WARM})
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)

4.3.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 4-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 4-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Alternate pin functions are listed in the **Section 1.0 "Device Overview"**.

4.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 4-1).

The default value of the OSCTUNE register is ‘`0`’. The value is a 5-bit two’s complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5	**Unimplemented:** Read as ‘`0`’
bit 4-0	**TUN<4:0>:** Frequency Tuning bits `01111` = Maximum frequency `01110` = • • • `00001` = `00000` = Oscillator module is running at the calibrated frequency. `11111` = • • • `10000` = Minimum frequency

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets[(1)]
CONFIG[(2)]	IOSCFS	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	`---0 0000`	`---u uuuu`

Legend: x = unknown, u = unchanged, – = unimplemented locations read as ‘`0`’. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include $\overline{\text{MCLR}}$ Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.

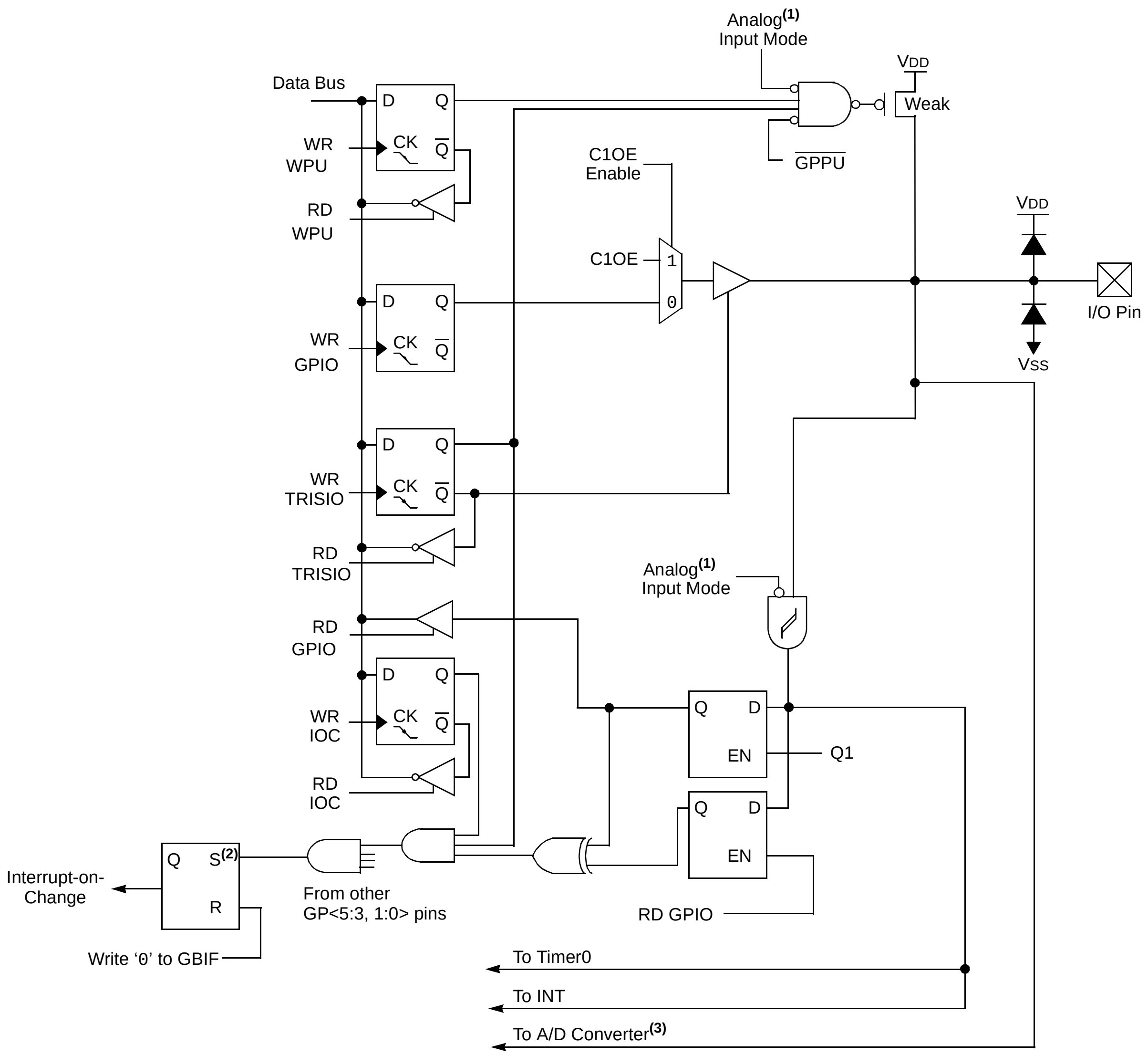
5.2.4.3 GP2/AN2(1)/T0CKI/INT/COUT/CCP1(1)/P1A(1)

Figure 5-2 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(1)
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from Comparator
- a Capture input/Compare input/PWM output(1)
- a PWM output(1)

Note 1: PIC12F615/617/HV615 only.

FIGURE 5-2: BLOCK DIAGRAM OF GP2



Note 1: Comparator mode and ANSEL determines Analog Input mode.

2: Set has priority over Reset.

3: PIC12F615/617/HV615 only.

REGISTER 10-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = `0` (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0	**ADRES<9:2>**: ADC Result Register bits Upper 8 bits of 10-bit conversion result

REGISTER 10-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = `0` (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6	**ADRES<1:0>**: ADC Result Register bits Lower 2 bits of 10-bit conversion result
bit 5-0	**Unimplemented:** Read as ‘`0`’

REGISTER 10-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-2	**Unimplemented:** Read as ‘`0`’
bit 1-0	**ADRES<9:8>**: ADC Result Register bits Upper 2 bits of 10-bit conversion result

REGISTER 10-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0	**ADRES<7:0>**: ADC Result Register bits Lower 8 bits of 10-bit conversion result

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	`0-00 0000`	`0-00 0000`
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								`xxxx xxxx`	`uuuu uuuu`
CCPR1H	Capture/Compare/PWM Register 1 High Byte								`xxxx xxxx`	`uuuu uuuu`
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	`0000 0000`	`0000 0000`
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	`-00- 0-00`	`-00- 0-00`
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	`-00- 0-00`	`-00- 0-00`
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	`0000 0000`	`uuuu uuuu`
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								`xxxx xxxx`	`uuuu uuuu`
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								`xxxx xxxx`	`uuuu uuuu`
TMR2	Timer2 Module Register								`0000 0000`	`0000 0000`
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	`--11 1111`	`--11 1111`

Legend: - = Unimplemented locations, read as '`0`', u = unchanged, x = unknown. Shaded cells are not used by the Compare.

Note 1: For PIC12F615/617/HV615 only.

REGISTER 11-2: ECCPAS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7	**ECCPASE:** ECCP Auto-Shutdown Event Status bit 1 = A shutdown event has occurred; ECCP outputs are in shutdown state 0 = ECCP outputs are operating
bit 6-4	**ECCPAS<2:0>:** ECCP Auto-shutdown Source Select bits 000 =Auto-Shutdown is disabled 001 =Comparator output change 010 =Auto-Shutdown is disabled 011 =Comparator output change(1) 100 =VIL on INT pin 101 =VIL on INT pin or Comparator change 110 =VIL on INT pin(1) 111 =VIL on INT pin or Comparator change
bit 3-2	**PSSAC<1:0>:** Pin P1A Shutdown State Control bits 00 = Drive pin P1A to ‘0’ 01 = Drive pin P1A to ‘1’ 1x = Pin P1A tri-state
bit 1-0	**PSSBD<1:0>:** Pin P1B Shutdown State Control bits 00 = Drive pin P1B to ‘0’ 01 = Drive pin P1B to ‘1’ 1x = Pin P1B tri-state

Note 1: If CMSYNC is enabled, the shutdown will be delayed by Timer1.

Note 1: The auto-shutdown condition is a level-based signal, not an edge-based signal. As long as the level is present, the auto-shutdown will persist.

2: Writing to the ECCPASE bit is disabled while an auto-shutdown condition persists.

3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.

12.0 SPECIAL FEATURES OF THE CPU

The PIC12F609/615/617/12HV609/615 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving features and offer code protection.

These features are:

- Reset
  - Power-on Reset (POR)
  - Power-up Timer (PWRT)
  - Oscillator Start-up Timer (OST)
  - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator selection
- Sleep
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC12F609/615/617/12HV609/615 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions-on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

12.1 Configuration Bits

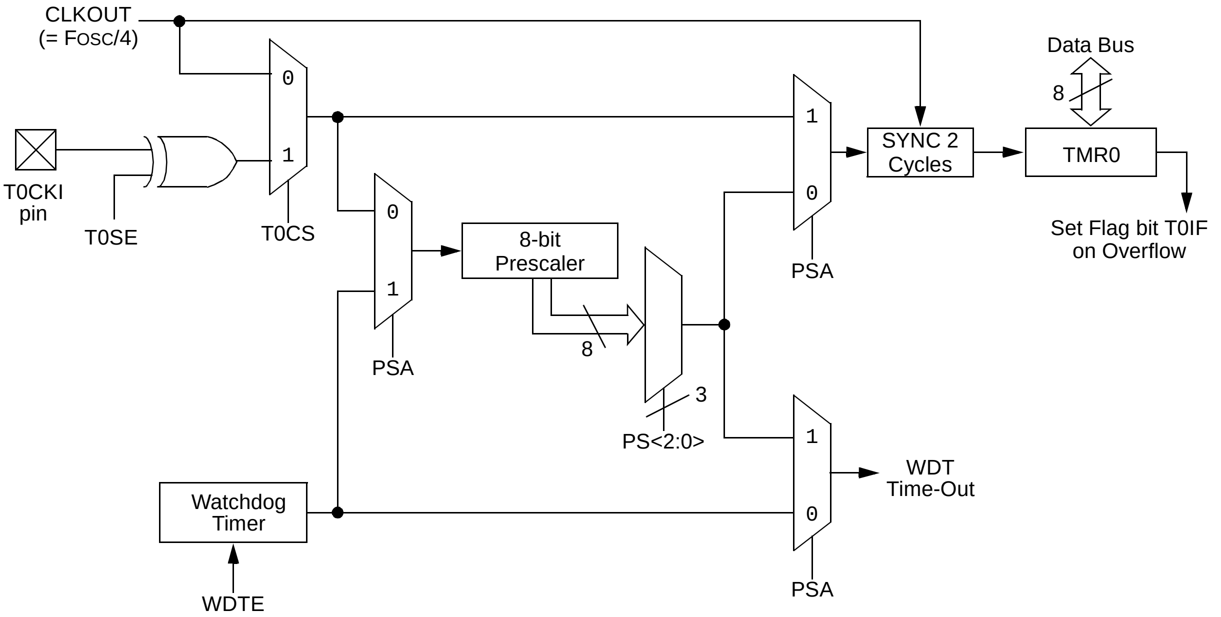
The Configuration bits can be programmed (read as '`0`'), or left unprogrammed (read as '`1`') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

Note:	Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See *Memory Programming Specification* (DS41204) for more information.

12.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst-case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time out occurs.

FIGURE 12-2: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

TABLE 12-8: WDT STATUS

Conditions	WDT
WDTE = `0`	Cleared
`CLRWDT` Command	
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

TABLE 12-9: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	`1111 1111`	`1111 1111`
CONFIG	IOSCFS	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 12-1 for operation of all Configuration Word register bits.

15.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB C Compiler for Various Device Families
  - HI-TECH C for Various Device Families
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
  - MPLAB ICD 3
  - PICkit™ 3 Debug Express
- Device Programmers
  - PICkit™ 2 Programmer
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

15.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - In-Circuit Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (C or assembly)
  - Mixed C and assembly
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

16.8 DC Characteristics: PIC12F609/615/617/12HV609/615-I (Industrial) PIC12F609/615/617/12HV609/615-E (Extended)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O port:					
D030		with TTL buffer	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
D030A			Vss	—	0.15 VDD	V	2.0V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer	Vss	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
D032		$\overline{\text{MCLR}}$, OSC1 (RC mode)	VSS	—	0.2 VDD	V	**(NOTE 1)**
D033		OSC1 (XT and LP modes)	VSS	—	0.3	V	
D033A		OSC1 (HS mode)	VSS	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25 VDD + 0.8	—	VDD	V	2.0V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	2.0V ≤ VDD ≤ 5.5V
D042		$\overline{\text{MCLR}}$	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP modes)	1.6	—	VDD	V	
D043A		OSC1 (HS mode)	0.7 VDD	—	VDD	V	
D043B		OSC1 (RC mode)	0.9 VDD	—	VDD	V	**(NOTE 1)**
	IIL	**Input Leakage Current(2,3)**					
D060		I/O ports	—	± 0.1	± 1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D061		GP3/$\overline{\text{MCLR}}$(3,4)	—	± 0.7	± 5	μA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	± 0.1	± 5	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070*	IPUR	**GPIO Weak Pull-up Current(5)**	50	250	400	μA	VDD = 5.0V, VPIN = VSS
	VOL	**Output Low Voltage**	—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
	VOH	**Output High Voltage**	VDD – 0.7	—	—	V	IOH = -2.5mA, VDD = 4.5V, -40°C to +125°C
D090		I/O ports(2)	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: This specification applies to GP3/$\overline{\text{MCLR}}$ configured as GP3 with the internal weak pull-up disabled.

5: This specification applies to all weak pull-up pins, including the weak pull-up found on GP3/$\overline{\text{MCLR}}$. When GP3/$\overline{\text{MCLR}}$ is configured as $\overline{\text{MCLR}}$ reset pin, the weak pull-up is always enabled.

6: Applies to PIC12F617 only.

TABLE 16-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)
Operating Temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Freq. Tolerance	Min	Typ†	Max	Units	Conditions
OS06	TWARM	Internal Oscillator Switch when running[3]	—	—	—	2	TOSC	Slowest clock
OS07	INTOSC	Internal Calibrated INTOSC Frequency[2] (4MHz)	±1%	3.96	4.0	4.04	MHz	VDD = 3.5V, T_A = 25°C
			±2%	3.92	4.0	4.08	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	3.80	4.0	4.2	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS08	INTOSC	Internal Calibrated INTOSC Frequency[2] (8MHz)	±1%	7.92	8.0	8.08	MHz	VDD = 3.5V, T_A = 25°C
			±2%	7.84	8.0	8.16	MHz	2.5V ≤ VDD ≤ 5.5V, 0°C ≤ TA ≤ +85°C
			±5%	7.60	8.0	8.40	MHz	2.0V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +85°C (Ind.), -40°C ≤ TA ≤ +125°C (Ext.)
OS10*	TIOSC ST	INTOSC Oscillator Wake-up from Sleep Start-up Time	—	5.5	12	24	μs	VDD = 2.0V, -40°C to +85°C
			—	3.5	7	14	μs	VDD = 3.0V, -40°C to +85°C
			—	3	6	11	μs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

3: By design.

TABLE 16-11: PIC12F615/617/HV615 A/D CONVERTER (ADC) CHARACTERISTICS:

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	±1	LSb	VREF = 5.12V(5)
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes to 10 bits VREF = 5.12V(5)
AD04	EOFF	Offset Error	—	+1.5	+2.0	LSb	VREF = 5.12V(5)
AD07	EGN	Gain Error	—	—	±1	LSb	VREF = 5.12V(5)
AD06 AD06A	VREF	Reference Voltage(3)	2.2 2.5	—	— VDD	V	Absolute minimum to ensure 1 LSb accuracy
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	IREF	VREF Input Current(3)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

5: VREF = 5V for PIC12HV615.

TABLE 16-12: PIC12F615/617/HV615 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ TA ≤ +125°C

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
AD130*	TAD	A/D Clock Period	1.6	—	9.0	μs	TOSC-based, VREF ≥ 3.0V
			3.0	—	9.0	μs	TOSC-based, VREF full range(3)
		A/D Internal RC Oscillator Period	3.0	6.0	9.0	μs	ADCS<1:0> = 11 (ADRC mode) At VDD = 2.5V
			1.6	4.0	6.0	μs	At VDD = 5.0V
AD131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO/$\overline{\text{DONE}}$ bit to new data in A/D Result register
AD132*	TACQ	Acquisition Time		11.5	—	μs	
AD133*	TAMP	Amplifier Settling Time	—	—	5	μs	
AD134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	
			—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

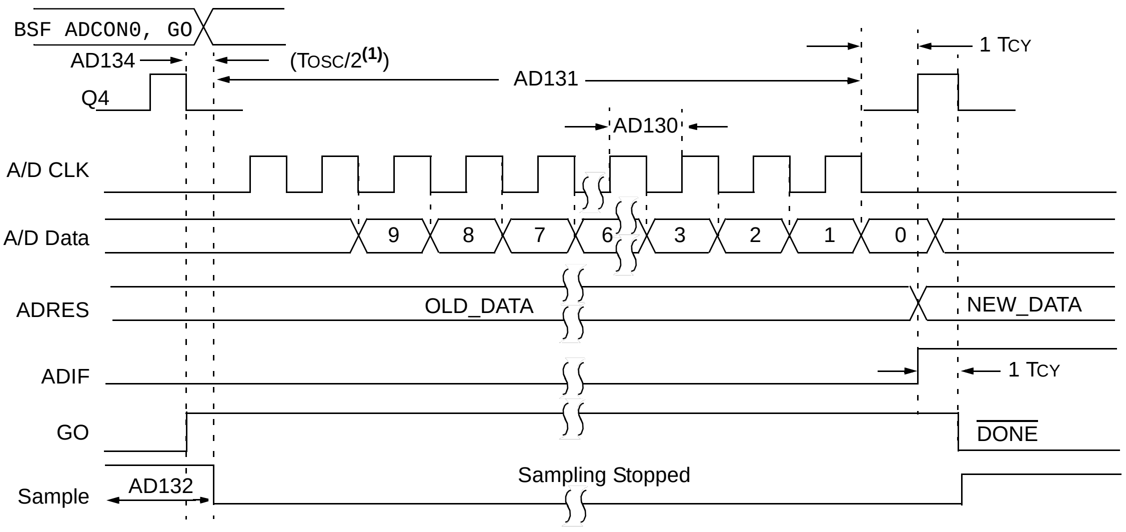
† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See **Section 10.3 “A/D Acquisition Requirements”** for minimum conditions.

3: Full range for PIC12HV609/HV615 powered by the shunt regulator is the 5V regulated voltage.

FIGURE 16-10: PIC12F615/617/HV615 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 16-14: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						VDD	Note
D010	Supply Current (IDD)	μA	—	13	58	2.0	IDD LP OSC (32 kHz)
			—	19	67	3.0	
			—	32	92	5.0	
D011		μA	—	135	316	2.0	IDD XT OSC (1 MHz)
			—	185	400	3.0	
			—	300	537	5.0	
D012		μA	—	240	495	2.0	IDD XT OSC (4 MHz)
			—	360	680	3.0	
		mA	—	0.660	1.20	5.0	
D013		μA	—	75	158	2.0	IDD EC OSC (1 MHz)
			—	155	338	3.0	
			—	345	792	5.0	
D014		μA	—	185	357	2.0	IDD EC OSC (4 MHz)
			—	325	625	3.0	
		mA	—	0.665	1.30	5.0	
D016		μA	—	245	476	2.0	IDD INTOSC (4 MHz)
			—	360	672	3.0	
			—	620	1.10	5.0	
D017		μA	—	395	757	2.0	IDD INTOSC (8 MHz)
		mA	—	0.620	1.20	3.0	
			—	1.20	2.20	5.0	
D018		μA	—	175	332	2.0	IDD EXTRC (4 MHz)
			—	285	518	3.0	
			—	530	972	5.0	
D019		mA	—	2.20	4.10	4.5	IDD HS OSC (20 MHz)
			—	2.80	4.80	5.0	

TABLE 16-15: DC CHARACTERISTICS FOR IPD SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						VDD	Note
D020E	Power Down Base Current	μA	—	0.05	12	2.0	IPD Base
			—	0.15	13	3.0	
			—	0.35	14	5.0	
D021E		μA	—	0.5	20	2.0	WDT Current
			—	2.5	25	3.0	
			—	9.5	36	5.0	
D022E		μA	—	5.0	28	3.0	BOR Current
			—	6.0	36	5.0	
D023E		μA	—	105	195	2.0	IPD Current (Both Comparators Enabled)
			—	110	210	3.0	
			—	116	220	5.0	
		μA	—	50	105	2.0	IPD Current (One Comparator Enabled)
			—	55	110	3.0	
			—	60	125	5.0	
D024E		μA	—	30	58	2.0	IPD (CVREF, High Range)
			—	45	85	3.0	
			—	75	142	5.0	
D025E		μA	—	39	76	2.0	IPD (CVREF, Low Range)
			—	59	114	3.0	
			—	98	190	5.0	
D026E		μA	—	5.5	30	2.0	IPD (T1 OSC, 32 kHz)
			—	7.0	35	3.0	
			—	8.5	45	5.0	
D027E		μA	—	0.2	12	3.0	IPD (A2D on, not converting)
			—	0.3	15	5.0	

TABLE 16-16: WATCHDOG TIMER SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	ms	6	20	70	150°C Temperature

TABLE 16-17: LEAKAGE CURRENT SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
D061	IIL	Input Leakage Current(1) (GP3/RA3/$\overline{\text{MCLR}}$)	μA	—	±0.5	±5.0	VSS ≤ VPIN ≤ VDD
D062	IIL	Input Leakage Current(2) (GP3/RA3/$\overline{\text{MCLR}}$)	μA	50	250	400	VDD = 5.0V

Note 1: This specification applies when GP3/RA3/$\overline{\text{MCLR}}$ is configured as an input with the pull-up disabled. The leakage current for the GP3/RA3/$\overline{\text{MCLR}}$ pin is higher than for the standard I/O port pins.

2: This specification applies when GP3/RA3/$\overline{\text{MCLR}}$ is configured as the $\overline{\text{MCLR}}$ reset pin function with the weak pull-up enabled.

FIGURE 17-3: PIC12F609/615/617 IDD EC (4 MHz) vs. VDD

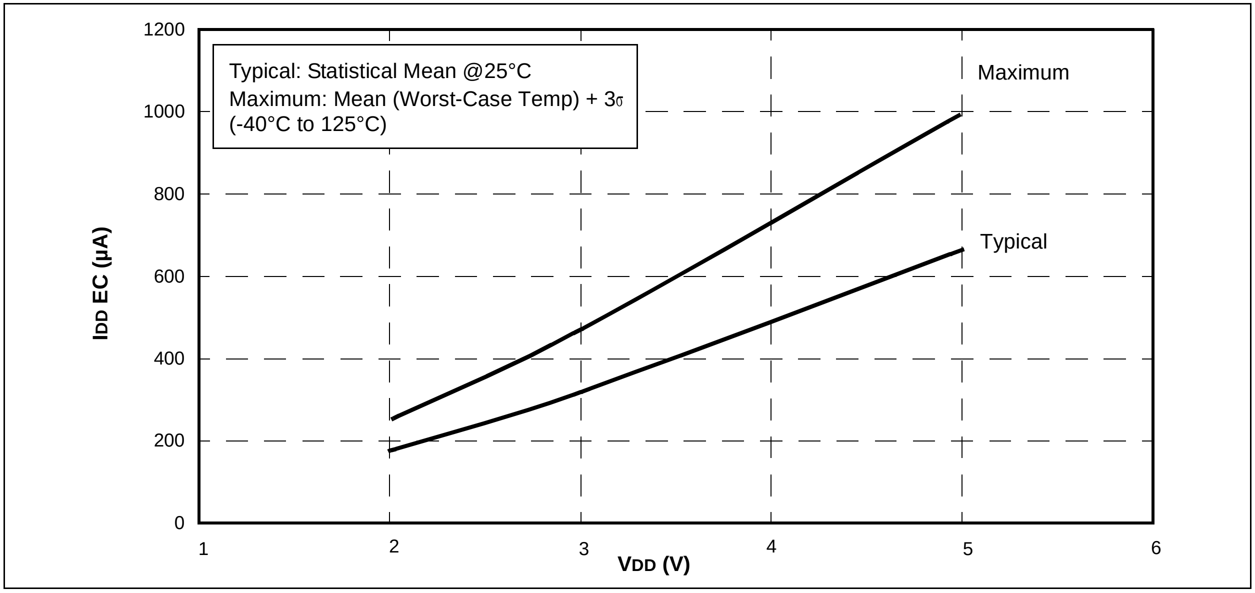


FIGURE 17-4: PIC12F609/615/617 IDD XT (1 MHz) vs. VDD

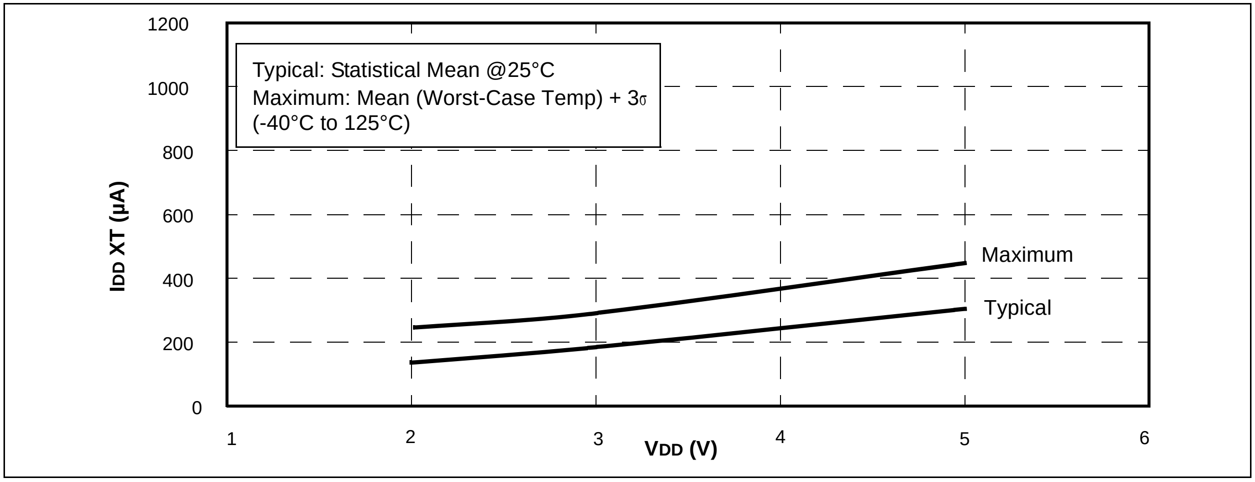


FIGURE 17-5: PIC12F609/615/617 IDD XT (4 MHz) vs. VDD

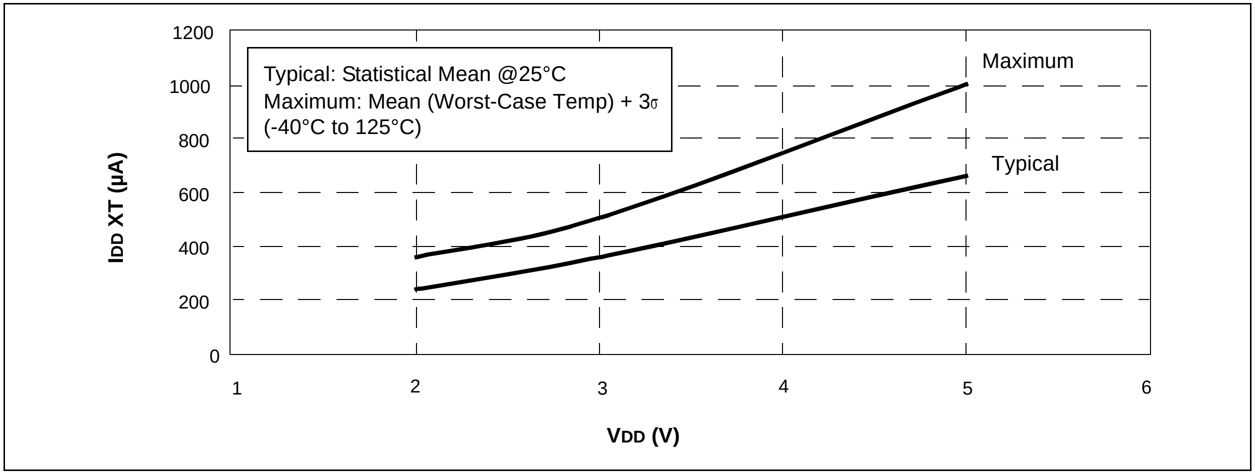


FIGURE 17-35: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

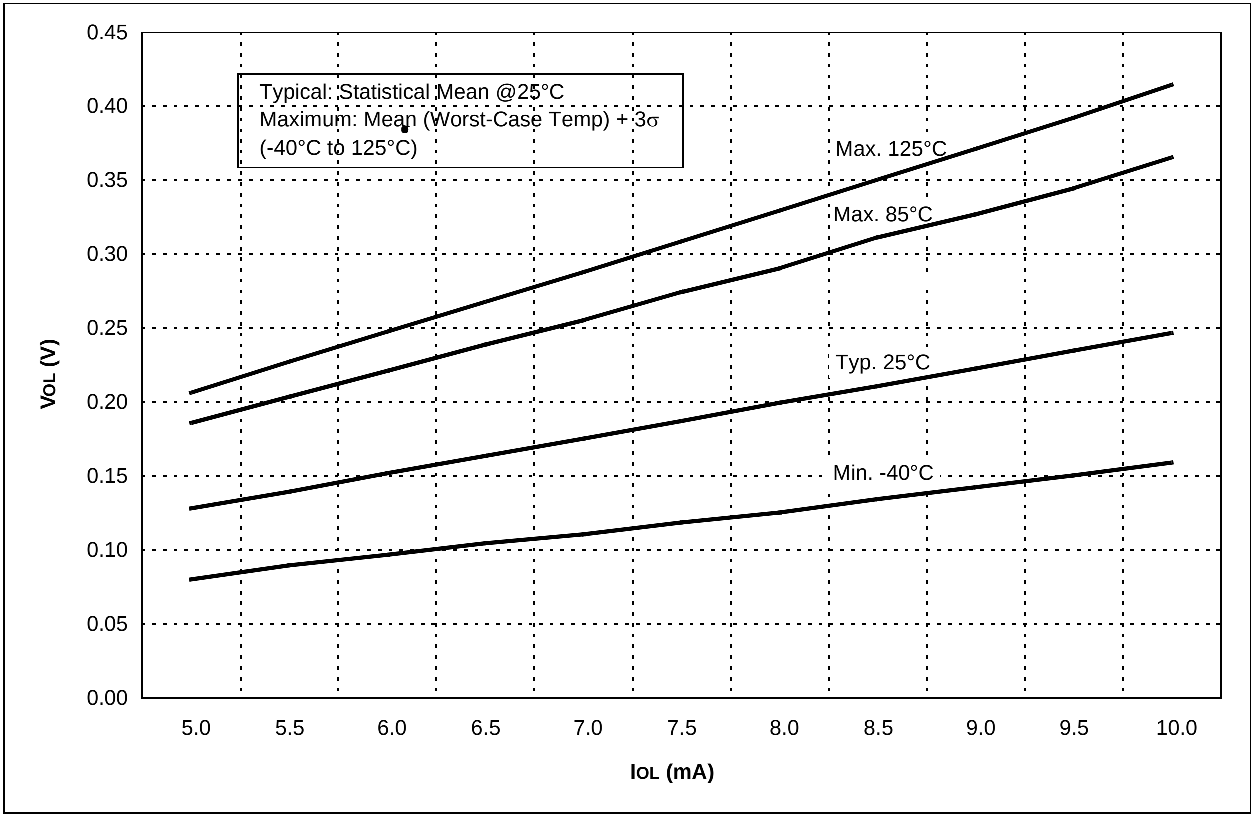


FIGURE 17-36: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

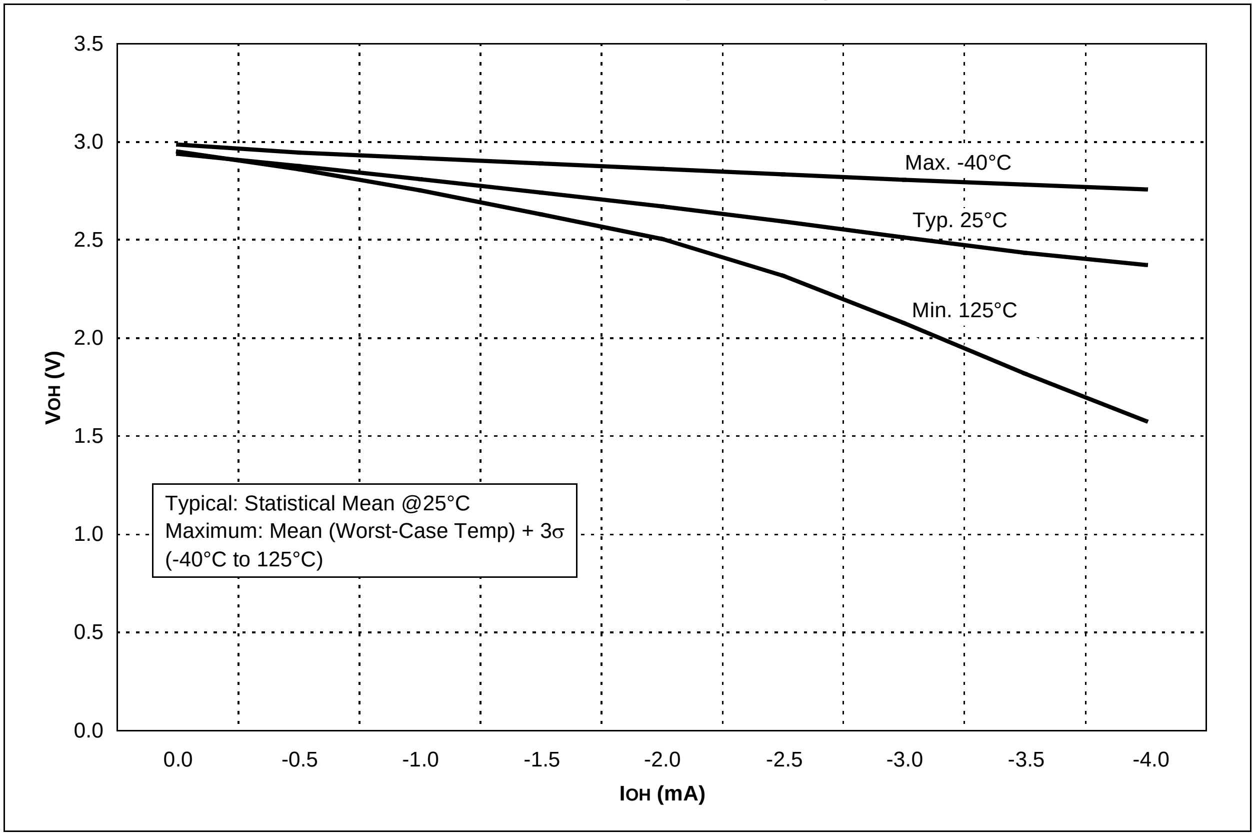


FIGURE 17-45: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (125°C)

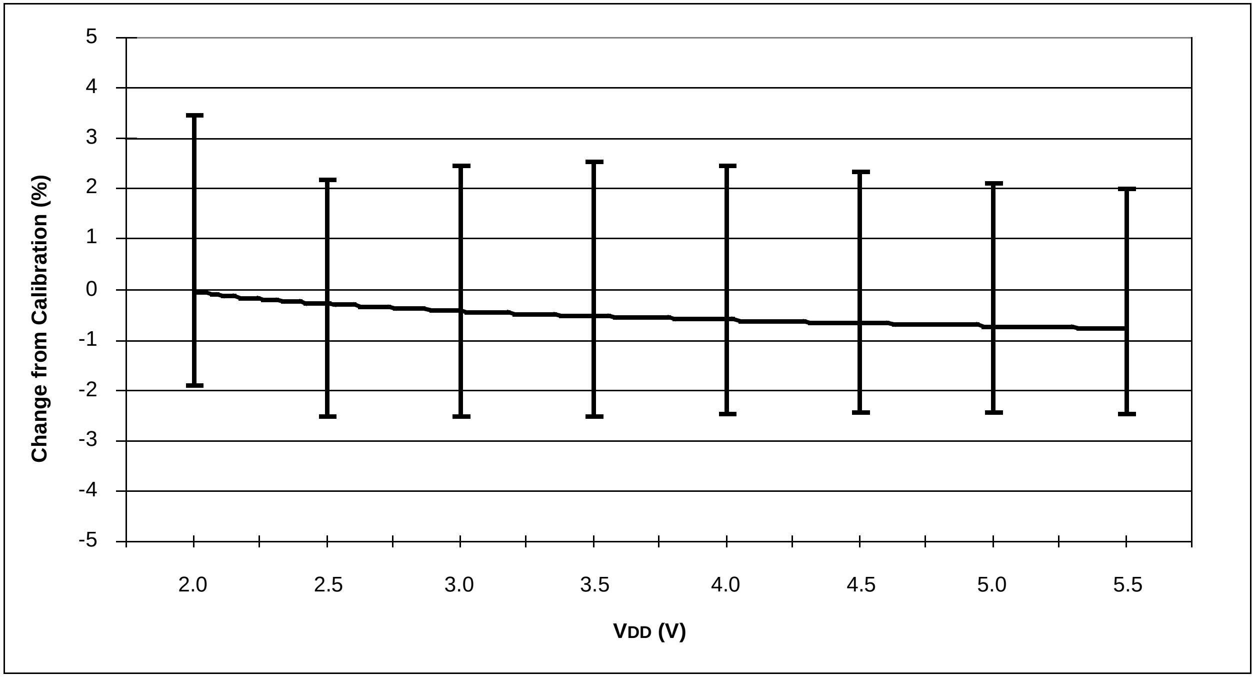
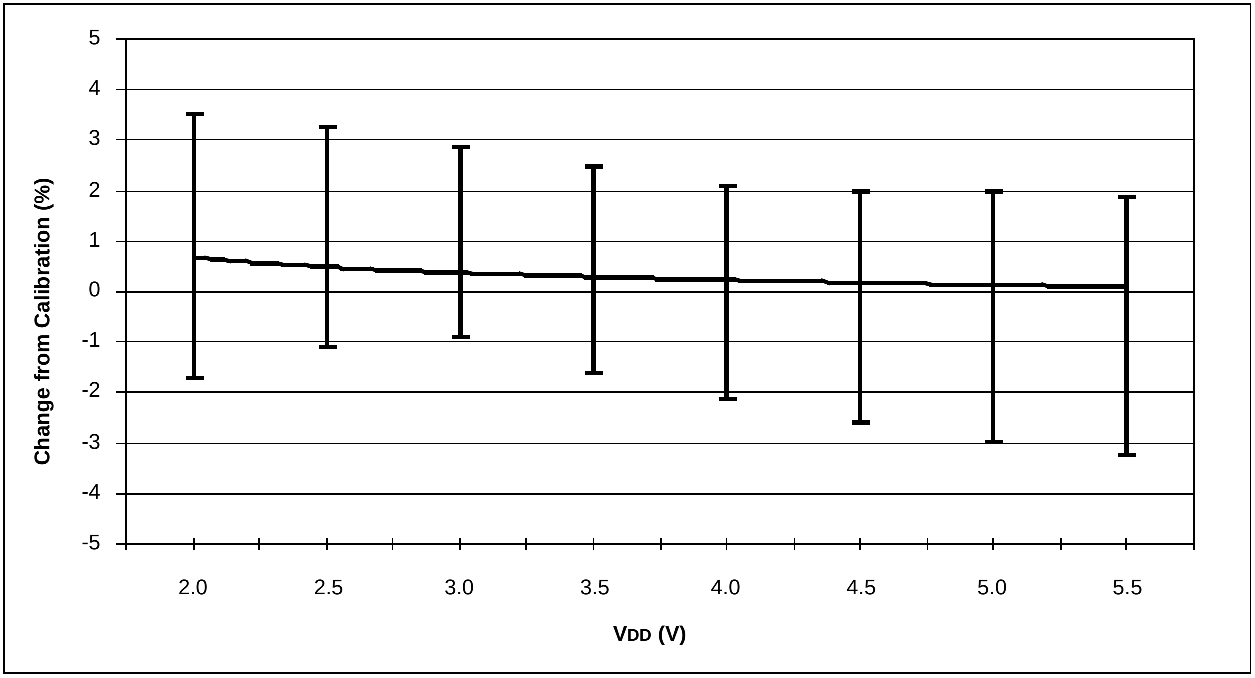


FIGURE 17-46: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)



NOTES: