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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f615t-i-ms

TABLE 1-1: PIC12F609/HV609 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/CIN+/ICSPDAT	GP0	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	CIN+	AN	—	Comparator non-inverting input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
GP1/CIN0-/ICSPCLK	GP1	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	CIN0-	AN	—	Comparator inverting input
	ICSPCLK	ST	—	Serial Programming Clock
GP2/T0CKI/INT/COUT	GP2	ST	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	COUT	—	CMOS	Comparator output
GP3/$\overline{MCLR}$/V_{PP}	GP3	TTL	—	General purpose input with interrupt-on-change
	$\overline{MCLR}$	ST	—	Master Clear w/internal pull-up
	V_{PP}	HV	—	Programming voltage
GP4/CIN1-/$\overline{T1G}$/OSC2/ CLKOUT	GP4	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	CIN1-	AN	—	Comparator inverting input
	$\overline{T1G}$	ST	—	Timer1 gate (count enable)
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	F_{OSC}/4 output
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
V_{DD}	V_{DD}	Power	—	Positive supply
V_{SS}	V_{SS}	Power	—	Ground reference

Legend: AN=Analog input or output CMOS = CMOS compatible input or output HV= High Voltage
ST=Schmitt Trigger input with CMOS levels TTL = TTL compatible input XTAL=Crystal

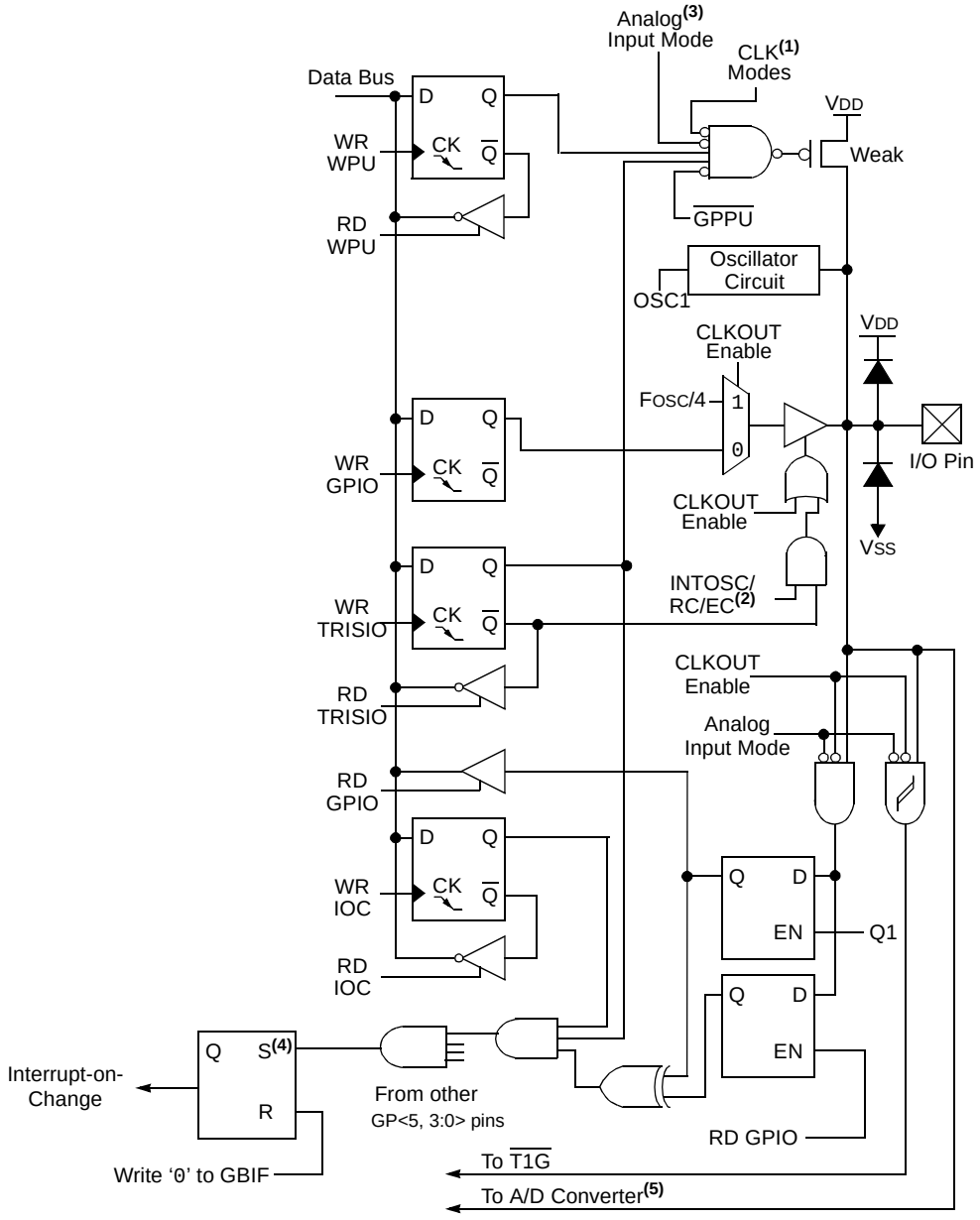
5.2.4.5 GP4/AN3(2)/CIN1-/$\overline{T1G}$/P1B(1, 2)/OSC2/CLKOUT

Figure 5-4 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC(2)
- Comparator inverting input
- a Timer1 gate (count enable)
- PWM output, alternate pin(1, 2)
- a crystal/resonator connection
- a clock output

Note 1: Alternate pin function.
2: PIC12F615/617/HV615 only.

FIGURE 5-4: BLOCK DIAGRAM OF GP4



Note 1: CLK modes are XT, HS, LP, TMR1 LP and CLKOUT Enable.
2: With CLKOUT option.
3: Analog Input mode comes from ANSEL.
4: Set has priority over Reset.
5: PIC12F615/617/HV615 only.

7.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

7.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after one or more of the following conditions:

- Timer1 is enabled after POR or BOR Reset
- A write to TMR1H or TMR1L
- T1CKI is high when Timer1 is disabled and when Timer1 is re-enabled T1CKI is low. See Figure 7-2.

7.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

7.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO5 and TRISIO4 bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as '0' and TRISIO5 and TRISIO4 bits read as '1'.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

7.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment.

Note:	In asynchronous counter mode or when using the internal oscillator and T1ACS=1, Timer1 can not be used as a time base for the capture or compare modes of the ECCP module (for PIC12F615/617/HV615 only).

7.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TTMR1L register pair.

9.3 Comparator Control

The comparator has two control and Configuration registers: CMCON0 and CMCON1. The CMCON1 register is used for controlling the interaction with Timer1 and simultaneously reading the comparator output.

The CMCON0 register (Register 9-1) contain the control and Status bits for the following:

- Enable
- Input selection
- Reference selection
- Output selection
- Output polarity

9.3.1 COMPARATOR ENABLE

Setting the CMON bit of the CMCON0 register enables the comparator for operation. Clearing the CMON bit disables the comparator for minimum current consumption.

9.3.2 COMPARATOR INPUT SELECTION

The CMCH bit of the CMCON0 register directs one of four analog input pins to the comparator inverting input.

Note:	To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

9.3.3 COMPARATOR REFERENCE SELECTION

Setting the CMR bit of the CMxCON0 register directs an internal voltage reference or an analog input pin to the non-inverting input of the comparator. See **Section 9.10 "Comparator Voltage Reference"** for more information on the internal voltage reference module.

9.3.4 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the COUT bit of the CMCON0 register. In order to make the output available for an external connection, the following conditions must be true:

- CMOE bit of the CMxCON0 register must be set
- Corresponding TRIS bit must be cleared
- CMON bit of the CMCON0 register must be set.

Note 1:	The CMOE bit overrides the PORT data latch. Setting the CMON has no impact on the port override.
2:	The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

9.3.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CMPOL bit of the CMCON0 register. Clearing CMPOL results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 9-1.

TABLE 9-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CMPOL	COUT
$CMV_{IN}- > CMV_{IN}+$	0	0
$CMV_{IN}- < CMV_{IN}+$	0	1
$CMV_{IN}- > CMV_{IN}+$	1	1
$CMV_{IN}- < CMV_{IN}+$	1	0

Note: COUT refers to both the register bit and output pin.

9.4 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See **Section 16.0 "Electrical Specifications"** for more details.

REGISTER 9-3: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMVREN	—	VRR	FVREN	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CMVREN:** Comparator Voltage Reference Enable bit(1, 2)
1 = CVREF circuit powered on and routed to CVREF input of the Comparator
0 = 0.6 Volt constant reference routed to CVREF input of the Comparator

bit 6 **Unimplemented:** Read as '0'

bit 5 **VRR:** CVREF Range Selection bit
1 = Low range
0 = High range

bit 4 **FVREN:** 0.6V Reference Enable bit(2)
1 = Enabled
0 = Disabled

bit 3-0 **VR<3:0>:** Comparator Voltage Reference CVREF Value Selection bits ($0 \leq$ VR<3:0> ≤ 15)
When VRR = 1: CVREF = (VR<3:0>/24) * VDD
When VRR = 0: CVREF = VDD/4 + (VR<3:0>/32) * VDD

Note 1: When CMVREN is low, the CVREF circuit is powered down and does not contribute to IDD current.
2: When CMVREN is low and the FVREN bit is low, the CVREF signal should provide Vss to the comparator.

REGISTER 10-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES9	ADRES8	ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 10-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0 (READ-ONLY)

R-x	R-x	U-0	U-0	U-0	U-0	U-0	U-0
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Unimplemented:** Read as '0'

REGISTER 10-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1 (READ-ONLY)

U-0	U-0	U-0	U-0	U-0	U-0	R-x	R-x
—	—	—	—	—	—	ADRES9	ADRES8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

REGISTER 10-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1 (READ-ONLY)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

11.0 ENHANCED CAPTURE/ COMPARE/PWM (WITH AUTO-SHUTDOWN AND DEAD BAND) MODULE (PIC12F615/617/ HV615 ONLY)

The Enhanced Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event.The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

Table 11-1 shows the timer resources required by the ECCP module.

TABLE 11-1: ECCP MODE – TIMER RESOURCES REQUIRED

ECCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 11-1: CCP1CON: ENHANCED CCP1 CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **P1M:** PWM Output Configuration bits
If CCP1M<3:2> = 00, 01, 10:
x = P1A assigned as Capture/Compare input; P1B assigned as port pins
If CCP1M<3:2> = 11:
0 = Single output; P1A modulated; P1B assigned as port pins
1 = Half-Bridge output; P1A, P1B modulated with dead-band control

bit 6 **Unimplemented:** Read as ‘0’

bit 5-4 **DC1B<1:0>:** PWM Duty Cycle Least Significant bits
Capture mode:
Unused.
Compare mode:
Unused.
PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** ECCP Mode Select bits
0000 =Capture/Compare/PWM off (resets ECCP module)
0001 =Unused (reserved)
0010 =Compare mode, toggle output on match (CCP1IF bit is set)
0011 =Unused (reserved)
0100 =Capture mode, every falling edge
0101 =Capture mode, every rising edge
0110 =Capture mode, every 4th rising edge
0111 =Capture mode, every 16th rising edge
1000 =Compare mode, set output on match (CCP1IF bit is set)
1001 =Compare mode, clear output on match (CCP1IF bit is set)
1010 =Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
1011 =Compare mode, trigger special event (CCP1IF bit is set; CCP1 resets TMR1 or TMR2 and starts an A/D conversion, if the ADC module is enabled)
1100 =PWM mode; P1A active-high; P1B active-high
1101 =PWM mode; P1A active-high; P1B active-low
1110 =PWM mode; P1A active-low; P1B active-high
1111 =PWM mode; P1A active-low; P1B active-low

NOTES:

TABLE 12-5: INITIALIZATION CONDITION FOR REGISTERS (PIC12F615/617/HV615)

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset WDT Reset Brown-out Reset(1)	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1(3)
STATUS	03h/83h	0001 1xxx	000q quuu(4)	uuuq quuu(4)
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	05h	--x0 x000	--u0 u000	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu(2)
PIR1	0Ch	-000 0-00	-000 0-00	-uuu u-uu(2)
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2(1)	11h	0000 0000	0000 0000	uuuu uuuu
T2CON(1)	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L(1)	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H(1)	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON(1)	15h	0-00 0000	0-00 0000	u-uu uuuu
PWM1CON(1)	16h	0000 0000	0000 0000	uuuu uuuu
ECCPAS(1)	17h	0000 0000	0000 0000	uuuu uuuu
VRCON	19h	0-00 0000	0-00 0000	u-uu uuuu
CMCON0	1Ah	0000 -0-0	0000 -0-0	uuuu -u-u
CMCON1	1Ch	---0 0-10	---0 0-10	---u u-qu
ADRESH(1)	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0(1)	1Fh	00-0 0000	00-0 0000	uu-u uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISIO	85h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	-00- 0-00	-00- 0-00	-uu- u-uu
PCON	8Eh	---- --0x	---- --uu(1, 5)	---- --uu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
APFCON	93h	---0 --00	---0 --00	---u --uu
WPU	95h	--11 -111	--11 -111	--uu -uuu
IOC	96h	--00 0000	--00 0000	--uu uuuu
PMCON1(6)	98h	---- -000	---- -000	---- -uuu
PMCON2(6)	99h	---- ----	---- ----	---- ----
PMADRL(6)	9Ah	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

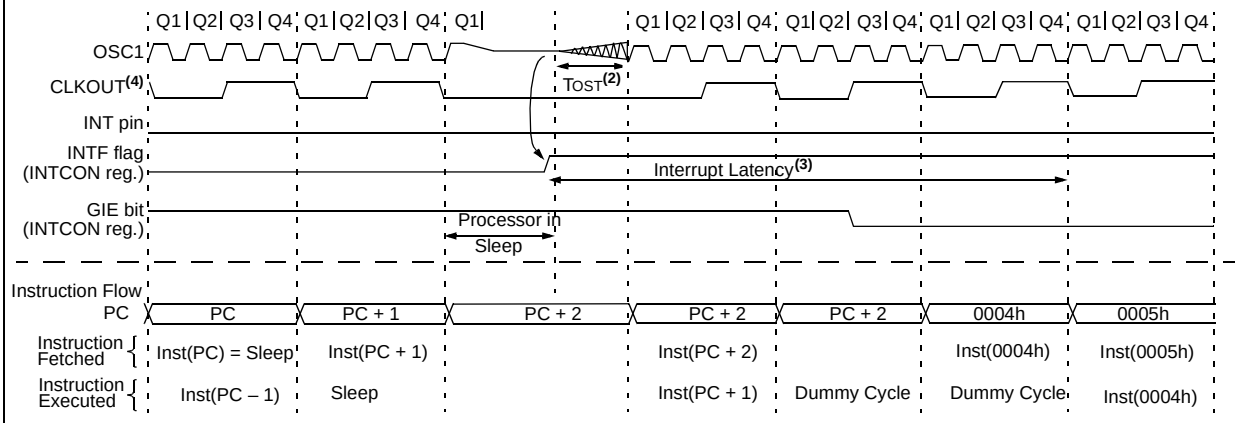
3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-6 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: For PIC12F617 only.

FIGURE 12-9: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.

2: TOST = 1024 TOSC (drawing not to scale). This delay does not apply to EC, INTOSC and RC Oscillator modes.

3: GIE = '1' assumed. In this case after wake-up, the processor jumps to 0004h. If GIE = '0', execution will continue in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

12.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note:	The entire Flash program memory will be erased when the code protection is turned off. See the *MemoryProgramming Specification* (DS41204) for more information.

12.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

15.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

15.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at V_{DDMIN} and V_{DDMAX} for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

15.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

16.4 DC Characteristics: PIC12F609/615/617 - I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	**Power-down Base Current (IPD)(2)**	—	0.05	0.9	µA	2.0	WDT, BOR, Comparator, VREF and T1OSC disabled
		—	0.15	1.2	µA	3.0	
	PIC12F609/615/617	—	0.35	1.5	µA	5.0	
			150	500	nA	3.0	-40°C ≤ TA ≤ +25°C for industrial
D021		—	0.5	1.5	µA	2.0	WDT Current(1)
		—	2.5	4.0	µA	3.0	
		—	9.5	17	µA	5.0	
D022		—	5.0	9	µA	3.0	BOR Current(1)
		—	6.0	12	µA	5.0	
D023		—	50	60	µA	2.0	Comparator Current(1), single comparator enabled
		—	55	65	µA	3.0	
		—	60	75	µA	5.0	
D024		—	30	40	µA	2.0	CVREF Current(1) (high range)
		—	45	60	µA	3.0	
		—	75	105	µA	5.0	
D025*		—	39	50	µA	2.0	CVREF Current(1) (low range)
		—	59	80	µA	3.0	
		—	98	130	µA	5.0	
D026		—	5.5	10	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	7.0	12	µA	3.0	
		—	8.5	14	µA	5.0	
D027		—	0.2	1.6	µA	3.0	A/D Current(1), no conversion in progress
		—	0.36	1.9	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

16.9 Thermal Considerations

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C					
Param No.	**Sym**	**Characteristic**	**Typ**	**Units**	**Conditions**
TH01	θJA	Thermal Resistance Junction to Ambient	84.6*	C/W	8-pin PDIP package
			149.5*	C/W	8-pin SOIC package
			211*	C/W	8-pin MSOP package
			60*	C/W	8-pin DFN 3x3mm package
			44*	C/W	8-pin DFN 4x4mm package
TH02	θJC	Thermal Resistance Junction to Case	41.2*	C/W	8-pin PDIP package
			39.9*	C/W	8-pin SOIC package
			39*	C/W	8-pin MSOP package
			9*	C/W	8-pin DFN 3x3mm package
			3.0*	C/W	8-pin DFN 4x4mm package
TH03	TDIE	Die Temperature	150*	C	
TH04	PD	Power Dissipation	—	W	PD = PINTERNAL + PI/O
TH05	PINTERNAL	Internal Power Dissipation	—	W	PINTERNAL = IDD x VDD **(NOTE 1)**
TH06	PI/O	I/O Power Dissipation	—	W	PI/O = Σ (IOL * VOL) + Σ (IOH * (VDD - VOH))
TH07	PDER	Derated Power	—	W	PDER = PDMAX (TDIE - TA)/θJA **(NOTE 2)**

* These parameters are characterized but not tested.

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient temperature.

FIGURE 17-18: PIC12HV609/615 IDD LP (32 kHz) vs. VDD

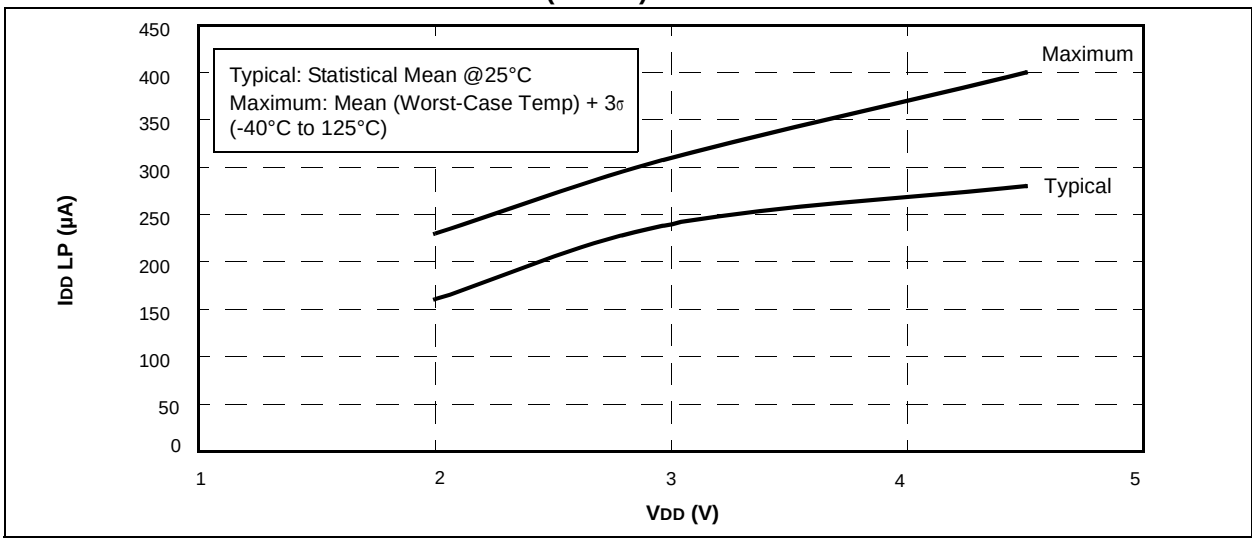


FIGURE 17-19: PIC12HV609/615 IDD EC (1 MHz) vs. VDD

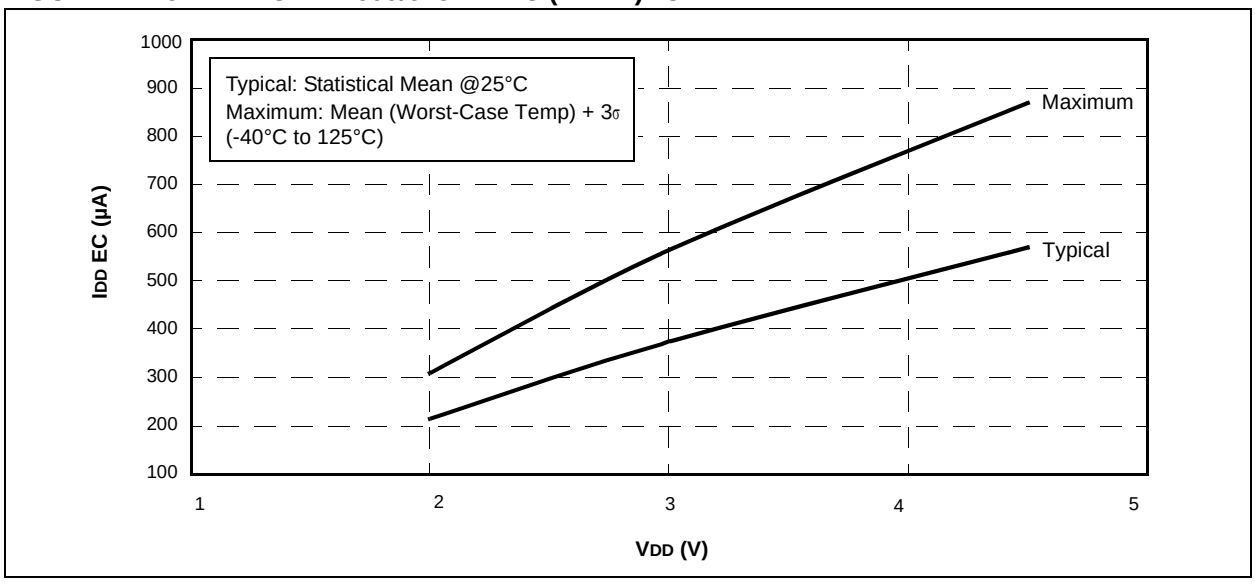


FIGURE 17-20: PIC12HV609/615 IDD EC (4 MHz) vs. VDD

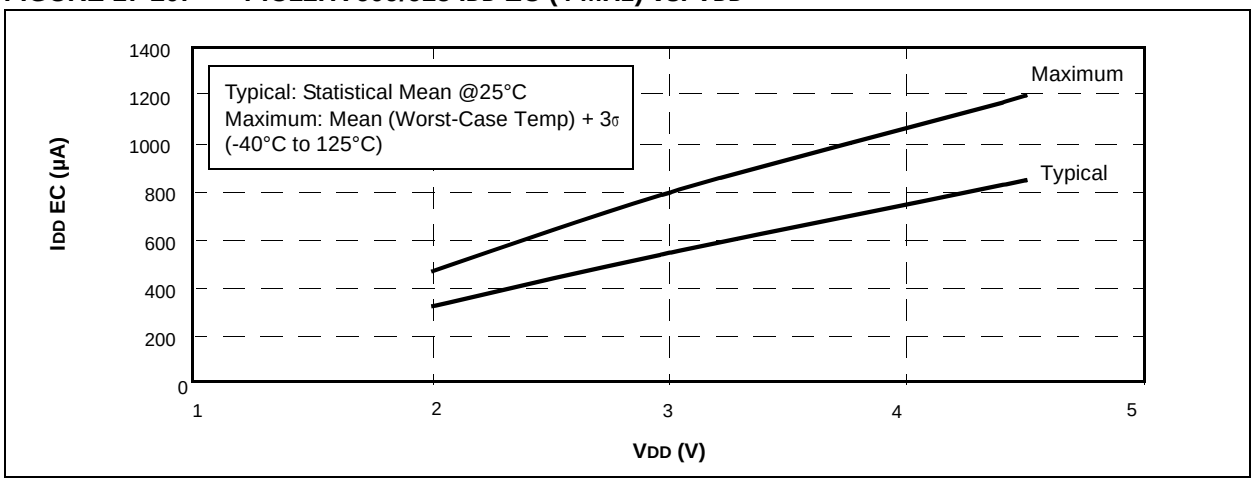


FIGURE 17-33: PIC12HV615 IPD A/D vs. VDD

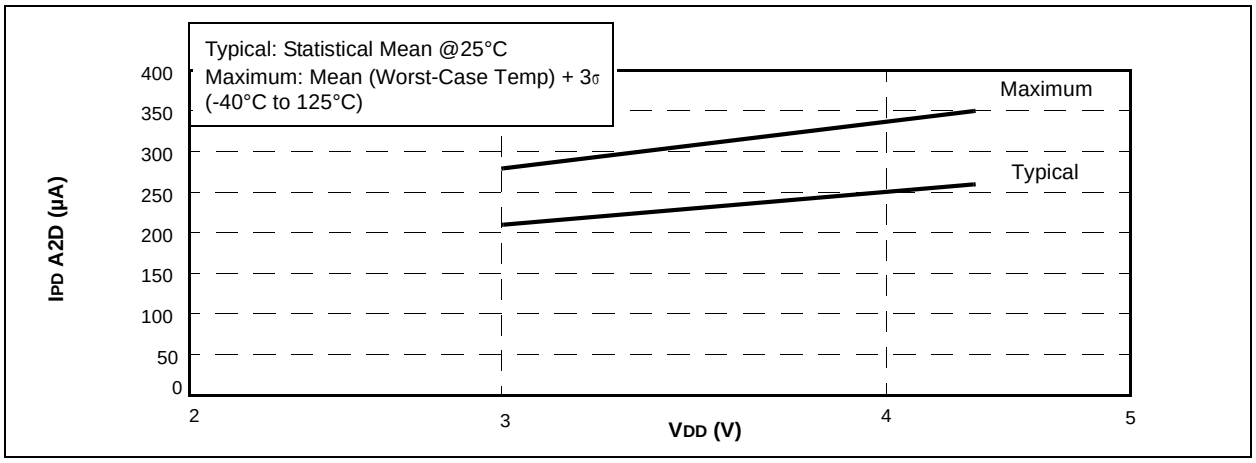


FIGURE 17-34: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)

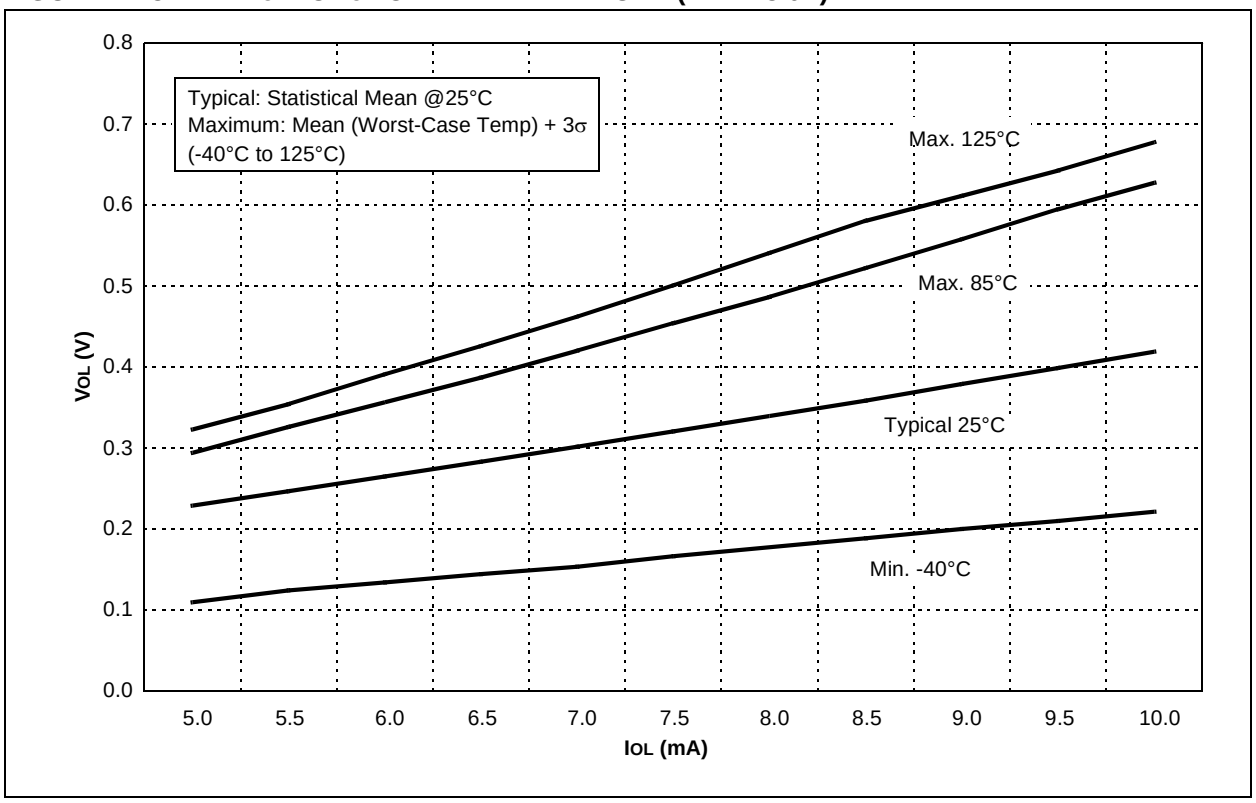


FIGURE 17-35: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)

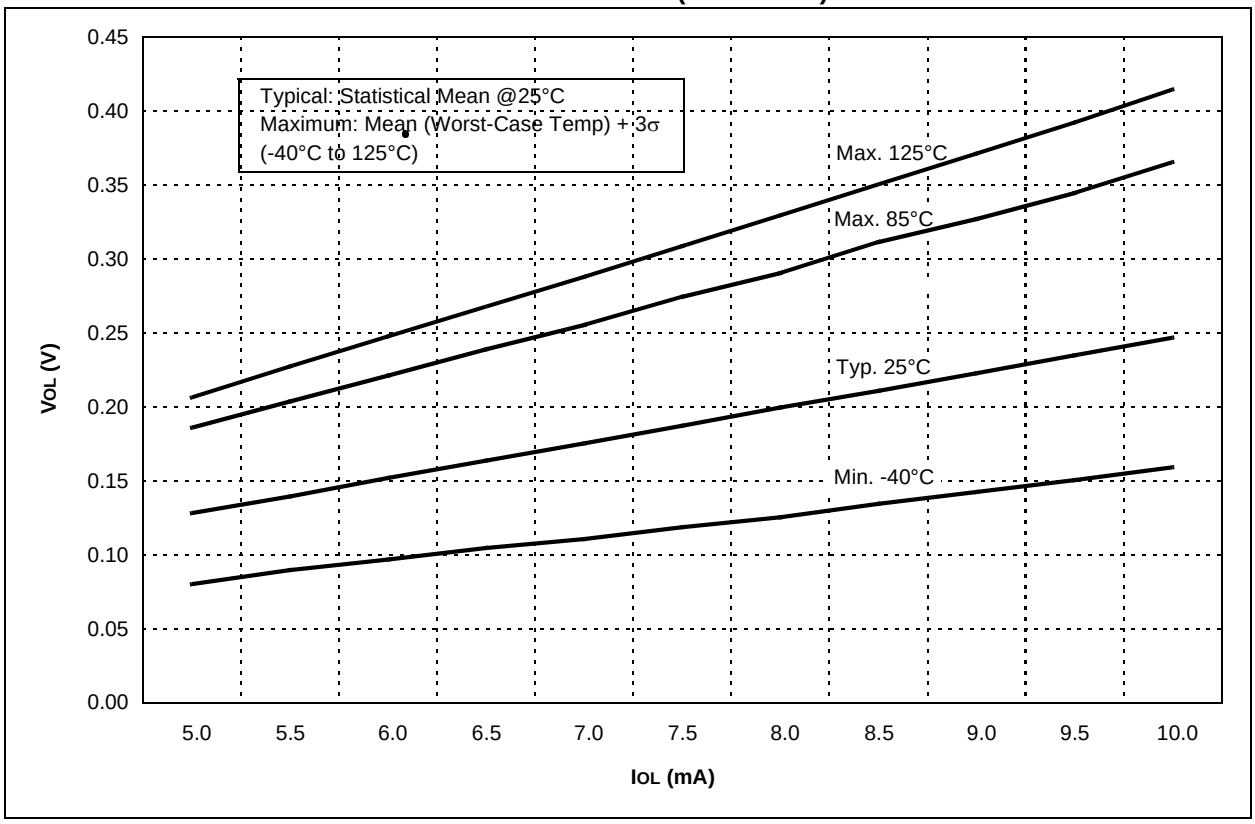


FIGURE 17-36: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)

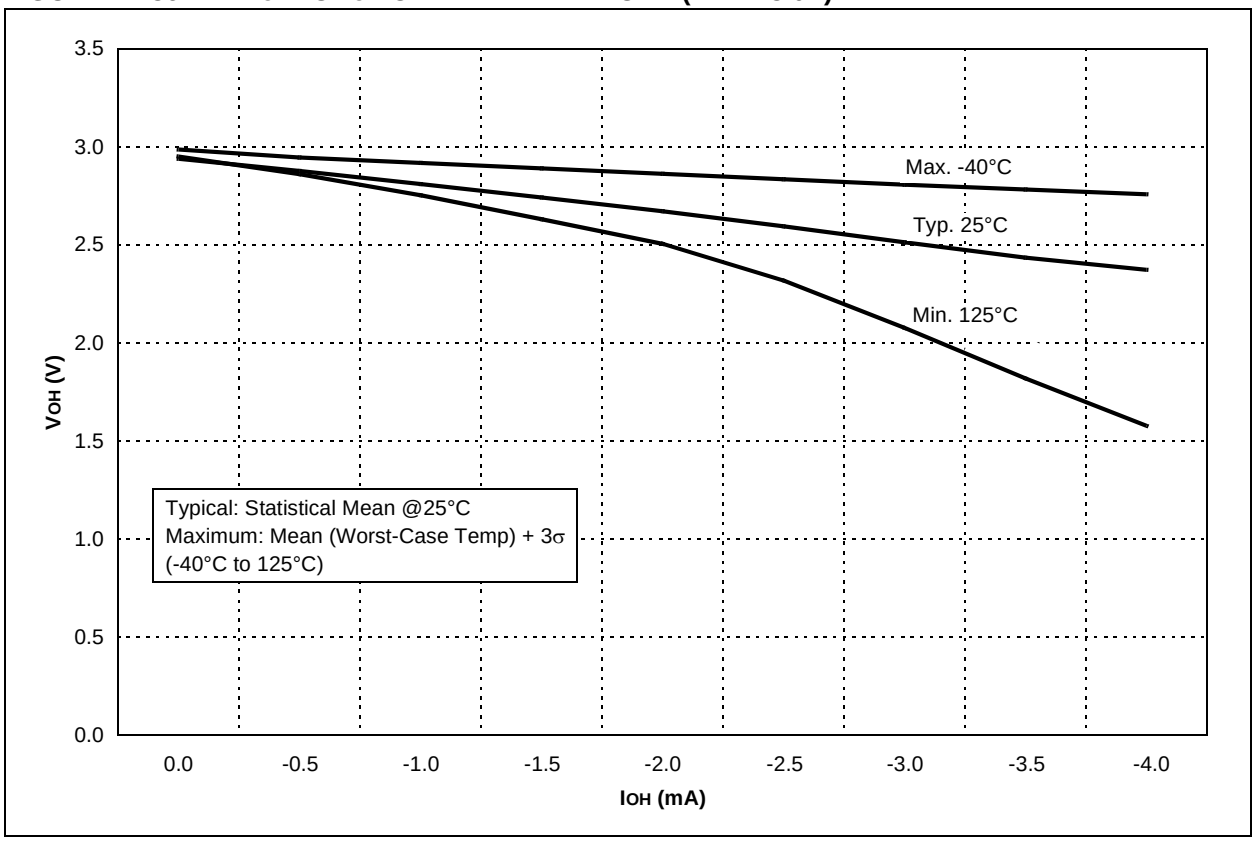


FIGURE 17-47: 0.6V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

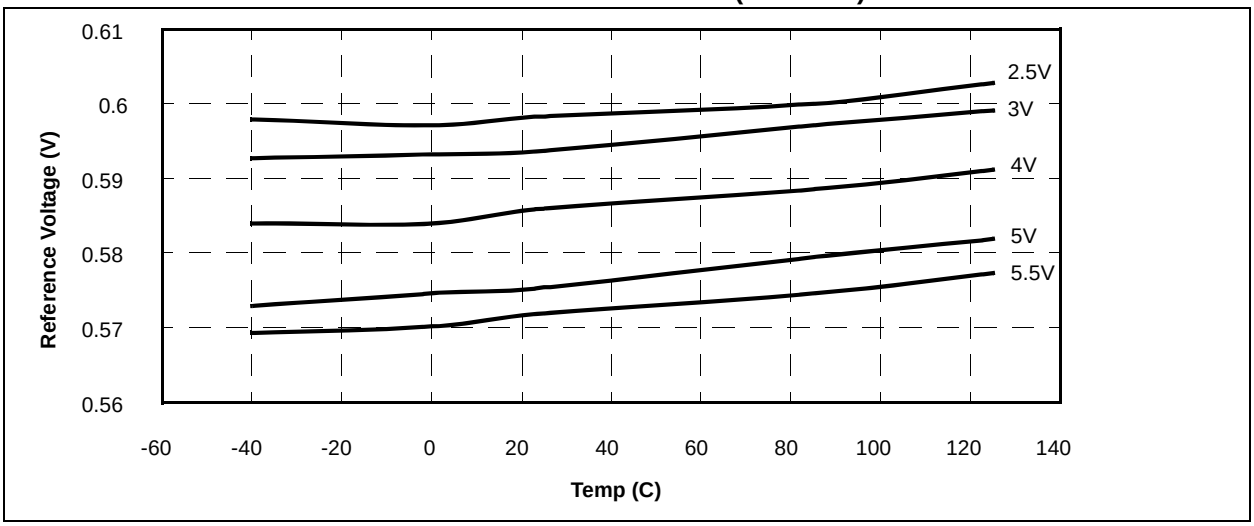


FIGURE 17-48: 1.2V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

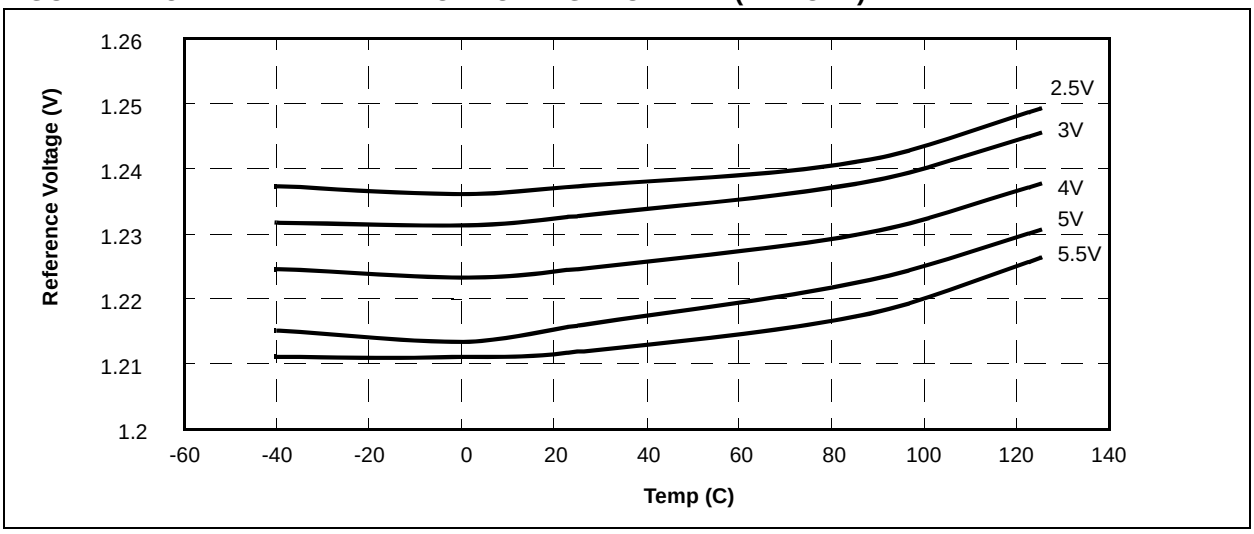
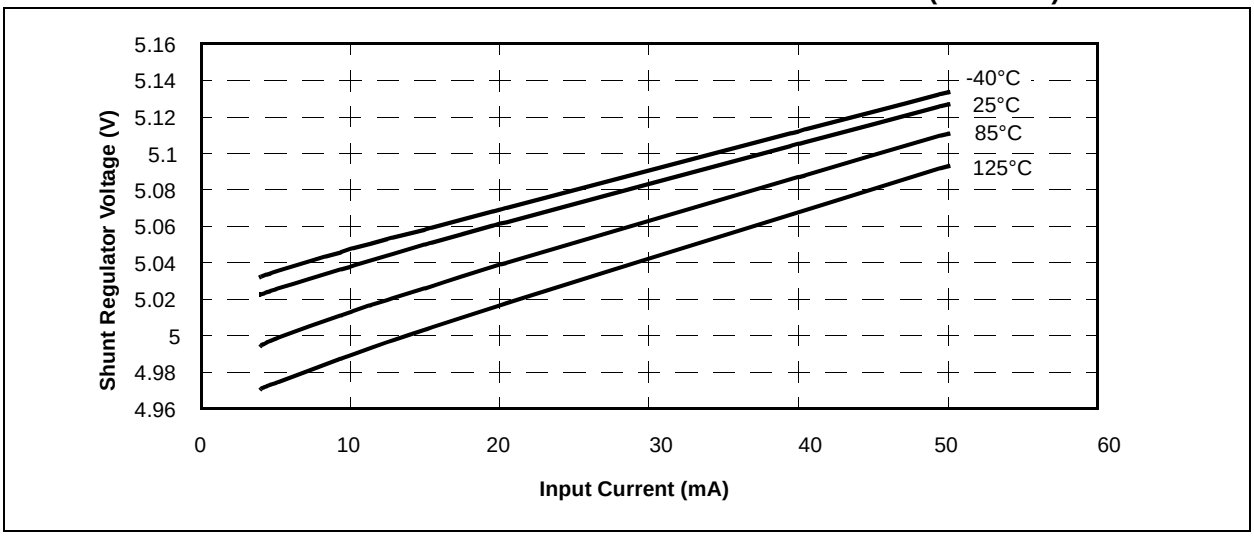


FIGURE 17-49: SHUNT REGULATOR VOLTAGE vs. INPUT CURRENT (TYPICAL)



NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC12F609, PIC12F609T(1), PIC12HV609, PIC12HV609T(1), PIC12F615, PIC12F615T(1), PIC12HV615, PIC12HV615T(1), PIC12F617, PIC12F617T(1)	
Temperature Range:	H = -40°C to +150°C	(High Temp)(3)
	I = -40°C to +85°C	(Industrial)
	E = -40°C to +125°C	(Extended)
Package:	P =	Plastic DIP (PDIP)
	SN =	8-lead Small Outline (150 mil) (SOIC)
	MS =	Micro Small Outline (MSOP)
	MF =	8-lead Plastic Dual Flat, No Lead (3x3) (DFN)
	MD =	8-lead Plastic Dual Flat, No Lead (4x4)(DFN)(1,2)
Pattern:	QTP, SQTP or ROM Code; Special Requirements (blank otherwise)	

Examples:

a) PIC12F615-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
b) PIC12F615-I/SN = Industrial Temp., SOIC package, 20 MHz
c) PIC12F615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
d) PIC12F609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
e) PIC12HV615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
f) PIC12HV609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
g) PIC12F617T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
h) PIC12F617-I/P = Industrial Temp., PDIP package, 20 MHz
i) PIC12F615-H/SN = High Temp., SOIC package, 20 MHz

Note 1: T = in tape and reel for MSOP, SOIC and DFN packages only.
2: Not available for PIC12F617.
3: High Temp. available for PIC12F615 only.