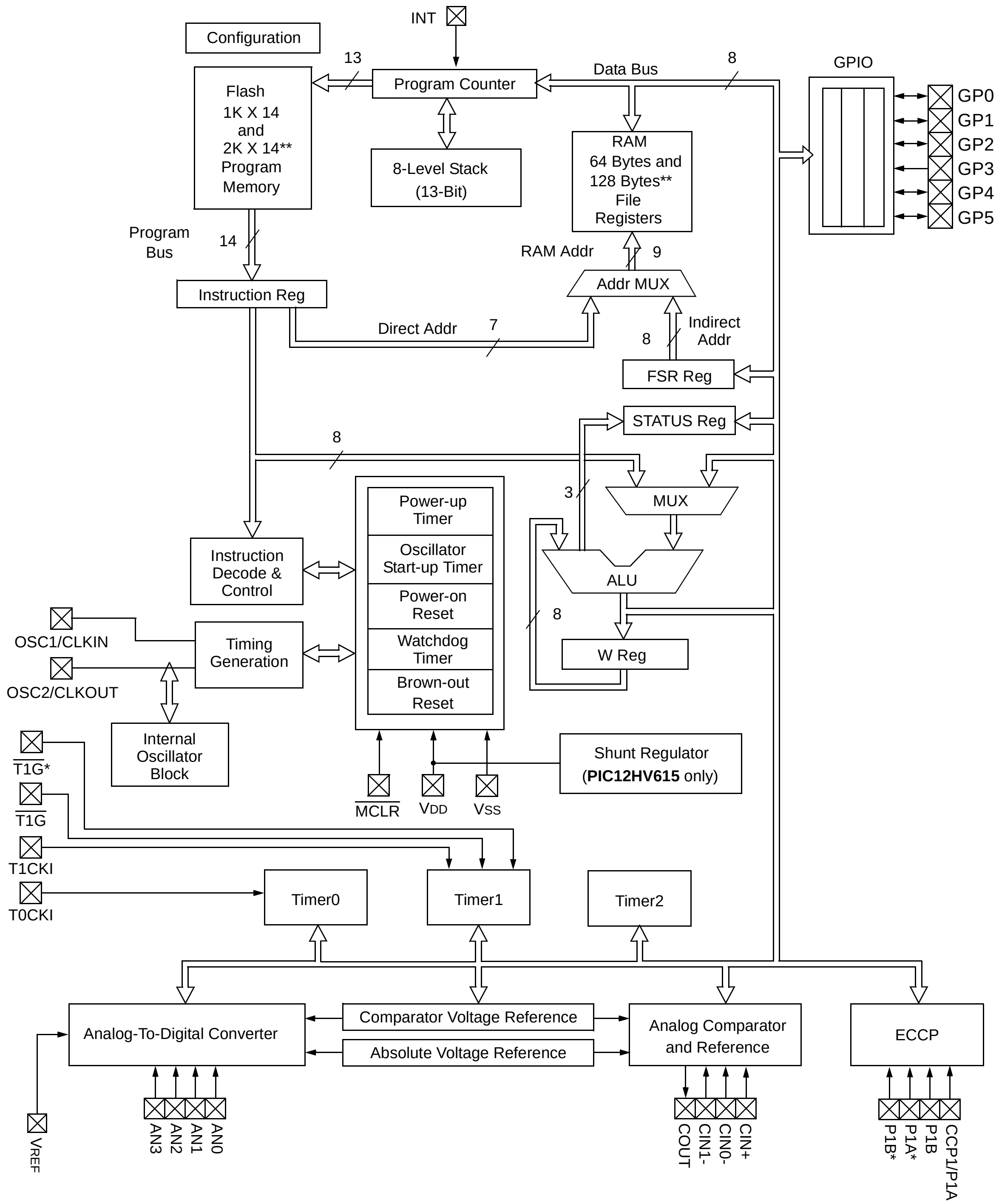
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f615t-i-sn

FIGURE 1-2: PIC12F615/617/HV615 BLOCK DIAGRAM



* Alternate pin function.
** For the PIC12F617 only.

TABLE 1-2: PIC12F615/617/HV615 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/AN0/CIN+/P1B/ICSPDAT	GP0	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	CIN+	AN	—	Comparator non-inverting input
	P1B	—	CMOS	PWM output
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
GP1/AN1/CIN0-/VREF/ICSPCLK	GP1	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	CIN0-	AN	—	Comparator inverting input
	VREF	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
GP2/AN2/T0CKI/INT/COUT/CCP1/P1A	GP2	ST	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
	COUT	—	CMOS	Comparator output
	CCP1	ST	CMOS	Capture input/Compare input/PWM output
	P1A	—	CMOS	PWM output
GP3/$\overline{\text{T1G}}$*/$\overline{\text{MCLR}}$/VPP	GP3	TTL	—	General purpose input with interrupt-on-change
	$\overline{\text{T1G}}$*	ST	—	Timer1 gate (count enable), alternate pin
	$\overline{\text{MCLR}}$	ST	—	Master Clear w/internal pull-up
	VPP	HV	—	Programming voltage
GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B*/OSC2/CLKOUT	GP4	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	AN3	AN	—	A/D Channel 3 input
	CIN1-	AN	—	Comparator inverting input
	$\overline{\text{T1G}}$	ST	—	Timer1 gate (count enable)
	P1B*	—	CMOS	PWM output, alternate pin
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	FOSC/4 output
GP5/T1CKI/P1A*/OSC1/CLKIN	GP5	TTL	CMOS	General purpose I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock input
	P1A*	—	CMOS	PWM output, alternate pin
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
VDD	VDD	Power	—	Positive supply
VSS	VSS	Power	—	Ground reference

* Alternate pin function.

Legend: AN=Analog input or output; CMOS=CMOS compatible input or output; HV= High Voltage; ST=Schmitt Trigger input with CMOS levels; TTL = TTL compatible input; XTAL=Crystal

2.2.2.4 PIE1 Register

The PIE1 register contains the Peripheral Interrupt Enable bits, as shown in Register 2-4.

Note:	Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit(1)
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit(1)
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **CMIE:** Comparator Interrupt Enable bit
1 = Enables the Comparator interrupt
0 = Disables the Comparator interrupt

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit(1)
1 = Enables the Timer2 to PR2 match interrupt
0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note 1: PIC12F615/617/HV615 only. PIC12F609/HV609 unimplemented, read as ‘0’.

2.2.2.7 APFCON Register (PIC12F615/617/HV615 only)

The Alternate Pin Function Control (APFCON) register is used to steer specific peripheral input and output functions between different pins. For this device, the P1A, P1B and Timer1 Gate functions can be moved between different pins.

The APFCON register bits are shown in Register 2-7.

REGISTER 2-7: APFCON:ALTERNATE PIN FUNCTION REGISTER(1)

U-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	—	T1GSEL	—	—	P1BSEL	P1ASEL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5	**Unimplemented:** Read as ‘0’
bit 4	**T1GSEL:** TMR1 Input Pin Select bit 1 = T1G function is on GP3/$\overline{\text{T1G}}$(2)/$\overline{\text{MCLR}}$/V_{PP} 0 = T1G function is on GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B(2)/OSC2/CLKOUT
bit 3-2	**Unimplemented:** Read as ‘0’
bit 1	**P1BSEL:** P1B Output Pin Select bit 1 = P1B function is on GP4/AN3/CIN1-/$\overline{\text{T1G}}$/P1B(2)/OSC2/CLKOUT 0 = P1B function is on GP0/AN0/CIN+/P1B/ICSPDAT
bit 0	**P1ASEL:** P1A Output Pin Select bit 1 = P1A function is on GP5/T1CKI/P1A(2)/OSC1/CLKIN 0 = P1A function is on GP2/AN2/T0CKI/INT/COUT/CCP1/P1A

Note 1: PIC12F615/617/HV615 only.

2: Alternate pin function.

4.0 OSCILLATOR MODULE

4.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the Oscillator module.

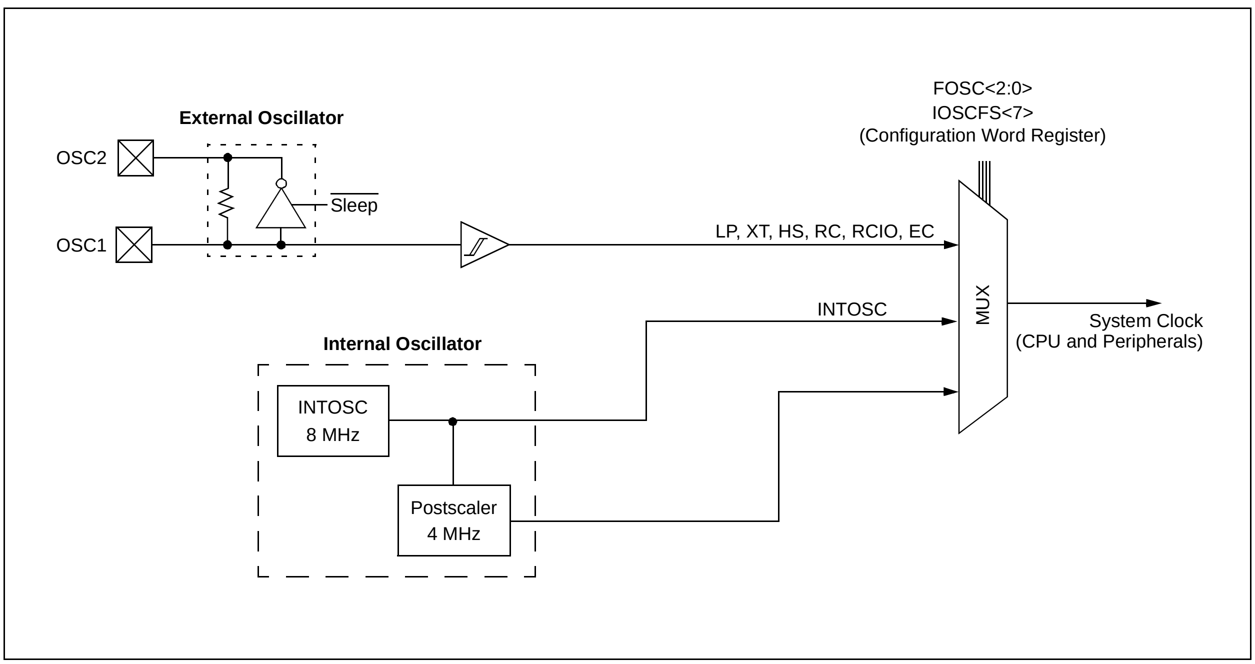
Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured with a choice of two selectable speeds: internal or external system clock source.

The Oscillator module can be configured in one of eight clock modes.

3. EC – External clock with I/O on OSC2/CLKOUT.
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
6. HS – High Gain Crystal or Ceramic Resonator mode.
7. RC – External Resistor-Capacitor (RC) with FOSC/4 output on OSC2/CLKOUT.
8. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
9. INTOSC – Internal oscillator with FOSC/4 output on OSC2 and I/O on OSC1/CLKIN.
10. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The Internal Oscillator module provides a selectable system clock mode of either 4 MHz (Postscaler) or 8 MHz (INTOSC).

FIGURE 4-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



REGISTER 6-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **$\overline{GPPU}$:** GPIO Pull-up Enable bit
1 = GPIO pull-ups are disabled
0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE	TMR0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000x
OPTION_REG	$\overline{GPPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: – = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

7.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected, the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

7.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge after one or more of the following conditions:

- Timer1 is enabled after POR or BOR Reset
- A write to TMR1H or TMR1L
- T1CKI is high when Timer1 is disabled and when Timer1 is re-enabled T1CKI is low. See Figure 7-2.

7.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

7.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO5 and TRISIO4 bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as ‘0’ and TRISIO5 and TRISIO4 bits read as ‘1’.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

7.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment.

Note:	In asynchronous counter mode or when using the internal oscillator and T1ACS=1, Timer1 can not be used as a time base for the capture or compare modes of the ECCP module (for PIC12F615/617/ HV615 only).

7.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TTMR1L register pair.

10.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
   - Disable pin output driver (See TRIS register)
   - Configure pin as analog
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Select result format
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt(1)
4. Wait the required acquisition time(2).
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1:	The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.
2:	See **Section 10.3 “A/D Acquisition Requirements”**.

EXAMPLE 10-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd reference, Frc clock
;and GP0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL  TRISIO       ;
BSF      TRISIO,0     ;Set GP0 to input
BANKSEL  ANSEL        ;
MOVLW    B’01110001’  ;ADC Frc clock,
IORWF    ANSEL        ; and GP0 as analog
BANKSEL  ADCON0       ;
MOVLW    B’10000001’  ;Right justify,
MOVWF    ADCON0       ;Vdd Vref, AN0, On
CALL     SampleTime   ;Acquisiton delay
BSF      ADCON0,GO    ;Start conversion
BTFSC    ADCON0,GO    ;Is conversion done?
GOTO     $-1          ;No, test again
BANKSEL  ADRESH       ;
MOVF     ADRESH,W     ;Read upper 2 bits
MOVWF    RESULTHI     ;Store in GPR space
BANKSEL  ADRESL       ;
MOVF     ADRESL,W     ;Read lower 8 bits
MOVWF    RESULTLO     ;Store in GPR space
```

TABLE 11-2: SUMMARY OF REGISTERS ASSOCIATED WITH CAPTURE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	0-00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	uuuu uuuu
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	-00- 0-00	-00- 0-00
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: - = Unimplemented locations, read as ‘0’, u = unchanged, x = unknown. Shaded cells are not used by the Capture.

Note 1: For PIC12F615/617/HV615 only.

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 1

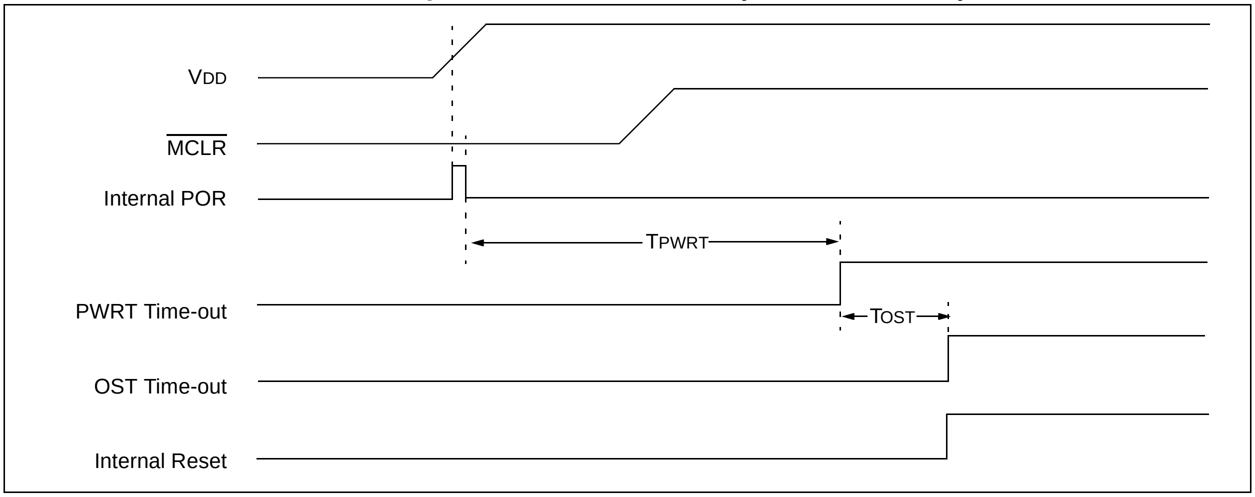


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR): CASE 2

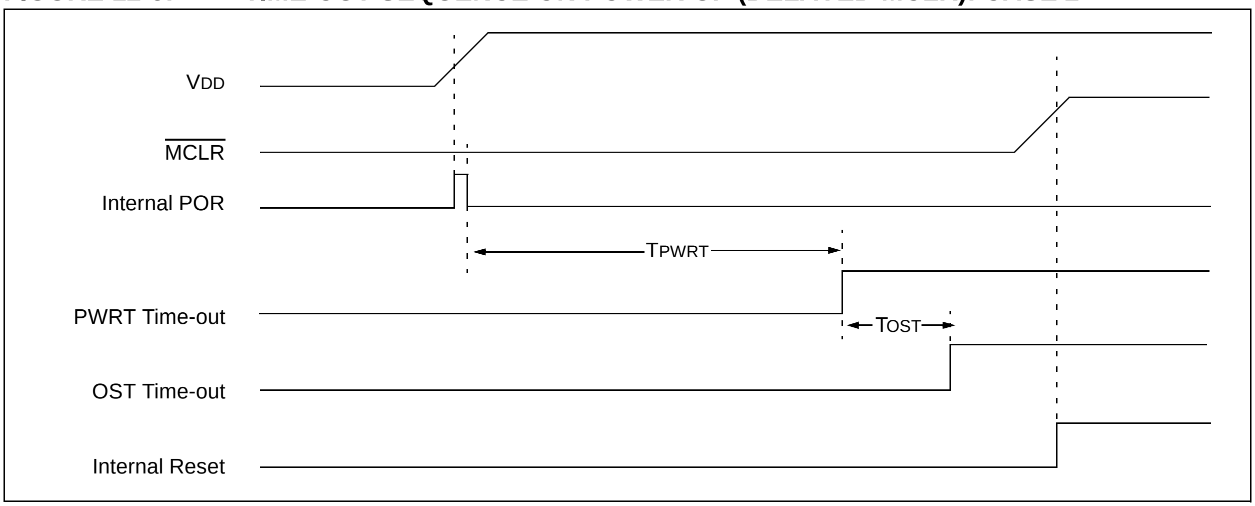
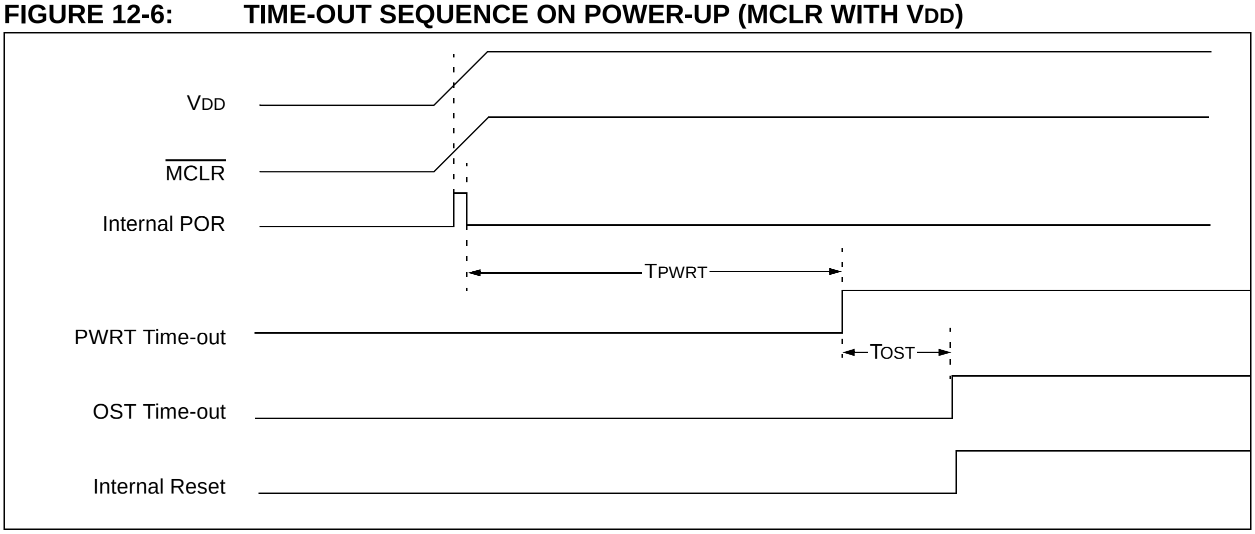


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR WITH VDD)



12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-3). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 12-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC12F609/615/617/12HV609/615 does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

12.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time out generates a device Reset. If the device is in Sleep mode, a WDT time out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (**Section 12.1 "Configuration Bits"**).

12.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

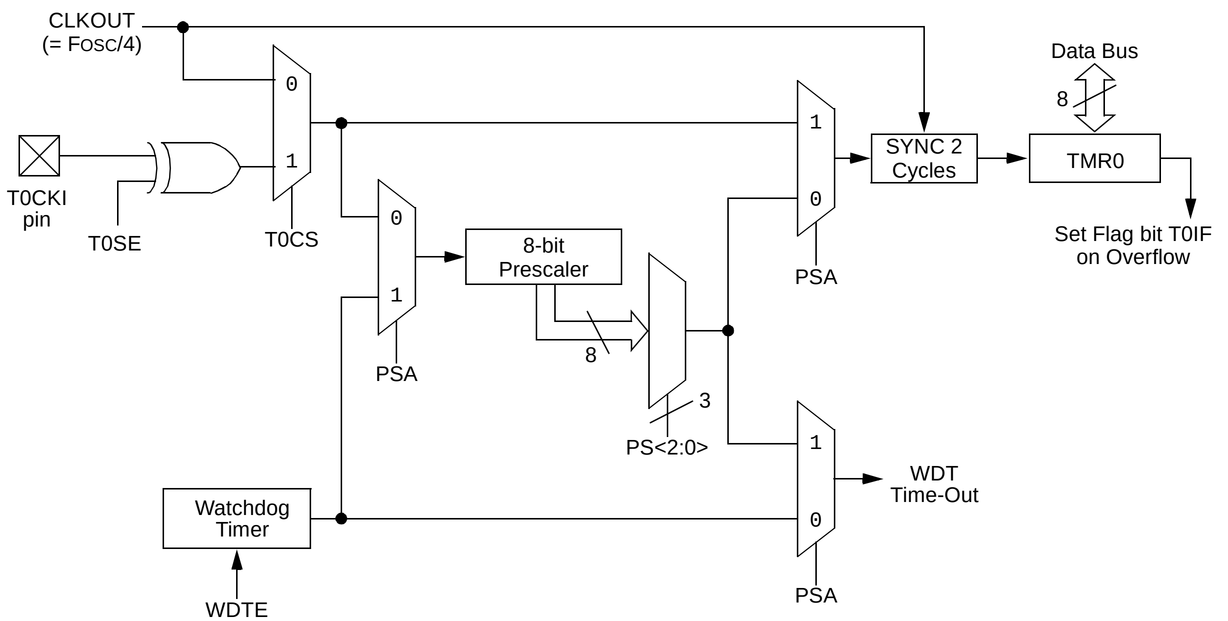
The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time out.

12.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst-case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time out occurs.

FIGURE 12-2: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: T0SE, T0CS, PSA, PS<2:0> are bits in the OPTION register.

TABLE 12-8: WDT STATUS

Conditions	WDT
WDTE = 0	Cleared
CLRWDT Command	Cleared
Oscillator Fail Detected	Cleared
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	Cleared
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

TABLE 12-9: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
OPTION_REG	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
CONFIG	IOSCFS	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.
Note 1: See Register 12-1 for operation of all Configuration Word register bits.

12.10 In-Circuit Serial Programming™

ThePIC12F609/615/617/12HV609/615 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

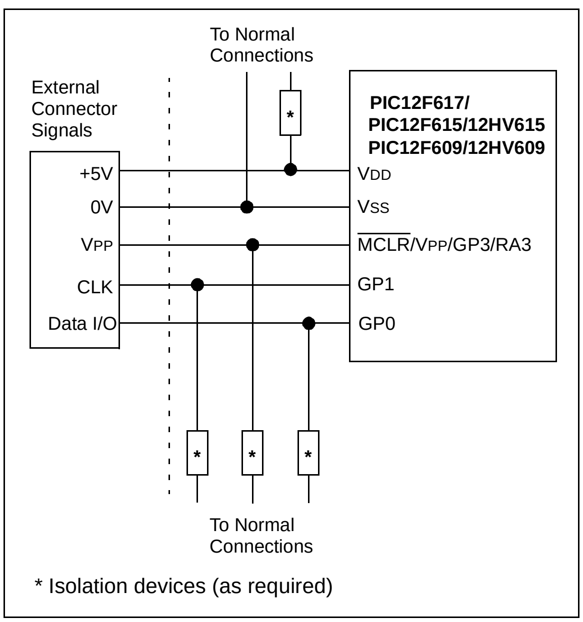
- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the *Memory Programming Specification* (DS41284) for more information. GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 12-10.

FIGURE 12-10: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



Note:	To erase the device VDD must be above the Bulk Erase VDD minimum given in the *Memory Programming Specification* (DS41284)

12.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with an 14-pin device is not practical. A special 28-pin PIC12F609/615/617/12HV609/615 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC12F609/615/617/12HV609/615 device. The debugging adapter is the only source of the ICD device.

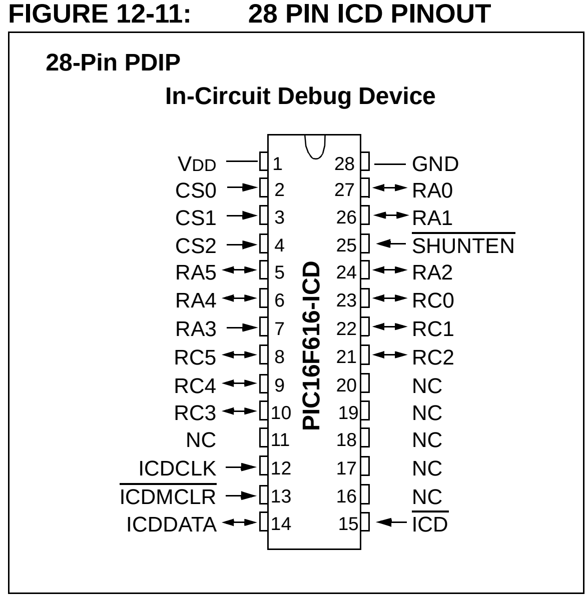
When the ICD pin on the PIC12F609/615/617/12HV609/615 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-10 shows which features are consumed by the background debugger.

TABLE 12-10: DEBUGGER RESOURCES

Resource	Description
I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be NOP 700h-7FFh

For more information, see "*MPLAB® ICD 2 In-Circuit Debugger User's Guide"* (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 12-11: 28 PIN ICD PINOUT



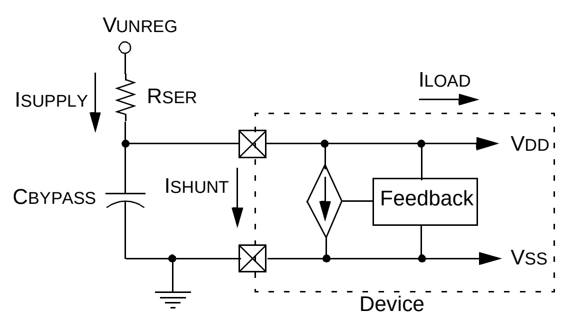
13.0 VOLTAGE REGULATOR

The PIC12HV609/HV615 devices include a permanent internal 5 volt (nominal) shunt regulator in parallel with the V_{DD} pin. This eliminates the need for an external voltage regulator in systems sourced by an unregulated supply. All external devices connected directly to the V_{DD} pin will share the regulated supply voltage and contribute to the total V_{DD} supply current (I_{LOAD}).

13.1 Regulator Operation

A shunt regulator generates a specific supply voltage by creating a voltage drop across a pass resistor R_{SER}. The voltage at the V_{DD} pin of the microcontroller is monitored and compared to an internal voltage reference. The current through the resistor is then adjusted, based on the result of the comparison, to produce a voltage drop equal to the difference between the supply voltage V_{UNREG} and the V_{DD} of the microcontroller. See Figure 13-1 for voltage regulator schematic.

FIGURE 13-1: VOLTAGE REGULATOR



An external current limiting resistor, R_{SER}, located between the unregulated supply, V_{UNREG}, and the V_{DD} pin, drops the difference in voltage between V_{UNREG} and V_{DD}. R_{SER} must be between R_{MAX} and R_{MIN} as defined by Equation 13-1.

EQUATION 13-1: R_{SER} LIMITING RESISTOR

$$R_{MAX} = \frac{(V_{UMIN} - 5V)}{1.05 \cdot (4\ mA + I_{LOAD})}$$

$$R_{MIN} = \frac{(V_{UMAX} - 5V)}{0.95 \cdot (50\ mA)}$$

Where:

R_{MAX} = maximum value of R_{SER} (ohms)

R_{MIN} = minimum value of R_{SER} (ohms)

V_{UMIN} = minimum value of V_{UNREG}

V_{UMAX} = maximum value of V_{UNREG}

V_{DD} = regulated voltage (5V nominal)

I_{LOAD} = maximum expected load current in mA including I/O pin currents and external circuits connected to V_{DD}.

1.05 = compensation for +5% tolerance of R_{SER}

0.95 = compensation for -5% tolerance of R_{SER}

13.2 Regulator Considerations

The supply voltage V_{UNREG} and load current are not constant. Therefore, the current range of the regulator is limited. Selecting a value for R_{SER} must take these three factors into consideration.

Since the regulator uses the band gap voltage as the regulated voltage reference, this voltage reference is permanently enabled in the PIC12HV609/HV615 devices.

The shunt regulator will still consume current when below operating voltage range for the shunt regulator.

13.3 Design Considerations

For more information on using the shunt regulator and managing current load, see Application Note AN1035, "*Designing with HV Microcontrollers"* (DS01035).

RETFIE	**Return from Interrupt**
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
Example:	RETFIE
	After Interrupt PC = TOS GIE = 1

RETLW	**Return with literal in W**
Syntax:	[*label*] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2

Example:

```
        CALL TABLE;W contains
                  ;table offset
                  ;value
        GOTO DONE
TABLE   •
        •
        ADDWF PC  ;W = offset
        RETLW k1  ;Begin table
        RETLW k2  ;
        •
        •
        •
        RETLW kn  ;End of table
DONE
```

Before Instruction
W = 0x07
After Instruction
W = value of k8

RETURN	**Return from Subroutine**
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

16.3 DC Characteristics: PIC12HV609/615-I (Industrial) PIC12HV609/615-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	**Supply Current (IDD)**(1, 2) PIC12HV609/615	—	160	230	μA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	240	310	μA	3.0	
		—	280	400	μA	4.5	
D011*		—	270	380	μA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	400	560	μA	3.0	
		—	520	780	μA	4.5	
D012		—	380	540	μA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	575	810	μA	3.0	
		—	0.875	1.3	mA	4.5	
D013*		—	215	310	μA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	375	565	μA	3.0	
		—	570	870	μA	4.5	
D014		—	330	475	μA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	550	800	μA	3.0	
		—	0.85	1.2	mA	4.5	
D016*		—	310	435	μA	2.0	FOSC = 4 MHz INTOSC mode
		—	500	700	μA	3.0	
		—	0.74	1.1	mA	4.5	
D017		—	460	650	μA	2.0	FOSC = 8 MHz INTOSC mode
		—	0.75	1.1	mA	3.0	
		—	1.2	1.6	mA	4.5	
D018		—	320	465	μA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	510	750	μA	3.0	
		—	0.770	1.0	mA	4.5	
D019		—	2.5	3.4	mA	4.5	FOSC = 20 MHz HS Oscillator mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{MCLR}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ.

16.7 DC Characteristics: PIC12HV609/615-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020E	**Power-down Base Current (IPD)**(2,3) PIC12HV609/615	—	135	200	μA	2.0	WDT, BOR, Comparator, VREF and T1OSC disabled
		—	210	280	μA	3.0	
		—	260	350	μA	4.5	
D021E		—	135	200	μA	2.0	WDT Current(1)
		—	210	285	μA	3.0	
		—	265	360	μA	4.5	
D022E		—	215	285	μA	3.0	BOR Current(1)
		—	265	360	μA	4.5	
D023E		—	185	280	μA	2.0	Comparator Current(1), single comparator enabled
		—	265	360	μA	3.0	
		—	320	430	μA	4.5	
D024E		—	165	235	μA	2.0	CVREF Current(1) (high range)
		—	255	330	μA	3.0	
		—	330	430	μA	4.5	
D025E*		—	175	245	μA	2.0	CVREF Current(1) (low range)
		—	275	350	μA	3.0	
		—	355	450	μA	4.5	
D026E		—	140	205	μA	2.0	T1OSC Current(1), 32.768 kHz
		—	220	290	μA	3.0	
		—	270	360	μA	4.5	
D027E		—	210	280	μA	3.0	A/D Current(1), no conversion in progress
		—	260	350	μA	4.5	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 4.5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: Shunt regulator is always on and always draws operating current.

16.10 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

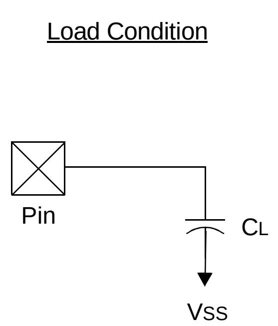
Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	$\overline{\text{RD}}$
cs	$\overline{\text{CS}}$	rw	$\overline{\text{RD}}$ or $\overline{\text{WR}}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{\text{SS}}$
dt	Data in	t0	T0CKI
io	I/O Port	t1	T1CKI
mc	$\overline{\text{MCLR}}$	wr	$\overline{\text{WR}}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 16-3: LOAD CONDITIONS



Legend: C_L=50 pF for all pins
15 pF for OSC2 output

17.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where s is a standard deviation, over each temperature range.

FIGURE 17-1: PIC12F609/615/617 IDD LP (32 kHz) vs. VDD

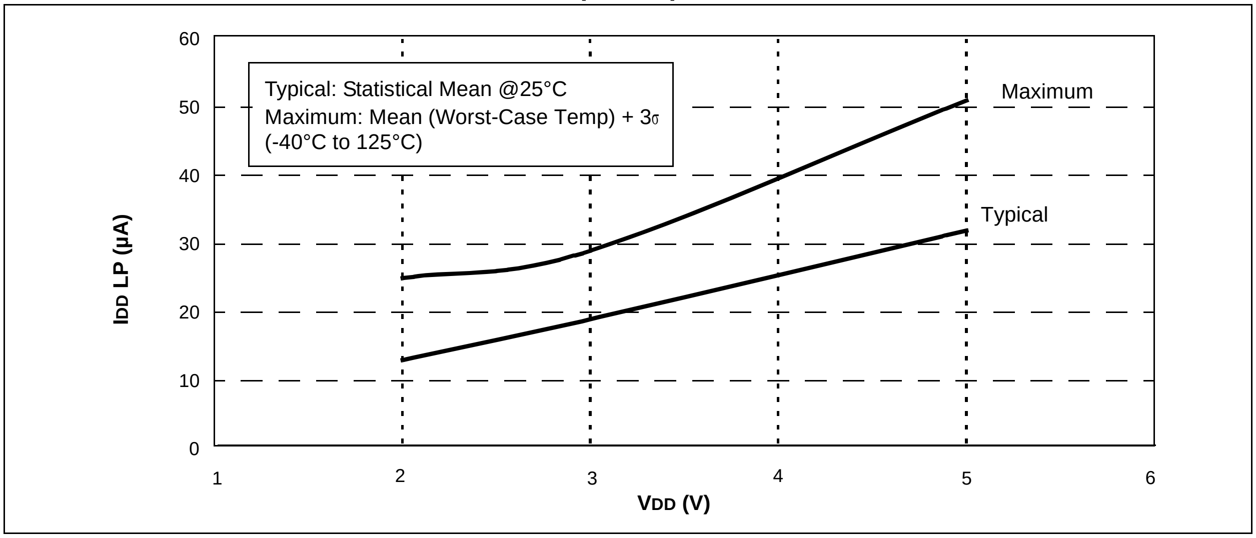
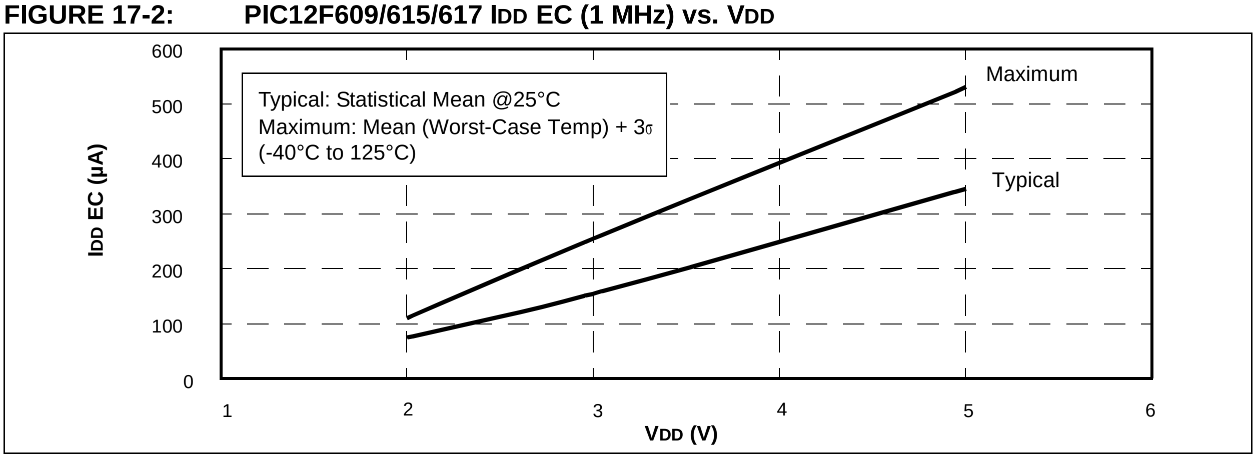


FIGURE 17-2: PIC12F609/615/617 IDD EC (1 MHz) vs. VDD



NOTES: