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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12hv609-i-ms

PIC12F609/615/617/12HV609/615

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F609/615/617/12HV609/615 has a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) for the PIC12F609/615/12HV609/615 is physically implemented. For the PIC12F617, the first 2K x 14 (0000h-07FFh) is physically implemented. Accessing a location above these boundaries will cause a wrap-around within the first 1K x 14 space for PIC12F609/615/12HV609/615 devices, and within the first 2K x 14 space for the PIC12F617 device. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F609/615/12HV609/615

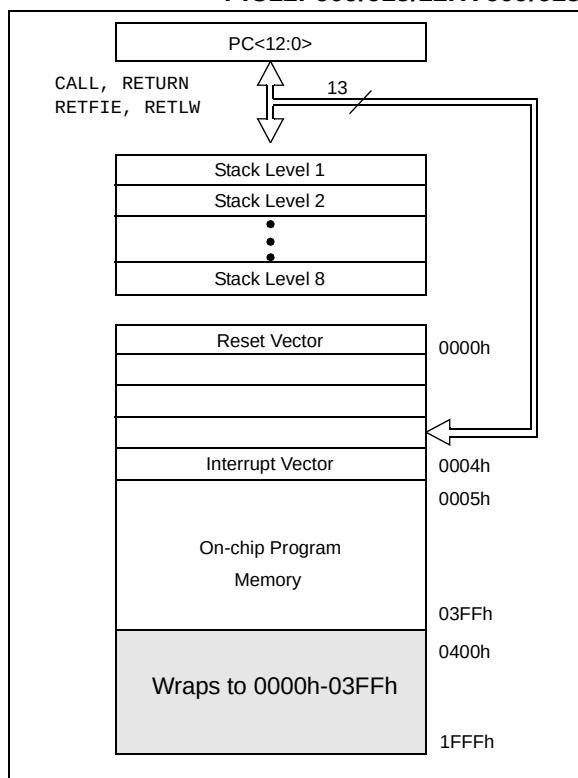
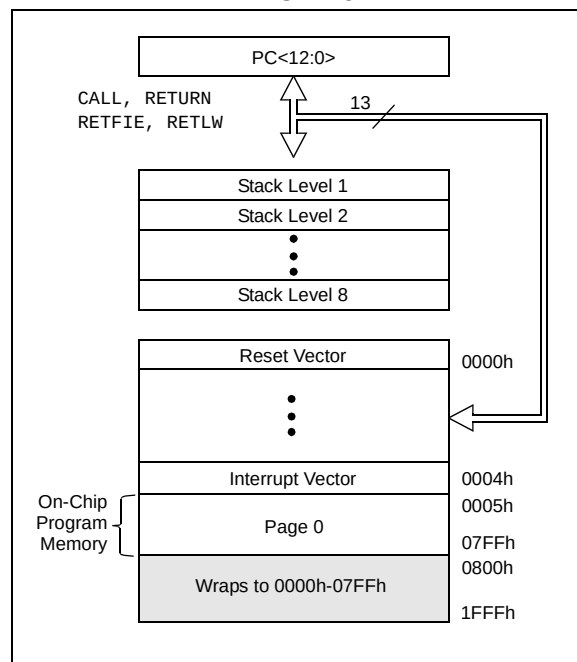


FIGURE 2-2: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F617



2.2 Data Memory Organization

The data memory (see Figure 2-3) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 40h-7Fh in Bank 0 are General Purpose Registers, implemented as static RAM. For the PIC12F617, the register locations 20h-7Fh in Bank 0 and A0h-EFh in Bank 1 are general purpose registers implemented as Static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. The RP0 bit of the STATUS register is the bank select bit.

RP0

- 0 → Bank 0 is selected
- 1 → Bank 1 is selected

Note: The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's.

PIC12F609/615/617/12HV609/615

TABLE 2-2: PIC12F615/617/HV615 SPECIAL FUNCTION REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	25, 116
01h	TMR0	Timer0 Module's Register								xxxx xxxx	53, 116
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	25, 116
03h	STATUS	IRP ⁽¹⁾	RP1 ⁽¹⁾	RP0	T0	PD	Z	DC	C	0001 1xxx	18, 116
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	25, 116
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--x0 x000	43, 116
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter				---	0 0000	25, 116
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	20, 116
0Ch	PIR1	—	ADIF	CCP1IF	—	CMIF	—	TMR2IF	TMR1IF	-00- 0-00	22, 116
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 116
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	57, 116
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	62, 116
11h	TMR2 ⁽³⁾	Timer2 Module Register								0000 0000	65, 116
12h	T2CON ⁽³⁾	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	66, 116
13h	CCPR1L ⁽³⁾	Capture/Compare/PWM Register 1 Low Byte								XXXX XXXX	90, 116
14h	CCPR1H ⁽³⁾	Capture/Compare/PWM Register 1 High Byte								XXXX XXXX	90, 116
15h	CCP1CON ⁽³⁾	P1M	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	0-00 0000	89, 116
16h	PWM1CON ⁽³⁾	PRSEN	PDC6	PDC5	PDC4	PDC3	PDC2	PDC1	PDC0	0000 0000	105, 116
17h	ECCPAS ⁽³⁾	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1	PSSBD0	0000 0000	102, 116
18h	—	Unimplemented								—	—
19h	VRCON	CMVREN	—	VRR	FVREN	VR3	VR2	VR1	VR0	0-00 0000	76, 116
1Ah	CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -0-0	72, 116
1Bh	—	Unimplemented								—	—
1Ch	CMCON1	—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC	---0 0-10	73, 116
1Dh	—	Unimplemented								—	—
1Eh	ADRESH ^(2, 3)	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	85, 116
1Fh	ADCON0 ⁽³⁾	ADFM	VCFG	—	CHS2	CHS1	CHS0	GO/DONE	ADON	00-0 0000	84, 116

Legend: — = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition, shaded = unimplemented

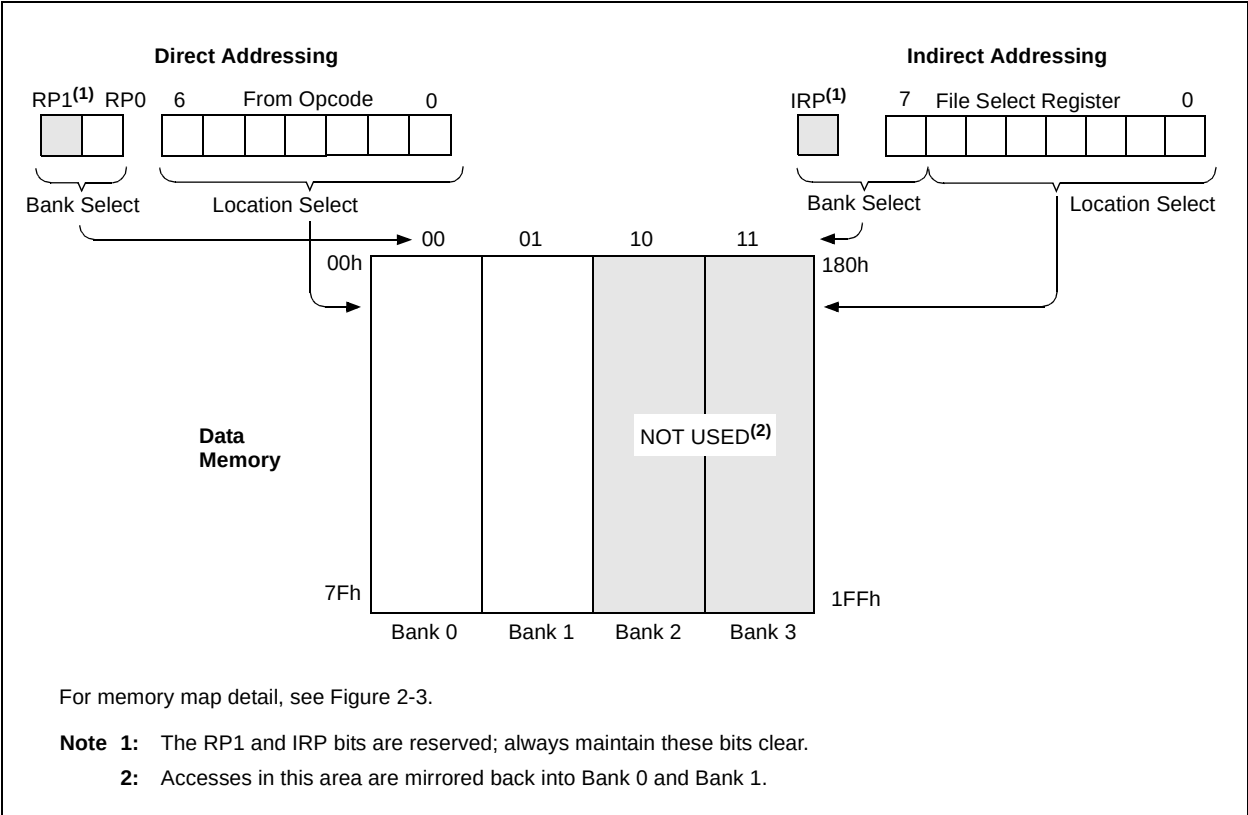
Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: Read only register.

3: PIC12F615/617/HV615 only.

PIC12F609/615/617/12HV609/615

FIGURE 2-6: DIRECT/INDIRECT ADDRESSING PIC12F609/615/617/12HV609/615



PIC12F609/615/617/12HV609/615

3.3 Reading the Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the PMADRL and PMADRH registers, and then set control bit RD (PMCON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle after to read the data. This causes the second instruction immediately following the “BSF PMCON1,RD” instruction to be ignored. The data is available in the very next cycle in the PMDATL and PMDATH registers; it can be read as two bytes in the following instructions. PMDATL and PMDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-1: FLASH PROGRAM READ

```
BANKSEL PM_ADR      ; Change STATUS bits RP1:0 to select bank with PMADRL
MOVLW  MS_PROG_PM_ADDR ;
MOVWF  PMADRH      ; MS Byte of Program Address to read
MOVLW  LS_PROG_PM_ADDR ;
MOVWF  PMADRL      ; LS Byte of Program Address to read
BANKSEL PMCON1      ; Bank to containing PMCON1
BSF    PMCON1, RD   ; PM Read

NOP                ; First instruction after BSF PMCON1,RD executes normally

NOP                ; Any instructions here are ignored as program
                  ; memory is read in second cycle after BSF PMCON1,RD
                  ;
BANKSEL PMDATL      ; Bank to containing PMADRL
MOVF   PMDATL, W    ; W = LS Byte of Program PMDATL
MOVF   PMDATH, W    ; W = MS Byte of Program PMDATL
```

4.3.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 4-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

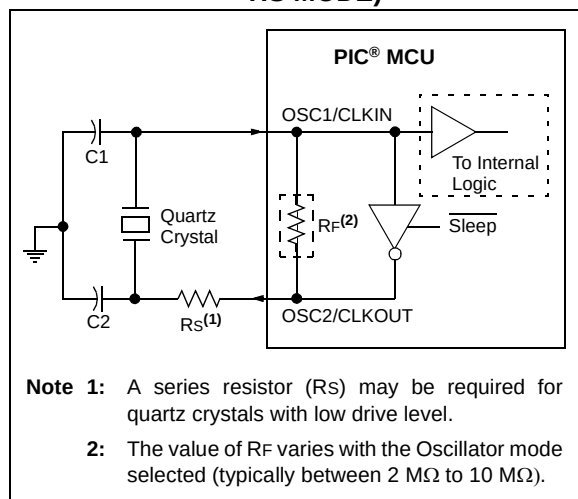
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 4-3 and Figure 4-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 4-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



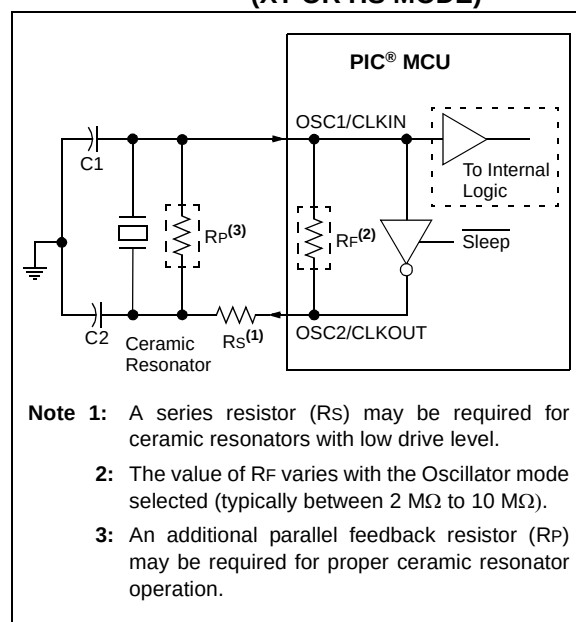
Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Applications Notes:

- AN826, "Crystal Oscillator Basics and Crystal Selection for rPIC[®] and PIC[®] Devices" (DS00826)
- AN849, "Basic PIC[®] Oscillator Design" (DS00849)
- AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
- AN949, "Making Your Oscillator Work" (DS00949)

FIGURE 4-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



PIC12F609/615/617/12HV609/615

REGISTER 6-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 7 **GPPU:** GPIO Pull-up Enable bit
 1 = GPIO pull-ups are disabled
 0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register
- bit 6 **INTEDG:** Interrupt Edge Select bit
 1 = Interrupt on rising edge of INT pin
 0 = Interrupt on falling edge of INT pin
- bit 5 **T0CS:** TMR0 Clock Source Select bit
 1 = Transition on T0CKI pin
 0 = Internal instruction cycle clock (Fosc/4)
- bit 4 **T0SE:** TMR0 Source Edge Select bit
 1 = Increment on high-to-low transition on T0CKI pin
 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA:** Prescaler Assignment bit
 1 = Prescaler is assigned to the WDT
 0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

BIT VALUE TMR0 RATE WDT RATE

000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000x
OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	- -11 1111	- -11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

9.5 Comparator Interrupt Operation

The comparator interrupt flag can be set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 9-4 and Figure 9-5). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. At this point the two mismatch latches have opposite output levels which is detected by the exclusive-or gate and fed to the interrupt circuitry. The mismatch condition persists until either the CMCON0 register is read or the comparator output returns to the previous state.

Note 1: A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

2: Comparator interrupts will operate correctly regardless of the state of CMOE.

The comparator interrupt is set by the mismatch edge and not the mismatch level. This means that the interrupt flag can be reset without the additional step of reading or writing the CMCON0 register to clear the mismatch registers. When the mismatch registers are cleared, an interrupt will occur upon the comparator's return to the previous state, otherwise no interrupt will be generated.

Software will need to maintain information about the status of the comparator output, as read from the CMCON1 register, to determine the actual change that has occurred.

The CMIF bit of the PIR1 register is the Comparator Interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, an interrupt can be generated.

The CMIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CMIF bit of the PIR1 register will still be set if an interrupt condition occurs.

FIGURE 9-4: COMPARATOR INTERRUPT TIMING W/O CMCON0 READ

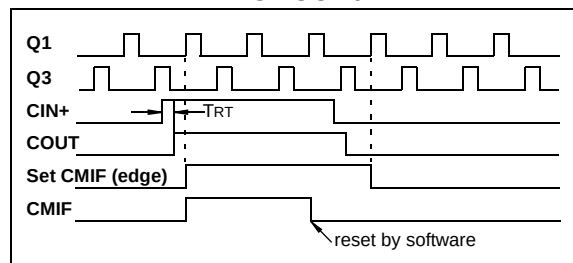
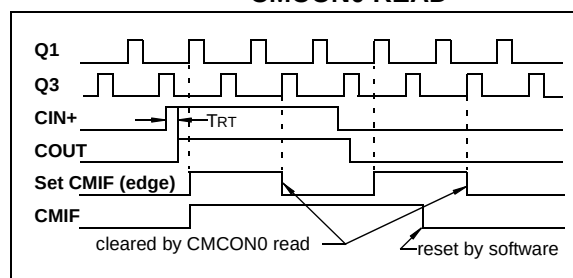


FIGURE 9-5: COMPARATOR INTERRUPT TIMING WITH CMCON0 READ



Note 1: If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF of the PIR1 register interrupt flag may not get set.

2: When a comparator is first enabled, bias circuitry in the comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μ s for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

9.8 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See **Section 7.0 “Timer1 Module with Gate Control”** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

9.9 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 7-1) for more information.

REGISTER 9-2: CMCON1: COMPARATOR CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **T1ACS:** Timer1 Alternate Clock Select bit

1 = Timer 1 Clock Source is System Clock (Fosc)

0 = Timer 1 Clock Source is Instruction Clock (Fosc/4)

bit 3 **CMHYS:** Comparator Hysteresis Select bit

1 = Comparator Hysteresis enabled

0 = Comparator Hysteresis disabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit⁽¹⁾

1 = Timer 1 Gate Source is $\overline{T1G}$ pin (pin should be configured as digital input)

0 = Timer 1 Gate Source is comparator output

bit 0 **CMSYNC:** Comparator Output Synchronization bit⁽²⁾

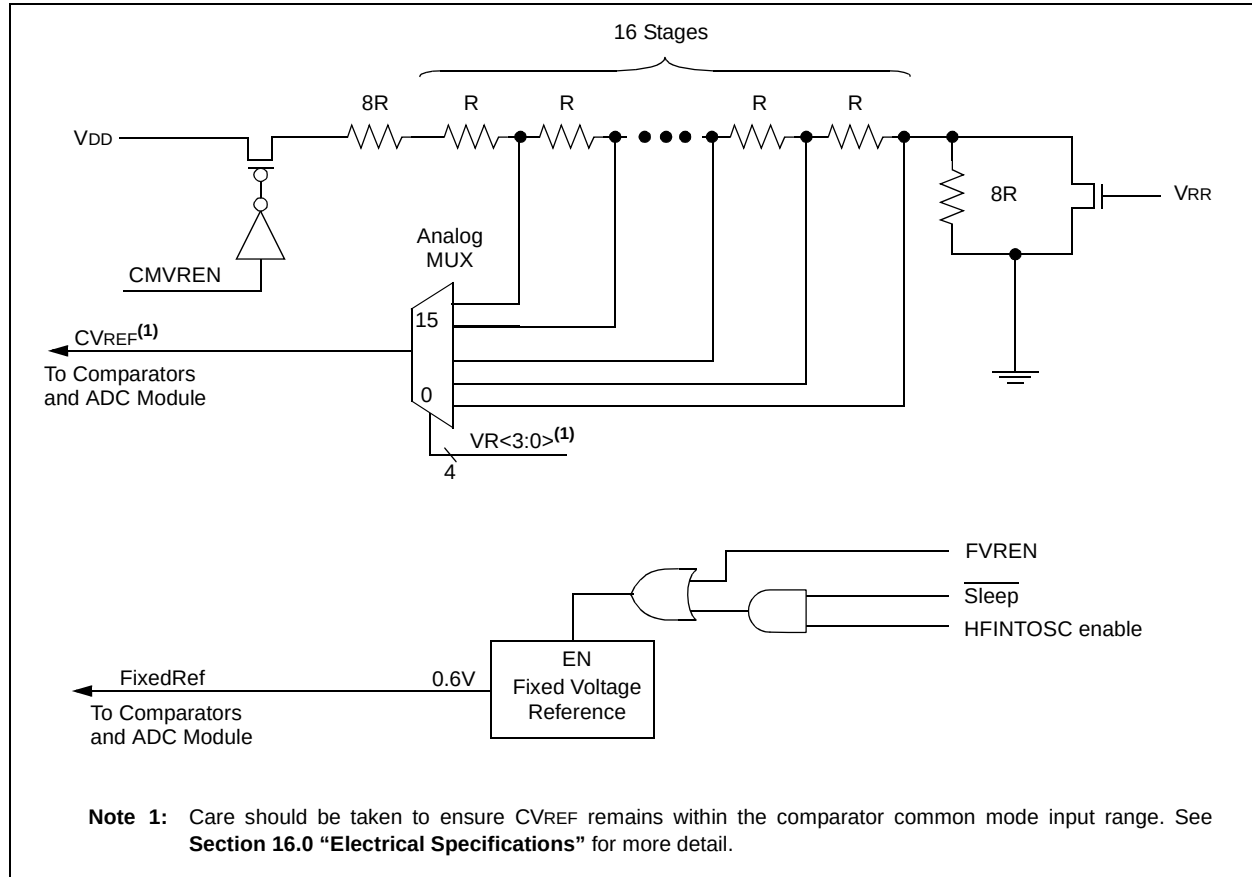
1 = Output is synchronized with falling edge of Timer1 clock

0 = Output is asynchronous

Note 1: Refer to **Section 7.6 “Timer1 Gate”**.

2: Refer to Figure 9-2.

FIGURE 9-6: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



10.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 10-4. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), see Figure 10-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed),

an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 10-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 10-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10kΩ 5.0V VDD

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/^\circ C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{2047} \right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within } 1/2 \text{ lsb}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{\frac{-T_C}{RC}} \right) = V_{APPLIED} \left(1 - \frac{1}{2047} \right) \quad ;\text{combining [1] and [2]}$$

Solving for TC:

$$\begin{aligned} T_C &= -CHOLD(RIC + R_{SS} + R_S) \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.37\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/^\circ C)] \\ &= 4.67\mu s \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

PIC12F609/615/617/12HV609/615

12.2 Calibration Bits

The 8 MHz internal oscillator is factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the *Memory Programming Specification* (DS41204) and thus, does not require reprogramming.

12.3 Reset

The PIC12F609/615/617/12HV609/615 device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- MCLR Reset during normal operation
- MCLR Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

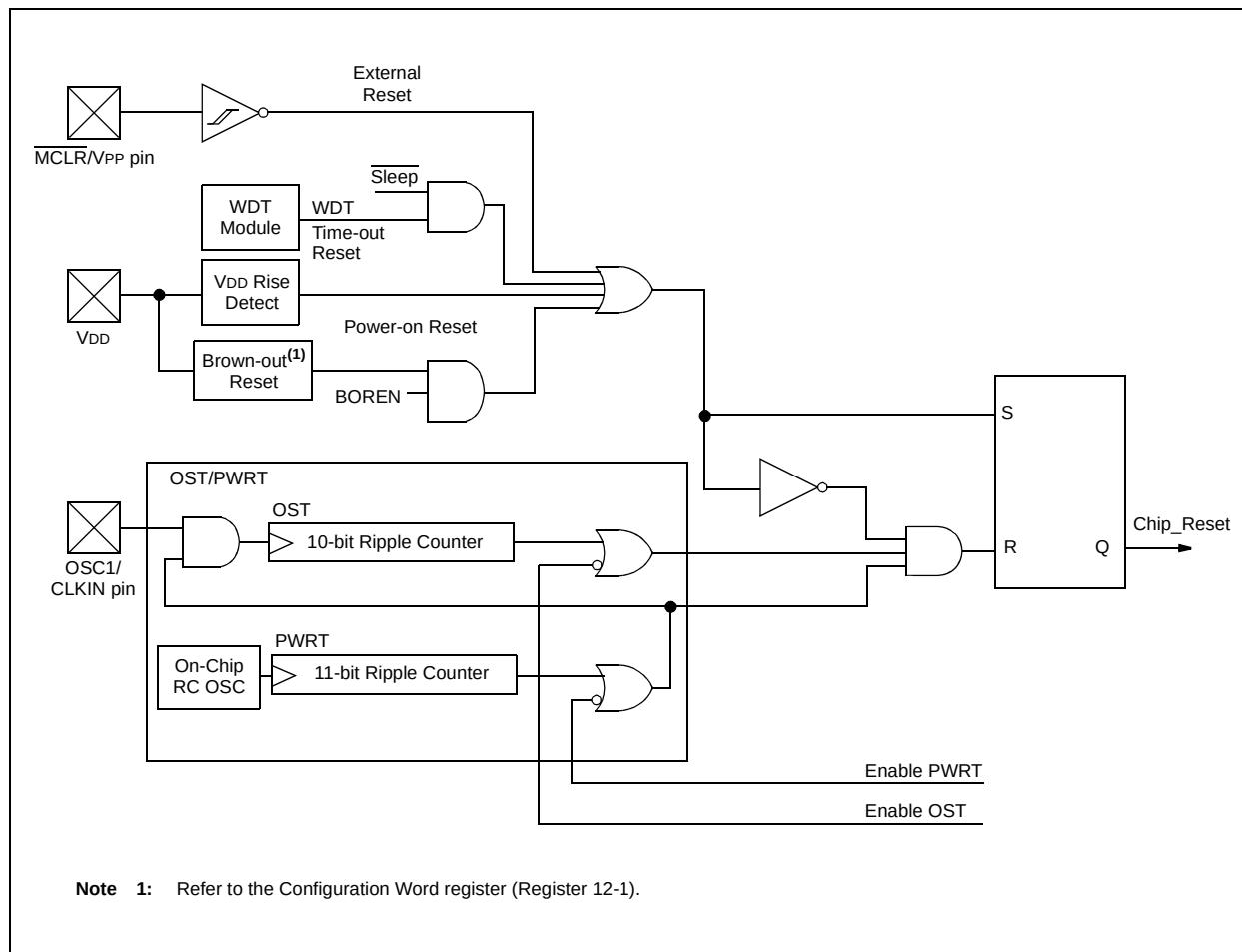
- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. $\overline{TO}$ and $\overline{PD}$ bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-5 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See **Section 16.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



PIC12F609/615/617/12HV609/615

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 1

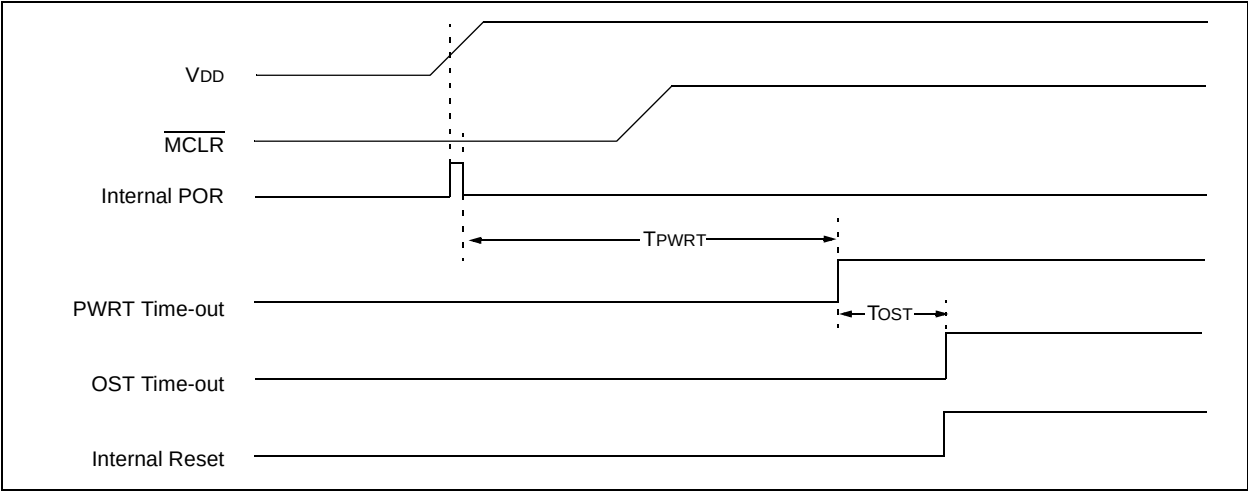


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED $\overline{\text{MCLR}}$): CASE 2

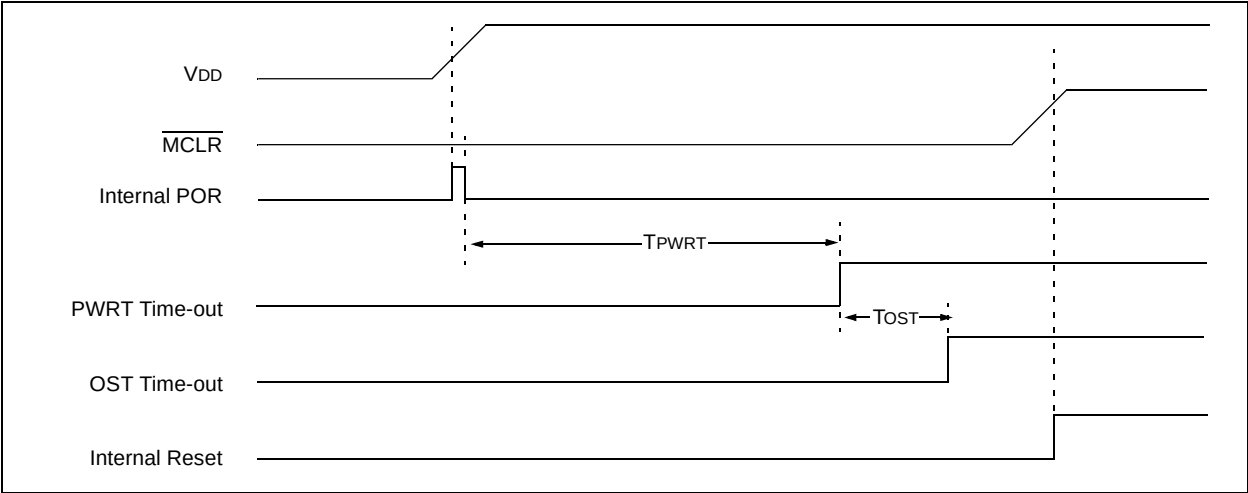
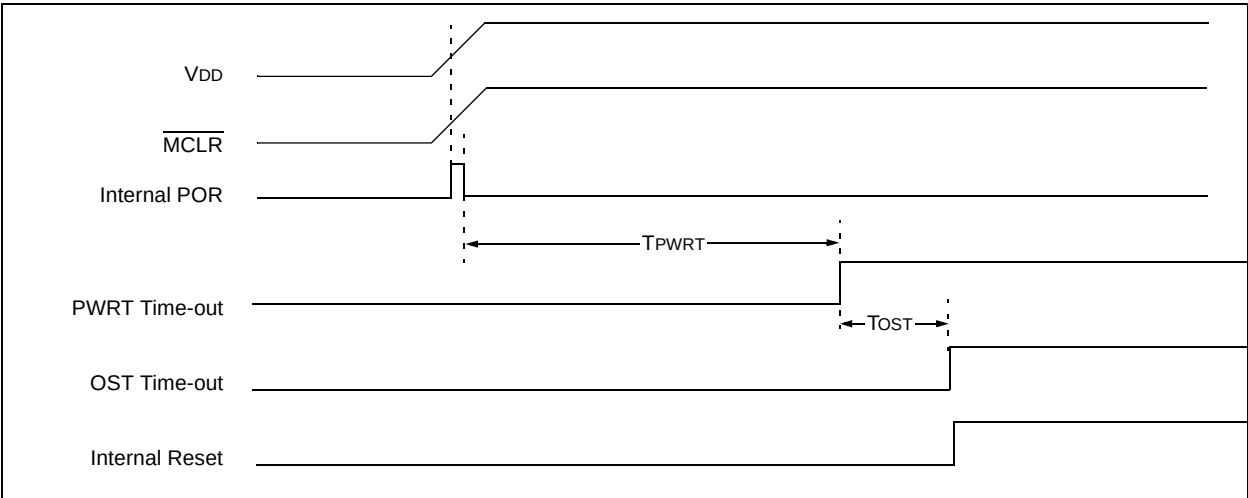


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ WITH VDD)



PIC12F609/615/617/12HV609/615

TABLE 12-5: INITIALIZATION CONDITION FOR REGISTERS (PIC12F615/617/HV615)

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	05h	--x0 x000	--u0 u000	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu ⁽²⁾
PIR1	0Ch	-000 0-00	-000 0-00	-uuu u-uu ⁽²⁾
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2 ⁽¹⁾	11h	0000 0000	0000 0000	uuuu uuuu
T2CON ⁽¹⁾	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L ⁽¹⁾	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H ⁽¹⁾	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON ⁽¹⁾	15h	0-00 0000	0-00 0000	u-uu uuuu
PWM1CON ⁽¹⁾	16h	0000 0000	0000 0000	uuuu uuuu
ECCPAS ⁽¹⁾	17h	0000 0000	0000 0000	uuuu uuuu
VRCON	19h	0-00 0000	0-00 0000	u-uu uuuu
CMCON0	1Ah	0000 -0-0	0000 -0-0	uuuu -u-u
CMCON1	1Ch	---0 0-10	---0 0-10	---u u-qu
ADRESH ⁽¹⁾	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0 ⁽¹⁾	1Fh	00-0 0000	00-0 0000	uu-u uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISIO	85h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	-00- 0-00	-00- 0-00	-uu- u-uu
PCON	8Eh	---- --0x	---- --uu ^(1, 5)	---- --uu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
APFCON	93h	---0 --00	---0 --00	---u --uu
WPU	95h	--11 -111	--11 -111	--uu -uuu
IOC	96h	--00 0000	--00 0000	--uu uuuu
PMCON1 ⁽⁶⁾	98h	---- -000	---- -000	---- -uuu
PMCON2 ⁽⁶⁾	99h	---- ----	---- ----	---- ----
PMADRL ⁽⁶⁾	9Ah	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If V_{DD} goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-6 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

6: For PIC12F617 only.

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12.4 Interrupts

The PIC12F609/615/617/12HV609/615 has 8 sources of interrupt:

- External Interrupt GP2/INT
- Timer0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt (PIC12F615/617/HV615 only)
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt (PIC12F615/617/HV615 only)
- Enhanced CCP Interrupt (PIC12F615/617/HV615 only)
- Flash Memory Self Write (PIC12F617 only)

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- GPIO Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the special register, PIR1. The corresponding interrupt enable bit is contained in special register, PIE1.

The following interrupt flags are contained in the PIR1 register:

- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Enhanced CCP Interrupt

For external interrupt events, such as the INT pin or GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see

Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, Enhanced CCP modules, refer to the respective peripheral section.

12.4.1 GP2/INT INTERRUPT

The external interrupt on the GP2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 12.7 “Power-Down Mode (Sleep)”** for details on Sleep and Figure 12-9 for timing of wake-up from Sleep through GP2/INT interrupt.

Note: The ANSEL register must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0' and cannot generate an interrupt.

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FIGURE 12-8: INT PIN INTERRUPT TIMING

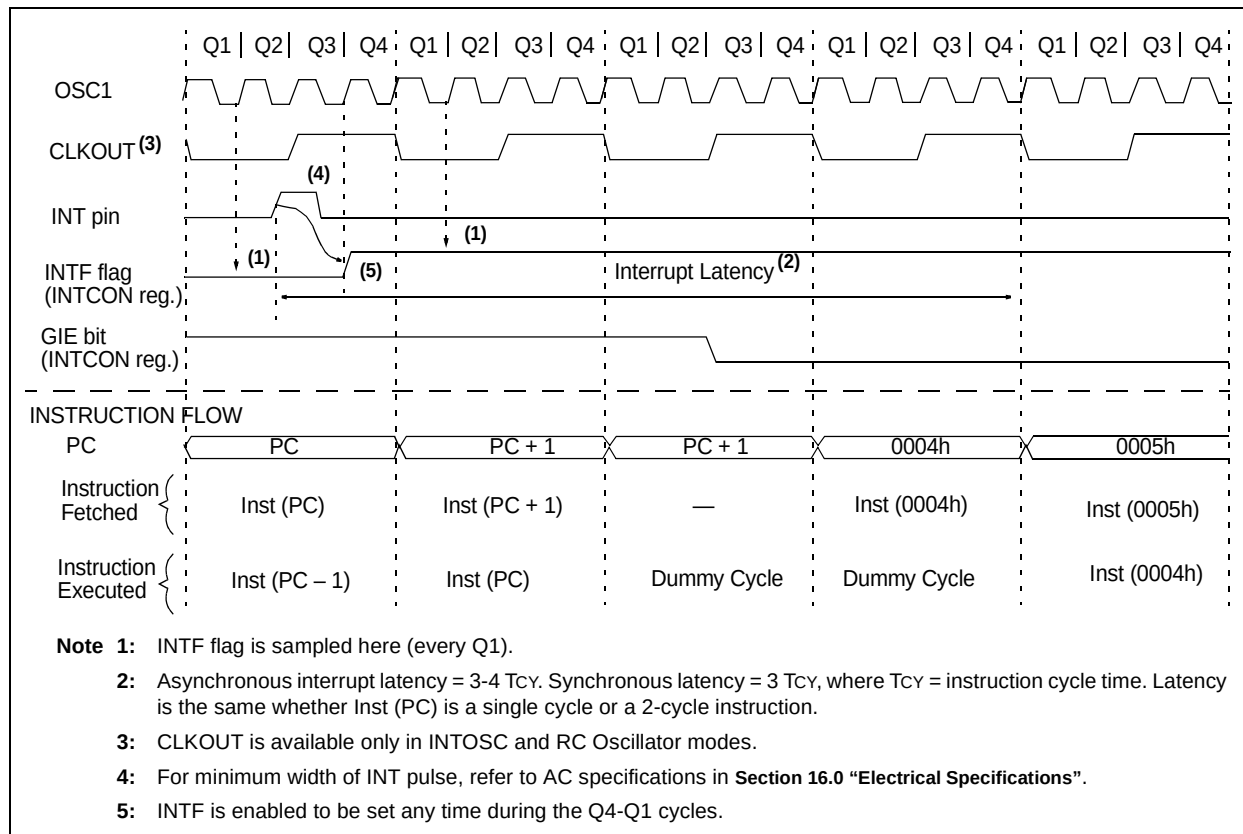


TABLE 12-7: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
PIR1	—	ADIF ⁽¹⁾	CCP1IF ⁽¹⁾	—	CMIF	—	TMR2IF ⁽¹⁾	TMR1IF	-00- 0-00	-000 0-00
PIE1	—	ADIE ⁽¹⁾	CCP1IE ⁽¹⁾	—	CMIE	—	TMR2IE ⁽¹⁾	TMR1IE	-00- 0-00	-000 0-00

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition.
Shaded cells are not used by the interrupt module.

Note 1: PIC12F615/617/HV615 only.

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BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS *f*,*b*
Operands: $0 \leq f \leq 127$
 $0 \leq b < 7$
Operation: skip if (*f*<*b*>) = 1
Status Affected: None
Description: If bit '*b*' in register '*f*' is '0', the next instruction is executed.
 If bit '*b*' is '1', then the next instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT
Operands: None
Operation: 00h → WDT
 0 → WDT prescaler,
 1 → $\overline{TO}$
 1 → $\overline{PD}$
Status Affected: $\overline{TO}$, $\overline{PD}$
Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

CALL **Call Subroutine**

Syntax: [*label*] CALL *k*
Operands: $0 \leq k \leq 2047$
Operation: (PC)+1 → TOS,
 k → PC<10:0>,
 (PCLATH<4:3>) → PC<12:11>
Status Affected: None
Description: Call Subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

COMF **Complement f**

Syntax: [*label*] COMF *f*,*d*
Operands: $0 \leq f \leq 127$
 d ∈ [0,1]
Operation: ($\bar{f}$) → (destination)
Status Affected: Z
Description: The contents of register '*f*' are complemented. If '*d*' is '0', the result is stored in W. If '*d*' is '1', the result is stored back in register '*f*'.

CLRF **Clear f**

Syntax: [*label*] CLRF *f*
Operands: $0 \leq f \leq 127$
Operation: 00h → (*f*)
 1 → Z
Status Affected: Z
Description: The contents of register '*f*' are cleared and the Z bit is set.

DECF **Decrement f**

Syntax: [*label*] DECF *f*,*d*
Operands: $0 \leq f \leq 127$
 d ∈ [0,1]
Operation: (*f*) - 1 → (destination)
Status Affected: Z
Description: Decrement register '*f*'. If '*d*' is '0', the result is stored in the W register. If '*d*' is '1', the result is stored back in register '*f*'.

CLRW **Clear W**

Syntax: [*label*] CLRW
Operands: None
Operation: 00h → (W)
 1 → Z
Status Affected: Z
Description: W register is cleared. Zero bit (Z) is set.

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NOTES:

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TABLE 16-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 5	— —	— —	μs μs	$V_{DD} = 5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $V_{DD} = 5\text{V}$, -40°C to $+125^{\circ}\text{C}$
31*	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	20 20	30 35	ms ms	$V_{DD} = 5\text{V}$, -40°C to $+85^{\circ}\text{C}$ $V_{DD} = 5\text{V}$, -40°C to $+125^{\circ}\text{C}$
32	TOST	Oscillation Start-up Timer Period ^(1, 2)	—	1024	—	TOSC	(NOTE 3)
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	TIOZ	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
35	VBOR	Brown-out Reset Voltage	2.0	2.15	2.3	V	(NOTE 4)
36*	VHYS	Brown-out Reset Hysteresis	—	100	—	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100	—	—	μs	$V_{DD} \leq V_{BOR}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

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FIGURE 17-27: PIC12HV609/615 I_{PD} COMPARATOR (SINGLE ON) vs. V_{DD}

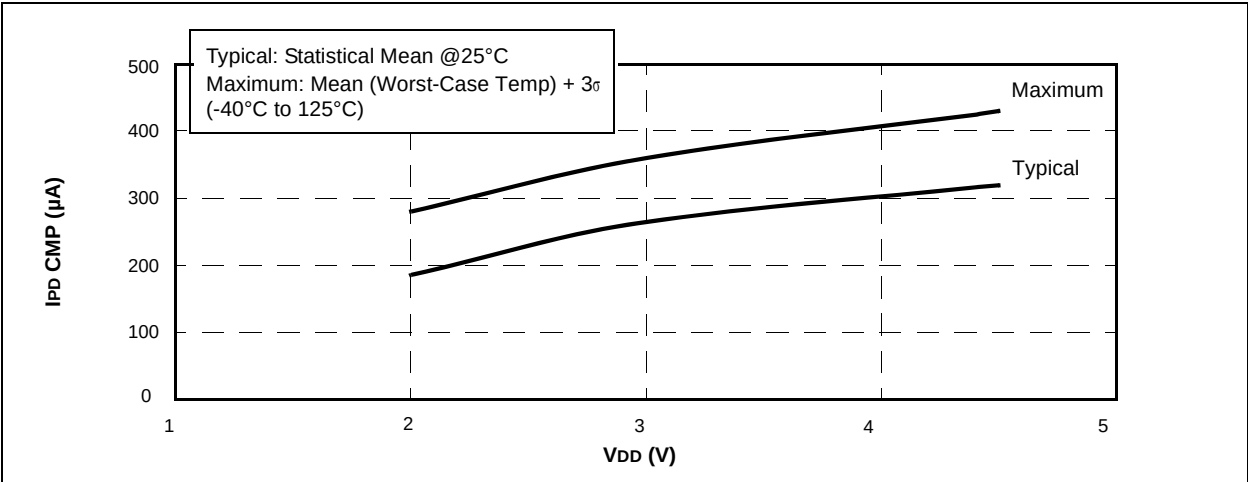


FIGURE 17-28: PIC12HV609/615 I_{PD} WDT vs. V_{DD}

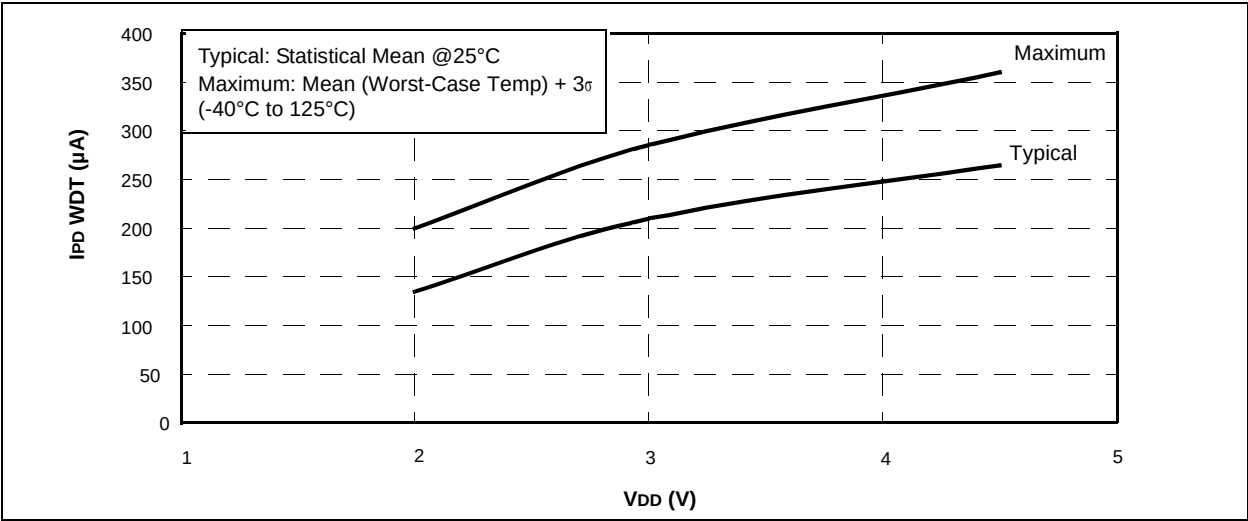
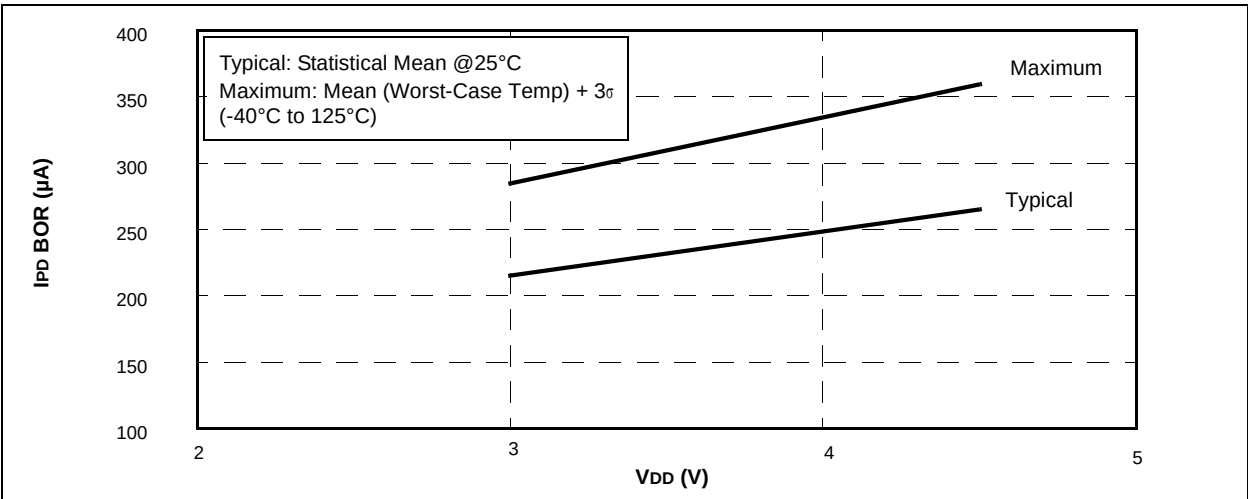


FIGURE 17-29: PIC12HV609/615 I_{PD} BOR vs. V_{DD}



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FIGURE 17-50: SHUNT REGULATOR VOLTAGE vs. TEMP (TYPICAL)

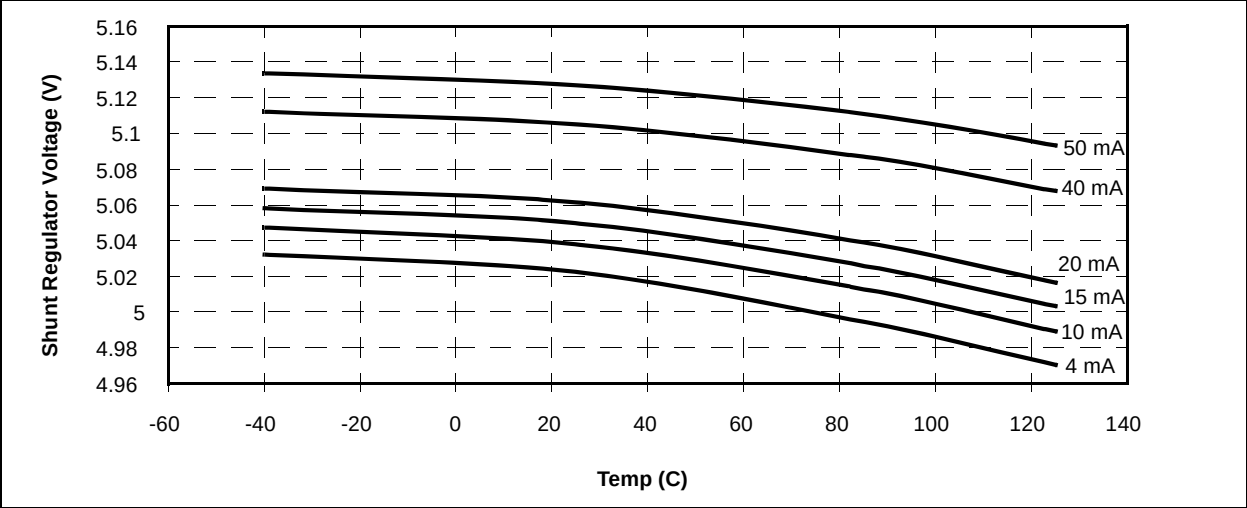


FIGURE 17-51: COMPARATOR RESPONSE TIME (RISING EDGE)

