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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12hv615-i-sn">https://www.e-xfl.com/product-detail/microchip-technology/pic12hv615-i-sn</a>



# MICROCHIP PIC12F609/615/617/12HV609/615

## 8-Pin Flash-Based, 8-Bit CMOS Microcontrollers

### High-Performance RISC CPU:

- Only 35 Instructions to Learn:
  - All single-cycle instructions except branches
- Operating Speed:
  - DC – 20 MHz oscillator/clock input
  - DC – 200 ns instruction cycle
- Interrupt Capability
- 8-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes

### Special Microcontroller Features:

- Precision Internal Oscillator:
  - Factory calibrated to  $\pm 1\%$ , typical
  - Software selectable frequency: 4 MHz or 8 MHz
- Power-Saving Sleep mode
- Voltage Range:
  - PIC12F609/615/617: 2.0V to 5.5V
  - PIC12HV609/615: 2.0V to user defined maximum (**see note**)
- Industrial and Extended Temperature Range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT) with independent Oscillator for Reliable Operation
- Multiplexed Master Clear with Pull-up/Input Pin
- Programmable Code Protection
- High Endurance Flash:
  - 100,000 write Flash endurance
  - Flash retention: > 40 years
- Self Read/ Write Program Memory (PIC12F617 only)

### Low-Power Features:

- Standby Current:
  - 50 nA @ 2.0V, typical
- Operating Current:
  - 11  $\mu$ A @ 32 kHz, 2.0V, typical
  - 260  $\mu$ A @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1  $\mu$ A @ 2.0V, typical

**Note:** Voltage across the shunt regulator should not exceed 5V.

### Peripheral Features:

- Shunt Voltage Regulator (PIC12HV609/615 only):
  - 5 volt regulation
  - 4 mA to 50 mA shunt range
- 5 I/O Pins and 1 Input Only
- High Current Source/Sink for Direct LED Drive
  - Interrupt-on-pin change or pins
  - Individually programmable weak pull-ups
- Analog Comparator module with:
  - One analog comparator
  - Programmable on-chip voltage reference (CVREF) module (% of VDD)
  - Comparator inputs and output externally accessible
  - Built-In Hysteresis (software selectable)
- Timer0: 8-Bit Timer/Counter with 8-Bit Programmable Prescaler
- Enhanced Timer1:
  - 16-bit timer/counter with prescaler
  - External Timer1 Gate (count enable)
  - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
  - Option to use system clock as Timer1
- In-Circuit Serial Programming™ (ICSP™) via Two Pins

### PIC12F615/617/HV615 ONLY:

- Enhanced Capture, Compare, PWM module:
  - 16-bit Capture, max. resolution 12.5 ns
  - Compare, max. resolution 200 ns
  - 10-bit PWM with 1 or 2 output channels, 1 output channel programmable “dead time,” max. frequency 20 kHz, auto-shutdown
- A/D Converter:
  - 10-bit resolution and 4 channels, samples internal voltage references
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler

# PIC12F609/615/617/12HV609/615

## 2.2.2.4 PIE1 Register

The PIE1 register contains the Peripheral Interrupt Enable bits, as shown in Register 2-4.

**Note:** Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

**REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1**

U-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
—	ADIE <sup>(1)</sup>	CCP1IE <sup>(1)</sup>	—	CMIE	—	TMR2IE <sup>(1)</sup>	TMR1IE
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7            **Unimplemented:** Read as '0'
- bit 6            **ADIE:** A/D Converter (ADC) Interrupt Enable bit<sup>(1)</sup>  
                   1 = Enables the ADC interrupt  
                   0 = Disables the ADC interrupt
- bit 5            **CCP1IE:** CCP1 Interrupt Enable bit<sup>(1)</sup>  
                   1 = Enables the CCP1 interrupt  
                   0 = Disables the CCP1 interrupt
- bit 4            **Unimplemented:** Read as '0'
- bit 3            **CMIE:** Comparator Interrupt Enable bit  
                   1 = Enables the Comparator interrupt  
                   0 = Disables the Comparator interrupt
- bit 2            **Unimplemented:** Read as '0'
- bit 1            **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit<sup>(1)</sup>  
                   1 = Enables the Timer2 to PR2 match interrupt  
                   0 = Disables the Timer2 to PR2 match interrupt
- bit 0            **TMR1IE:** Timer1 Overflow Interrupt Enable bit  
                   1 = Enables the Timer1 overflow interrupt  
                   0 = Disables the Timer1 overflow interrupt

**Note 1:** PIC12F615/617/HV615 only. PIC12F609/HV609 unimplemented, read as '0'.

## 3.0 FLASH PROGRAM MEMORY SELF READ/SELF WRITE CONTROL (FOR PIC12F617 ONLY)

The Flash program memory is readable and writable during normal operation (full V<sub>DD</sub> range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 3-1 to 3-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word which holds the 14-bit data for read/write, and the PMADRL and PMADRH registers form a two-byte word which holds the 13-bit address of the Flash location being accessed. These devices have 2K words of program Flash with an address range from 0000h to 07FFh.

The program memory allows single word read and a by four word write. A four word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the Flash program memory.

Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory, however, reads of the program memory are allowed.

When the Flash program memory Code Protection ( $\overline{CP}$ ) bit in the Configuration Word register is enabled, the program memory is code-protected, and the device programmer (ICSP™) cannot access data or program memory.

## 3.1 PMADRH and PMADRL Registers

The PMADRH and PMADRL registers can address up to a maximum of 8K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADRH register and the Least Significant Byte (LSB) is written to the PMADRL register.

## 3.2 PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

PMCON2 is not a physical register. Reading PMCON2 will read all '0's. The PMCON2 register is used exclusively in the Flash memory write sequence.

# PIC12F609/615/617/12HV609/615

## 4.4.1.1 OSCTUNE Register

The oscillator is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 4-1).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

### REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

#### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-5                      **Unimplemented:** Read as '0'

bit 4-0                      **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency

01110 =

•

•

•

00001 =

00000 = Oscillator module is running at the calibrated frequency.

11111 =

•

•

•

10000 = Minimum frequency

**TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets <sup>(1)</sup>
CONFIG <sup>(2)</sup>	IOSCF5	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

**Note 1:** Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

**2:** See Configuration Word register (Register 12-1) for operation of all register bits.

# PIC12F609/615/617/12HV609/615

## 7.6 Timer1 Gate

Timer1 gate source is software configurable to be the  $\overline{T1G}$  pin (or the alternate  $\overline{T1G}$  pin) or the output of the Comparator. This allows the device to directly time external events using  $\overline{T1G}$  or analog events using the Comparator. See the CMCON1 Register (Register 9-2) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**Note:** TMR1GE bit of the T1CON register must be set to use either  $\overline{T1G}$  or COUT as the Timer1 gate source. See Register 9-2 for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the  $\overline{T1G}$  pin or the Comparator output. This configures Timer1 to measure either the active-high or active-low time between events.

## 7.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

**Note:** The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

## 7.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

## 7.9 ECCP Capture/Compare Time Base (PIC12F615/617/HV615 only)

The ECCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see **Section 11.0 “Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC12F615/617/HV615 only)”**.

# PIC12F609/615/617/12HV609/615

**TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
APFCON <sup>(1)</sup>	—	—	—	T1GSEL	—	—	P1BSEL	P1ASEL	---0 --00	---0 --00
CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -0-0	0000 -0-0
CMCON1	—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC	---0 0-10	---0 0-10
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000x
PIE1	—	ADIE <sup>(1)</sup>	CCP1IE <sup>(1)</sup>	—	CMIE	—	TMR2IE <sup>(1)</sup>	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF <sup>(1)</sup>	CCP1IF <sup>(1)</sup>	—	CMIF	—	TMR2IF <sup>(1)</sup>	TMR1IF	-00- 0-00	-00- 0-00
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	0000 0000	uuuu uuuu

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

**Note 1:** PIC12F615/617/HV615 only.

# PIC12F609/615/617/12HV609/615

## 9.8 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See **Section 7.0 “Timer1 Module with Gate Control”** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

## 9.9 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 9-2) and the Timer1 Block Diagram (Figure 7-1) for more information.

**REGISTER 9-2: CMCON1: COMPARATOR CONTROL REGISTER 1**

U-0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0
—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC
bit 7						bit 0	

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7-5      **Unimplemented:** Read as '0'
- bit 4      **T1ACS:** Timer1 Alternate Clock Select bit  
1 = Timer 1 Clock Source is System Clock (FOSC)  
0 = Timer 1 Clock Source is Instruction Clock (FOSC/4)
- bit 3      **CMHYS:** Comparator Hysteresis Select bit  
1 = Comparator Hysteresis enabled  
0 = Comparator Hysteresis disabled
- bit 2      **Unimplemented:** Read as '0'
- bit 1      **T1GSS:** Timer1 Gate Source Select bit<sup>(1)</sup>  
1 = Timer 1 Gate Source is  $\overline{T1G}$  pin (pin should be configured as digital input)  
0 = Timer 1 Gate Source is comparator output
- bit 0      **CMSYNC:** Comparator Output Synchronization bit<sup>(2)</sup>  
1 = Output is synchronized with falling edge of Timer1 clock  
0 = Output is asynchronous

**Note 1:** Refer to **Section 7.6 “Timer1 Gate”**.  
**Note 2:** Refer to Figure 9-2.



# PIC12F609/615/617/12HV609/615

## 11.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

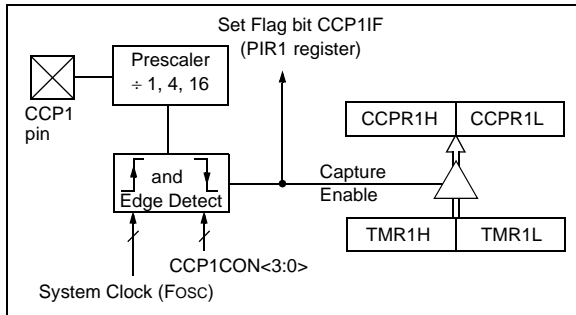
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 11-1).

### 11.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

**Note:** If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.

**FIGURE 11-1: CAPTURE MODE OPERATION BLOCK DIAGRAM**



### 11.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

### 11.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

### 11.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 11-1).

**EXAMPLE 11-1: CHANGING BETWEEN CAPTURE PRESCALERS**

```
BANKSEL CCP1CON    ;Set Bank bits to point
                   ;to CCP1CON
CLRF    CCP1CON    ;Turn CCP module off
MOVLW  NEW_CAPT_PS ;Load the W reg with
                   ; the new prescaler
MOVWF  CCP1CON    ; move value and CCP ON
MOVWF  CCP1CON    ;Load CCP1CON with this
                   ; value
```

# PIC12F609/615/617/12HV609/615

## 11.2 Compare Mode

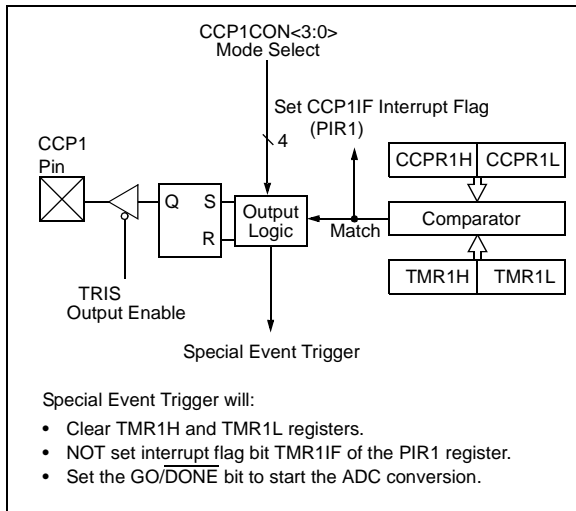
In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

- Toggle the CCP1 output.
- Set the CCP1 output.
- Clear the CCP1 output.
- Generate a Special Event Trigger.
- Generate a Software Interrupt.

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register.

All Compare modes can generate an interrupt.

**FIGURE 11-2: COMPARE MODE OPERATION BLOCK DIAGRAM**



### 11.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

**Note:** Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the PORT I/O data latch.

### 11.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

### 11.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

### 11.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (see the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

**Note 1:** The Special Event Trigger from the CCP module does not set interrupt flag bit TMRxIF of the PIR1 register.

- 2: Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

# PIC12F609/615/617/12HV609/615

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## 11.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

## 11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 4.0 “Oscillator Module”** for additional details.

## 11.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

## 11.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and DC1B bits of the CCP1CON register.
5. Configure and start Timer2:
  - Clear the TMR2IF interrupt flag bit of the PIR1 register.
  - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
  - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
  - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
  - Enable the CCP1 pin output driver by clearing the associated TRIS bit.

# PIC12F609/615/617/12HV609/615

**TABLE 12-5: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)(PIC12F615/617/HV615)**

Register	Address	Power-on Reset	MCLR Reset WDT Reset (Continued) Brown-out Reset <sup>(1)</sup>	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out (Continued)
PMADRH <sup>(6)</sup>	9Bh	---- -000	---- -000	---- -uuu
PMDATL <sup>(6)</sup>	9Ch	0000 0000	0000 0000	uuuu uuuu
PMDATH <sup>(6)</sup>	9Dh	--00 0000	--00 0000	--uu uuuu
ADRESL <sup>(1)</sup>	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ANSEL	9Fh	-000 1111	-000 1111	-uuu qqqq

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

**Note 1:** If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

**2:** One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

**3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**4:** See Table 12-6 for Reset value for specific condition.

**5:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

**6:** For PIC12F617 only.

**TABLE 12-6: INITIALIZATION CONDITION FOR SPECIAL REGISTERS**

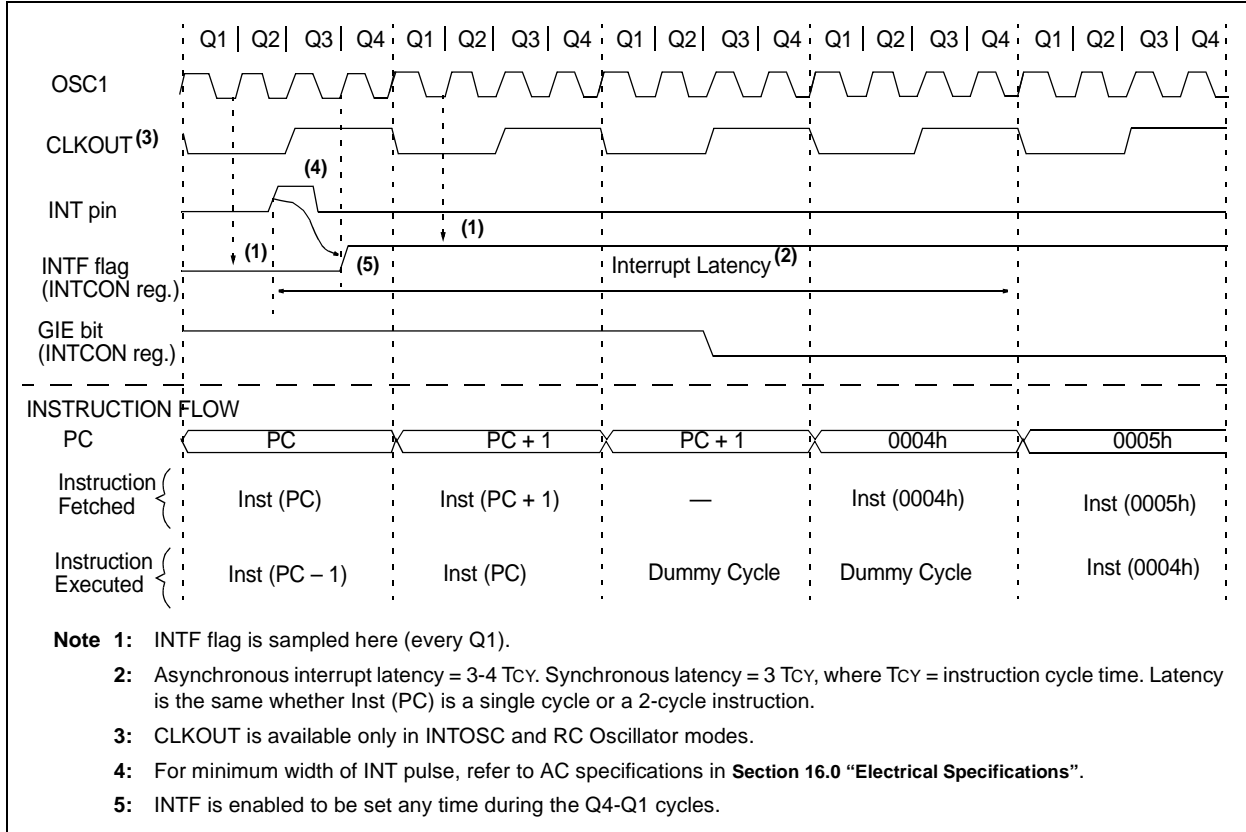
Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
MCLR Reset during normal operation	000h	000u uuuu	---- --uu
MCLR Reset during Sleep	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --10
Interrupt Wake-up from Sleep	PC + 1 <sup>(1)</sup>	uuu1 0uuu	---- --uu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

# PIC12F609/615/617/12HV609/615

**FIGURE 12-8: INT PIN INTERRUPT TIMING**



**TABLE 12-7: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
PIR1	—	ADIF <sup>(1)</sup>	CCP1IF <sup>(1)</sup>	—	CMIF	—	TMR2IF <sup>(1)</sup>	TMR1IF	-00- 0-00	-000 0-00
PIE1	—	ADIE <sup>(1)</sup>	CCP1IE <sup>(1)</sup>	—	CMIE	—	TMR2IE <sup>(1)</sup>	TMR1IE	-00- 0-00	-000 0-00

**Legend:** x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the interrupt module.

**Note 1:** PIC12F615/617/HV615 only.

## 12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W\_TEMP and STATUS\_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-3). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 12-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

**Note:** The PIC12F609/615/617/12HV609/615 does not require saving the PCLATH. However, if computed GOTOS are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

### EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF  W_TEMP           ;Copy W to TEMP register
SWAPF  STATUS,W         ;Swap status to be saved into W
                           ;Swaps are used because they do not affect the status bits
MOVWF  STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                   ;Insert user code here
:
SWAPF  STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                           ;(sets bank to original state)
MOVWF  STATUS           ;Move W into STATUS register
SWAPF  W_TEMP,F         ;Swap W_TEMP
SWAPF  W_TEMP,W         ;Swap W_TEMP into W
```

## 12.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time out generates a device Reset. If the device is in Sleep mode, a WDT time out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (**Section 12.1 “Configuration Bits”**).

### 12.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The  $\overline{TO}$  bit in the STATUS register will be cleared upon a Watchdog Timer time out.

# PIC12F609/615/617/12HV609/615

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## 15.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

## 15.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

## 15.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

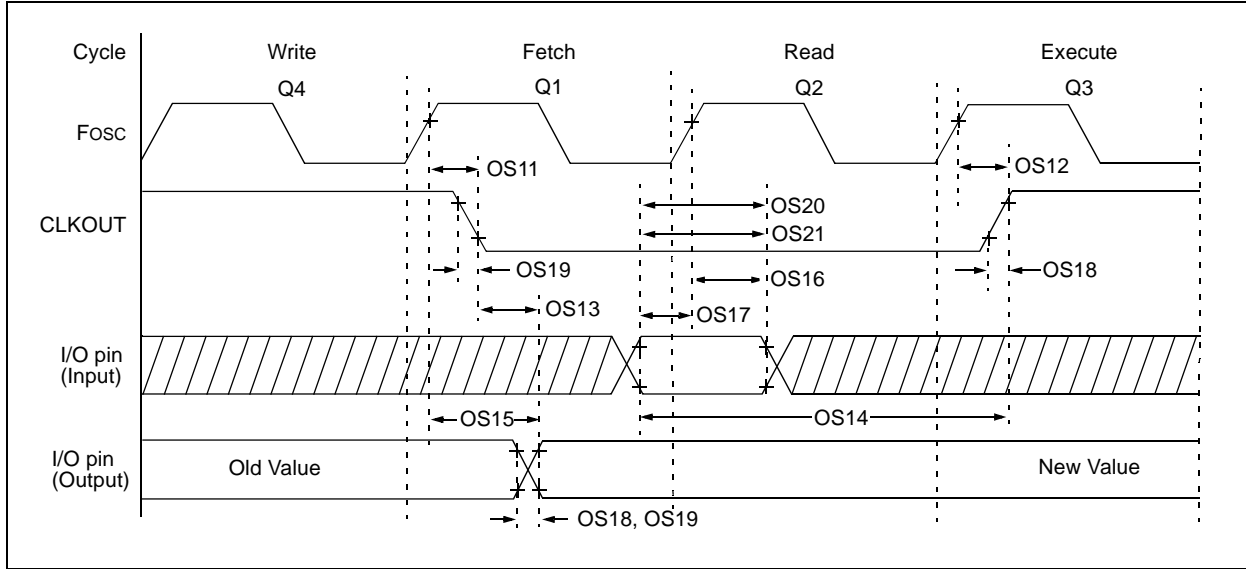
In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

# PIC12F609/615/617/12HV609/615

**FIGURE 16-5: CLKOUT AND I/O TIMING**



**TABLE 16-3: CLKOUT AND I/O TIMING PARAMETERS**

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS11	TosH2ckL	Fosc $\uparrow$ to CLKOUT $\downarrow$ <sup>(1)</sup>	—	—	70	ns	VDD = 5.0V
OS12	TosH2ckH	Fosc $\uparrow$ to CLKOUT $\uparrow$ <sup>(1)</sup>	—	—	72	ns	VDD = 5.0V
OS13	TckL2ioV	CLKOUT $\downarrow$ to Port out valid <sup>(1)</sup>	—	—	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT $\uparrow$ <sup>(1)</sup>	Tosc + 200 ns	—	—	ns	
OS15	TosH2ioV	Fosc $\uparrow$ (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 5.0V
OS16	TosH2ioI	Fosc $\uparrow$ (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 5.0V
OS17	TioV2osH	Port input valid to Fosc $\uparrow$ (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TioR	Port output rise time <sup>(2)</sup>	—	15 40	72 32	ns	VDD = 2.0V VDD = 5.0V
OS19	TioF	Port output fall time <sup>(2)</sup>	—	28 15	55 30	ns	VDD = 2.0V VDD = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TRAP	GPIO interrupt-on-change new input level time	Tcy	—	—	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated.

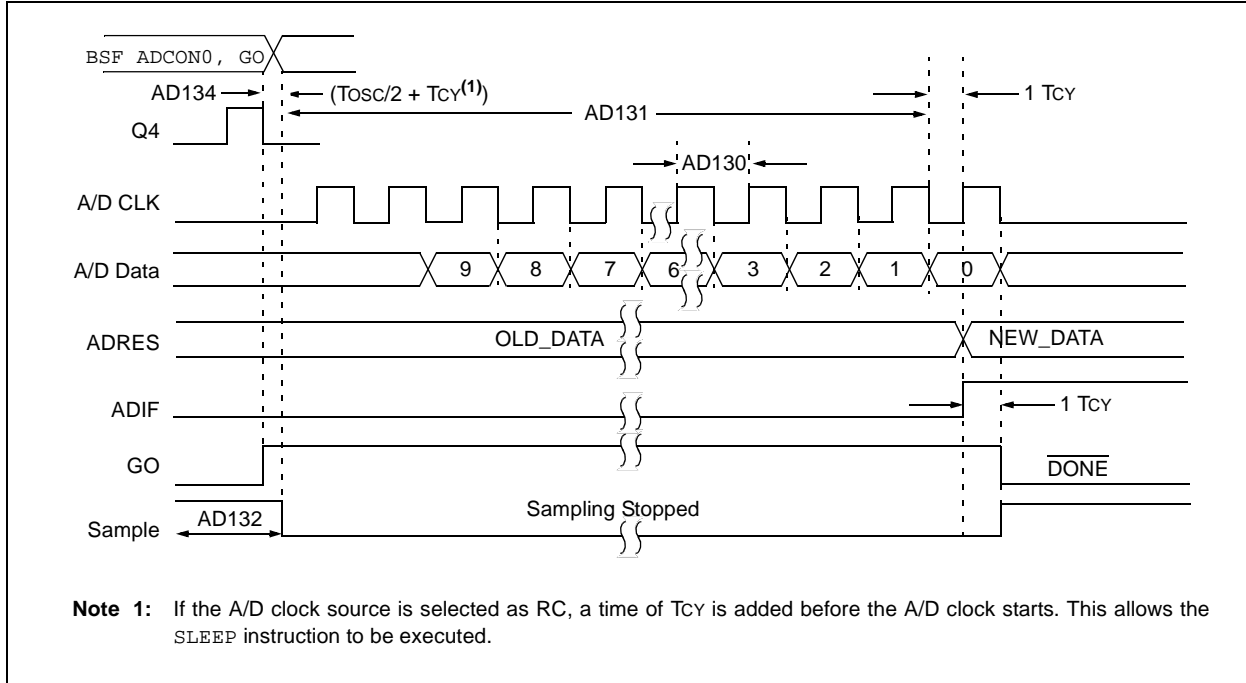
**Note 1:** Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

**Note 2:** Includes OSC2 in CLKOUT mode.



# PIC12F609/615/617/12HV609/615

**FIGURE 16-11: PIC12F615/617/HV615 A/D CONVERSION TIMING (SLEEP MODE)**



# PIC12F609/615/617/12HV609/615

FIGURE 17-35:  $V_{OL}$  vs.  $I_{OL}$  OVER TEMPERATURE ( $V_{DD} = 5.0V$ )

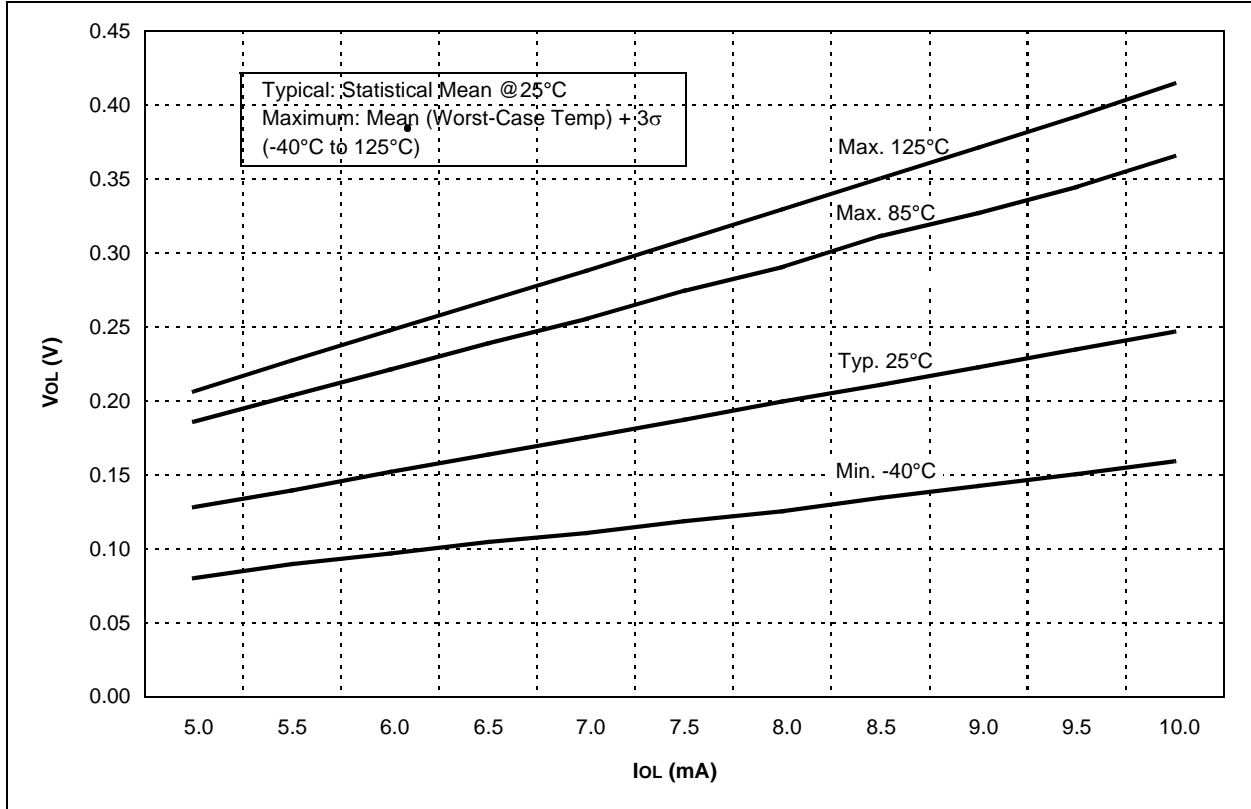
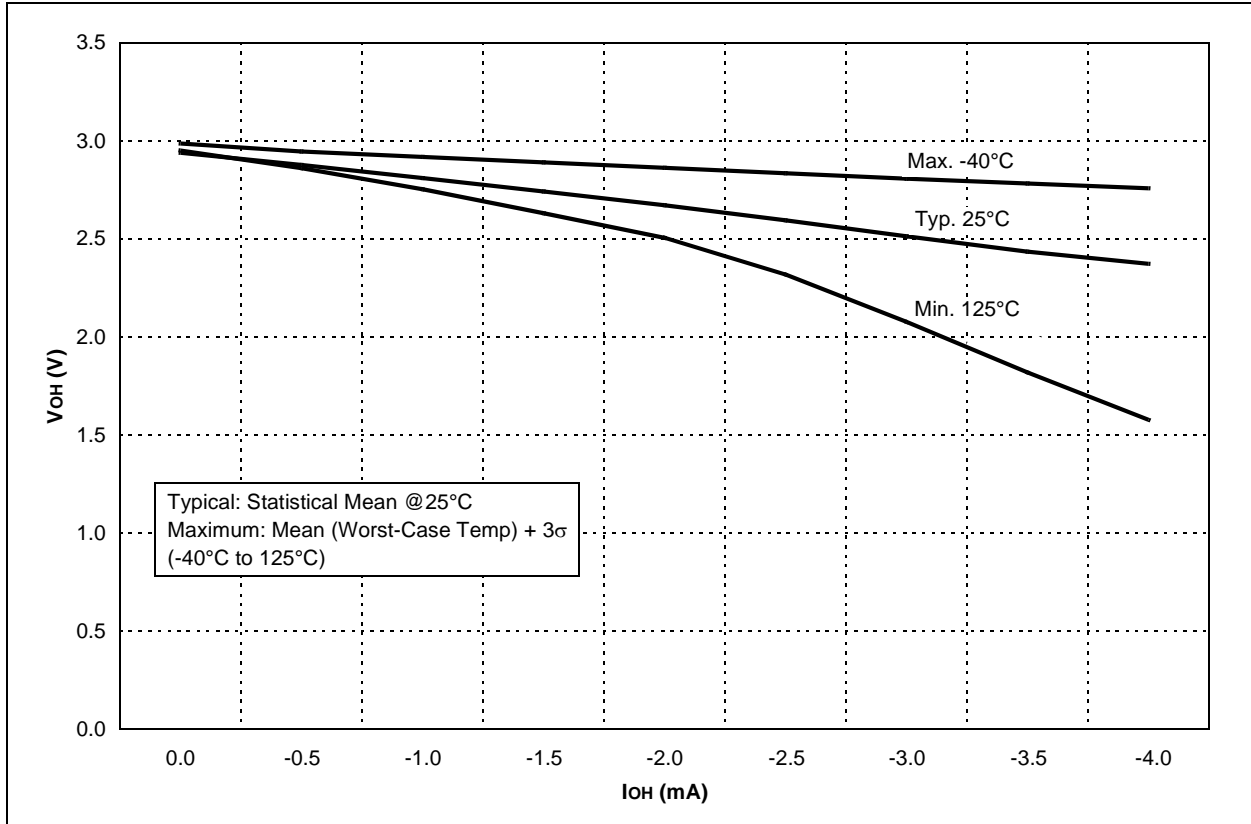


FIGURE 17-36:  $V_{OH}$  vs.  $I_{OH}$  OVER TEMPERATURE ( $V_{DD} = 3.0V$ )



# PIC12F609/615/617/12HV609/615

FIGURE 17-37:  $V_{OH}$  vs.  $I_{OH}$  OVER TEMPERATURE ( $V_{DD} = 5.0V$ )

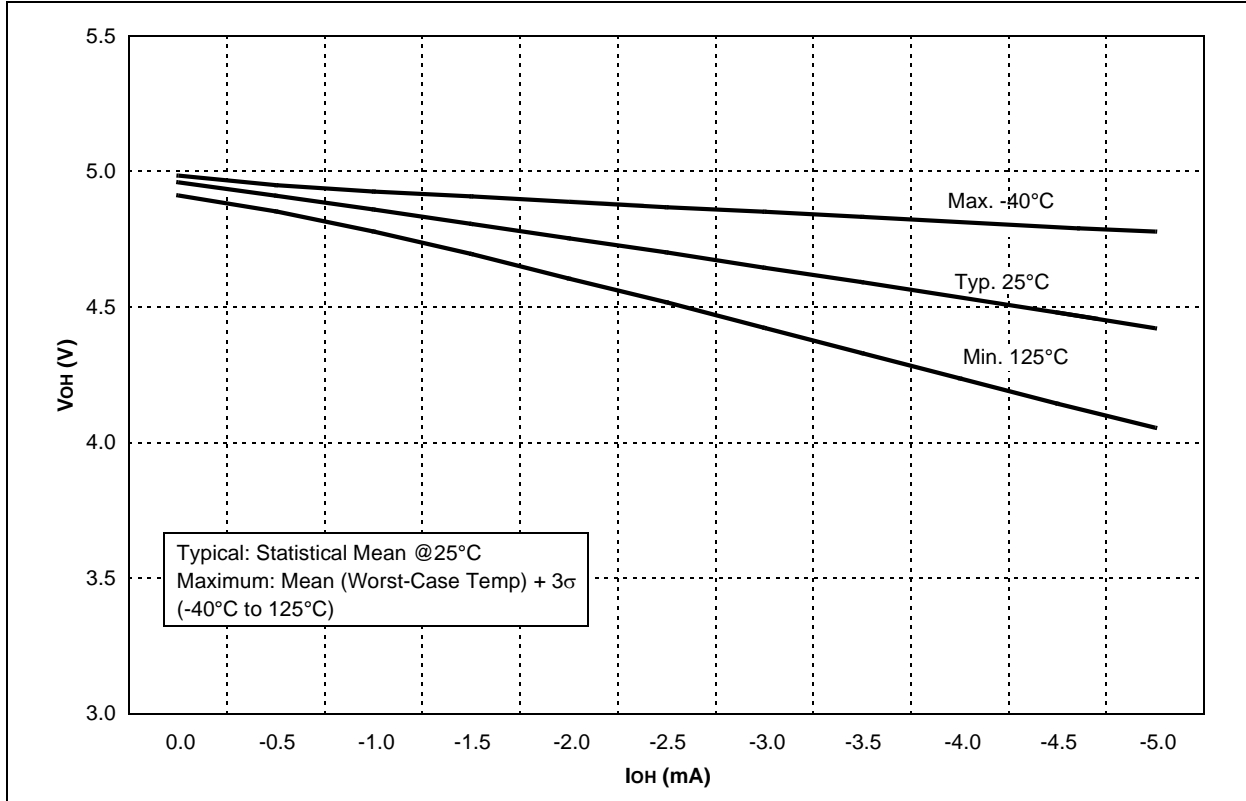
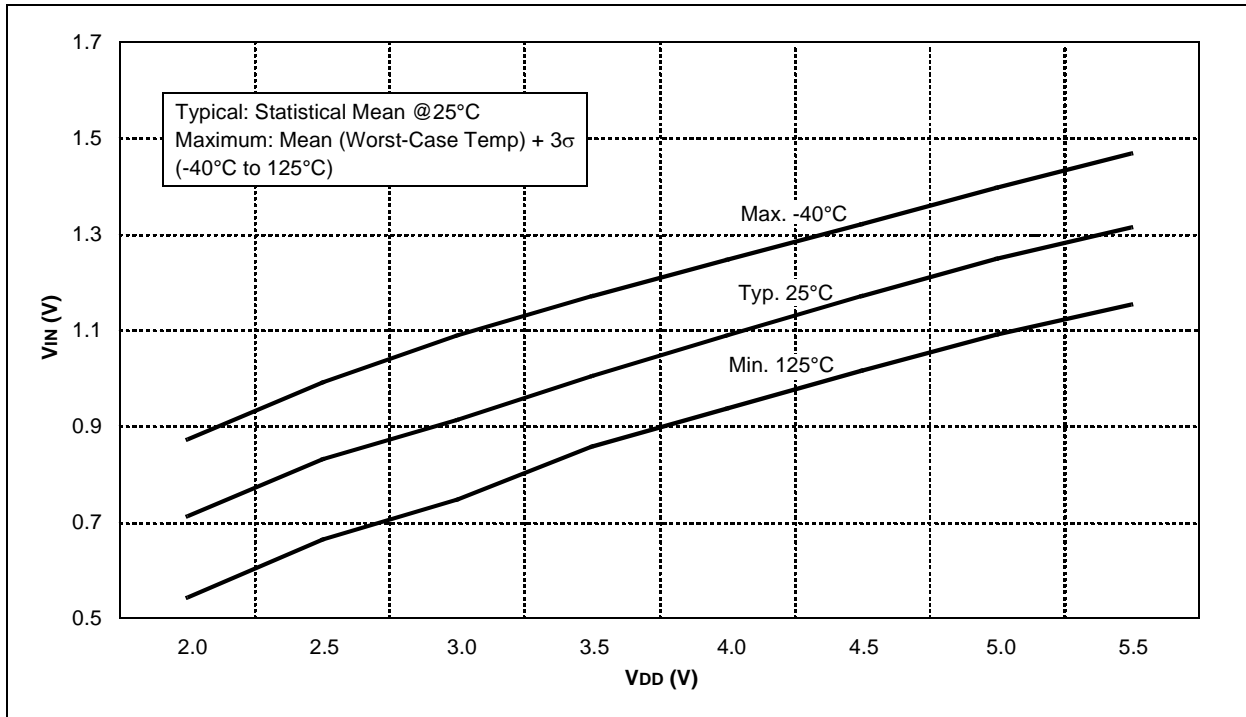


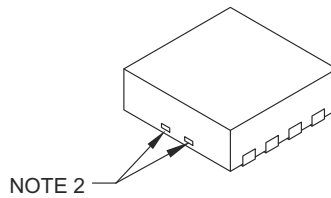
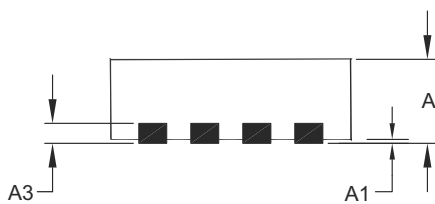
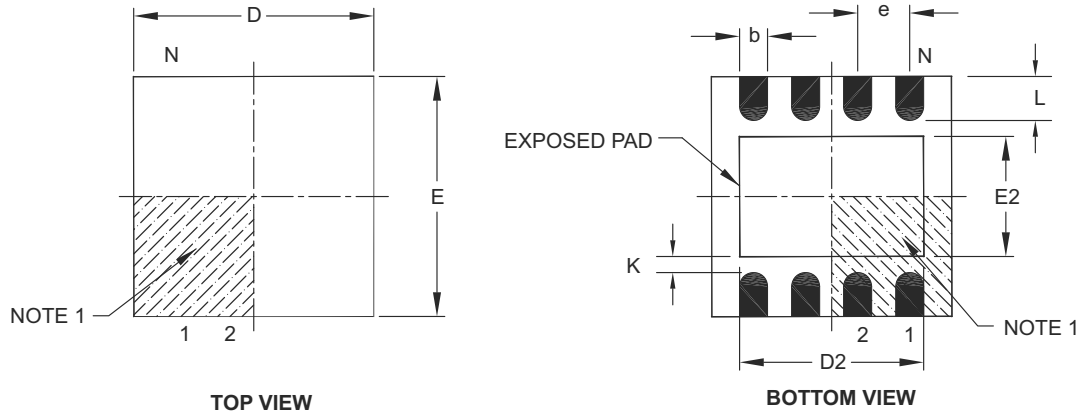
FIGURE 17-38: TTL INPUT THRESHOLD  $V_{IN}$  vs.  $V_{DD}$  OVER TEMPERATURE



# PIC12F609/615/617/12HV609/615

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Width	E2	0.00	–	1.60
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	0.00	–	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

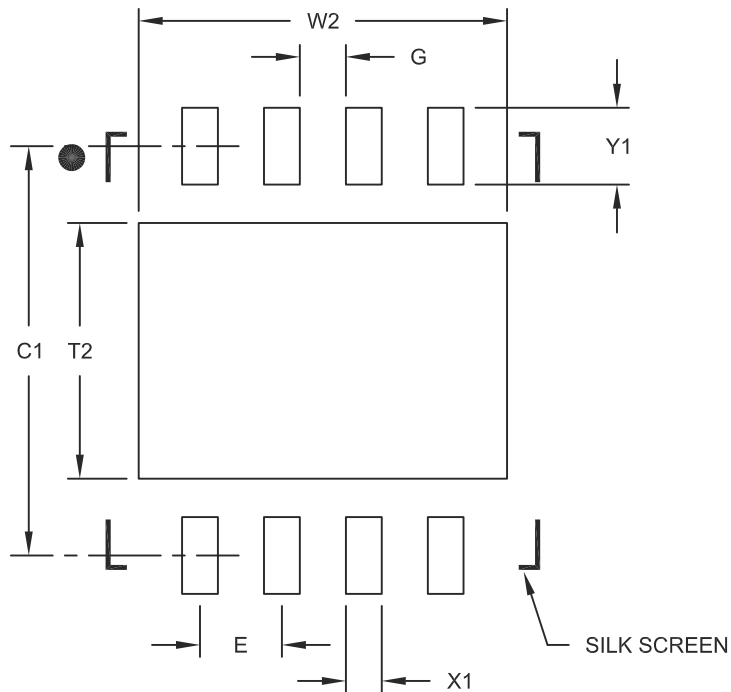
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-062B

# PIC12F609/615/617/12HV609/615

## 8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131B