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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12hv615t-i-ms

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

Note:	Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** GP2/INT External Interrupt Enable bit
1 = Enables the GP2/INT external interrupt
0 = Disables the GP2/INT external interrupt

bit 3 **GPIE:** GPIO Change Interrupt Enable bit(1)
1 = Enables the GPIO change interrupt
0 = Disables the GPIO change interrupt

bit 2 **T0IF:** Timer0 Overflow Interrupt Flag bit(2)
1 = Timer0 register has overflowed (must be cleared in software)
0 = Timer0 register did not overflow

bit 1 **INTF:** GP2/INT External Interrupt Flag bit
1 = The GP2/INT external interrupt occurred (must be cleared in software)
0 = The GP2/INT external interrupt did not occur

bit 0 **GPIF:** GPIO Change Interrupt Flag bit
1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software)
0 = None of the GPIO <5:0> pins have changed state

Note 1: IOC register must also be enabled.
2: T0IF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing T0IF bit.

3.0 FLASH PROGRAM MEMORY SELF READ/SELF WRITE CONTROL (FOR PIC12F617 ONLY)

The Flash program memory is readable and writable during normal operation (full V_{DD} range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (see Registers 3-1 to 3-5). There are six SFRs used to read and write this memory:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When interfacing the program memory block, the PMDATL and PMDATH registers form a two-byte word which holds the 14-bit data for read/write, and the PMADRL and PMADRH registers form a two-byte word which holds the 13-bit address of the Flash location being accessed. These devices have 2K words of program Flash with an address range from 0000h to 07FFh.

The program memory allows single word read and a by four word write. A four word write automatically erases the row of the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the Flash program memory.

Depending on the settings of the Flash Program Memory Enable (WRT<1:0>) bits, the device may or may not be able to write certain blocks of the program memory, however, reads of the program memory are allowed.

When the Flash program memory Code Protection ($\overline{CP}$) bit in the Configuration Word register is enabled, the program memory is code-protected, and the device programmer (ICSP™) cannot access data or program memory.

3.1 PMADRH and PMADRL Registers

The PMADRH and PMADRL registers can address up to a maximum of 8K words of program memory.

When selecting a program address value, the Most Significant Byte (MSB) of the address is written to the PMADRH register and the Least Significant Byte (LSB) is written to the PMADRL register.

3.2 PMCON1 and PMCON2 Registers

PMCON1 is the control register for the data program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear.

PMCON2 is not a physical register. Reading PMCON2 will read all '0's. The PMCON2 register is used exclusively in the Flash memory write sequence.

4.0 OSCILLATOR MODULE

4.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 4-1 illustrates a block diagram of the Oscillator module.

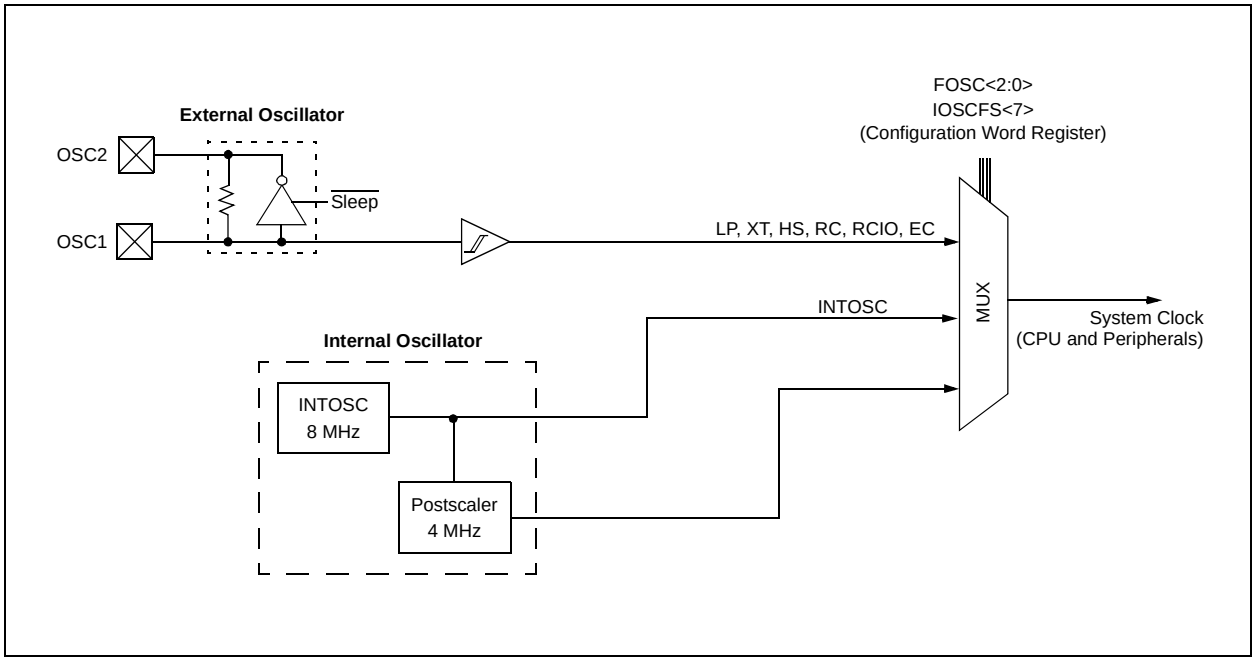
Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured with a choice of two selectable speeds: internal or external system clock source.

The Oscillator module can be configured in one of eight clock modes.

3. EC – External clock with I/O on OSC2/CLKOUT.
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
6. HS – High Gain Crystal or Ceramic Resonator mode.
7. RC – External Resistor-Capacitor (RC) with FOSC/4 output on OSC2/CLKOUT.
8. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
9. INTOSC – Internal oscillator with FOSC/4 output on OSC2 and I/O on OSC1/CLKIN.
10. INTOSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The Internal Oscillator module provides a selectable system clock mode of either 4 MHz (Postscaler) or 8 MHz (INTOSC).

FIGURE 4-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



NOTES:

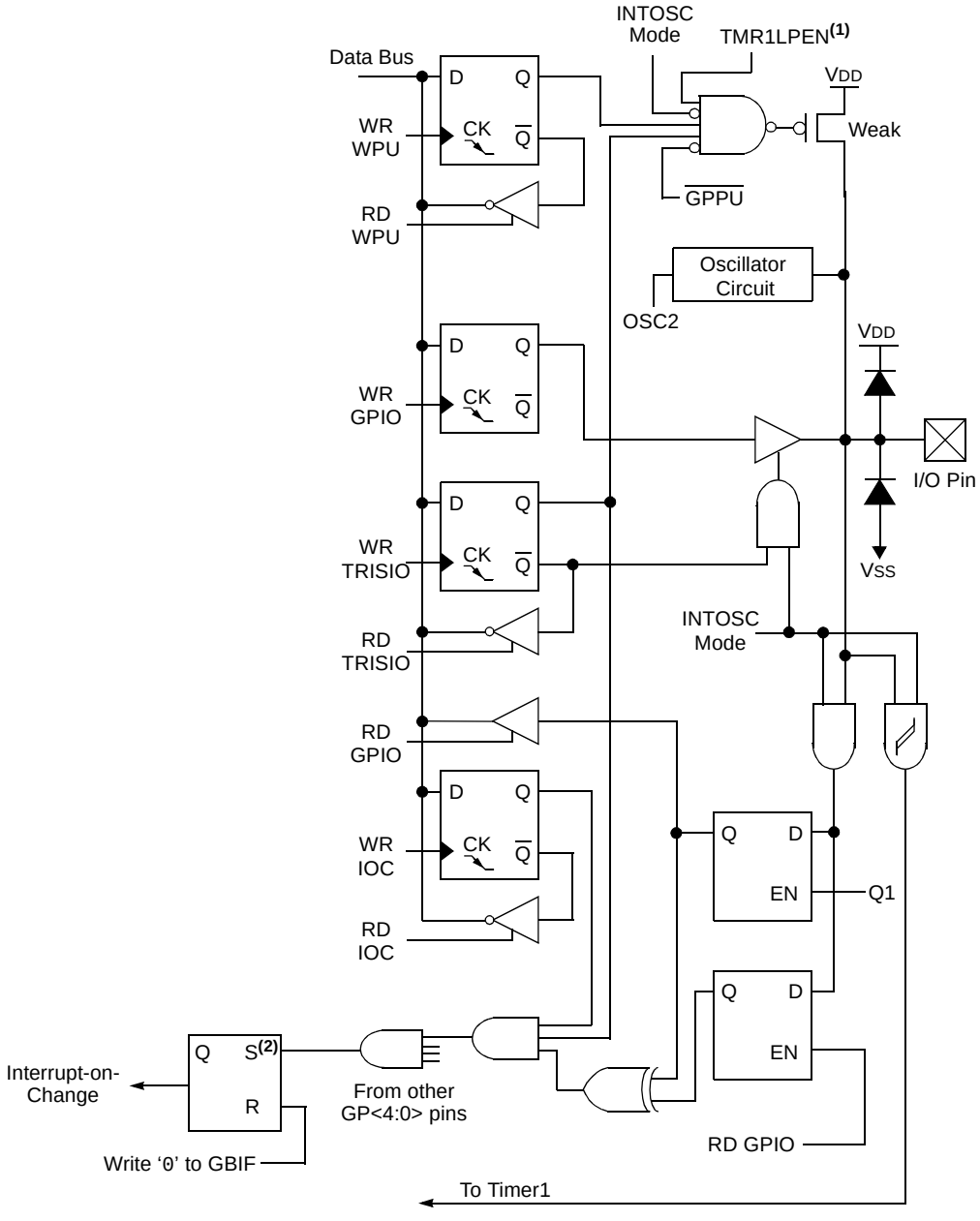
5.2.4.6 GP5/T1CKI/P1A(1, 2)/OSC1/CLKIN

Figure 5-5 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- PWM output, alternate pin(1, 2)
- a crystal/resonator connection
- a clock input

Note 1: Alternate pin function.
2: PIC12F615/617/HV615 only.

FIGURE 5-5: BLOCK DIAGRAM OF GP5



Note 1: Timer1 LP Oscillator enabled.
2: Set has priority over Reset.

9.2 Analog Input Connection Considerations

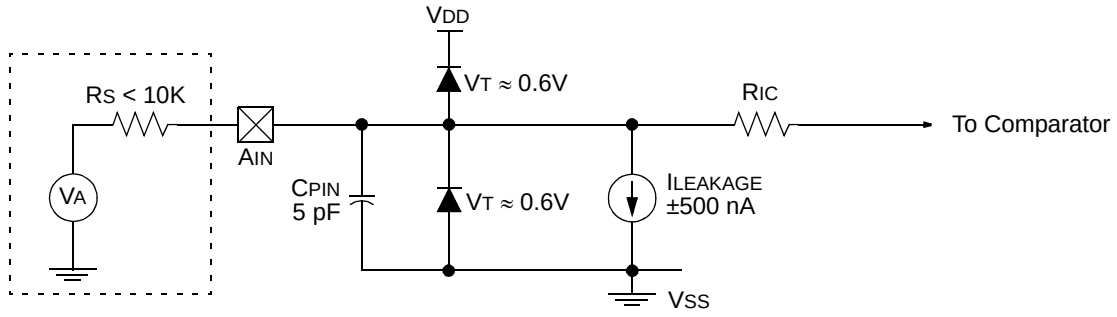
A simplified circuit for an analog input is shown in Figure 9-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a GPIO register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

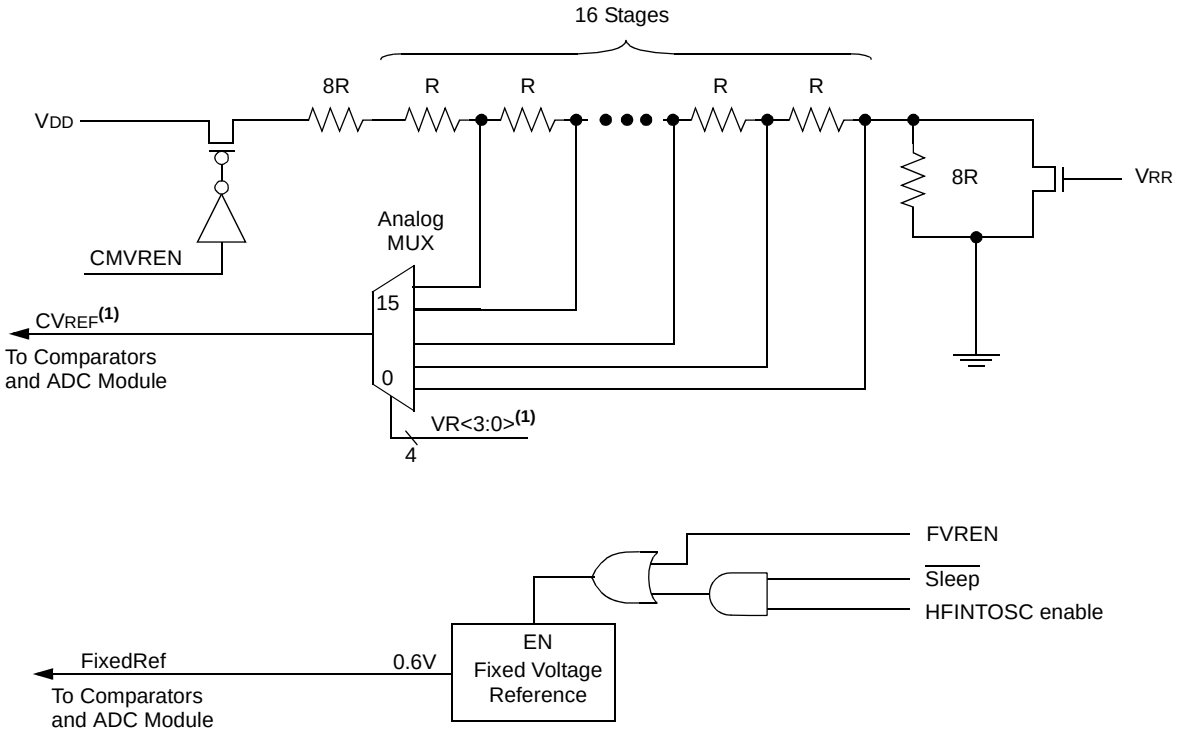
2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 9-3: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

FIGURE 9-6: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



Note 1: Care should be taken to ensure CV_{REF} remains within the comparator common mode input range. See **Section 16.0 "Electrical Specifications"** for more detail.

TABLE 9-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2(1)	ADCS1(1)	ADCS0(1)	ANS3	ANS2(1)	ANS1	ANS0	-000 1111	-000 1111
CMCON0	CMON	COUT	CMOE	CMPOL	—	CMR	—	CMCH	0000 -000	0000 -000
CMCON1	—	—	—	T1ACS	CMHYS	—	T1GSS	CMSYNC	0000 0000	0000 0000
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000x
PIE1	—	ADIE(1)	CCP1IE(1)	—	CMIE	—	TMR2IE(1)	TMR1IE	-00- 0-00	-00- 0-00
PIR1	—	ADIF(1)	CCP1IF(1)	—	CMIF	—	TMR2IF(1)	TMR1IF	-00- 0-00	-00- 0-00
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
VRCON	CMVREN	—	VRR	FVREN	VR3	VR2	VR1	VR0	0-00 0000	0-00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

Note 1: For PIC12F615/617/HV615 only.

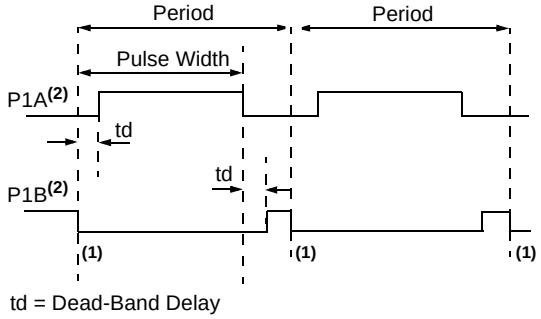
11.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCP1/P1A pin, while the complementary PWM output signal is output on the P1B pin (see Figure 11-8). This mode can be used for Half-Bridge applications, as shown in Figure 11-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWM1CON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 11.4.6 "Programmable Dead-Band Delay mode"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure P1A and P1B as outputs.

FIGURE 11-8: EXAMPLE OF HALF-BRIDGE PWM OUTPUT

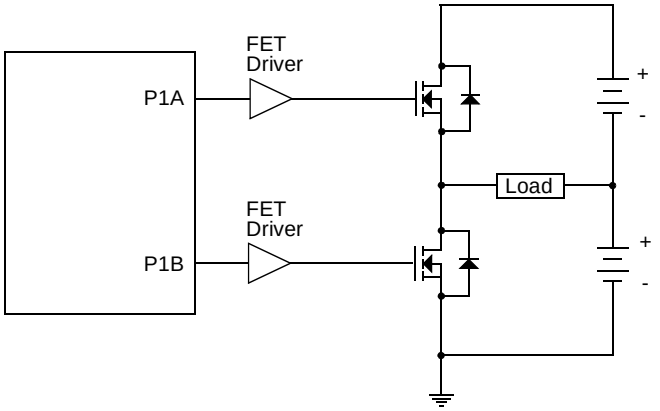


Note 1: At this time, the TMR2 register is equal to the PR2 register.

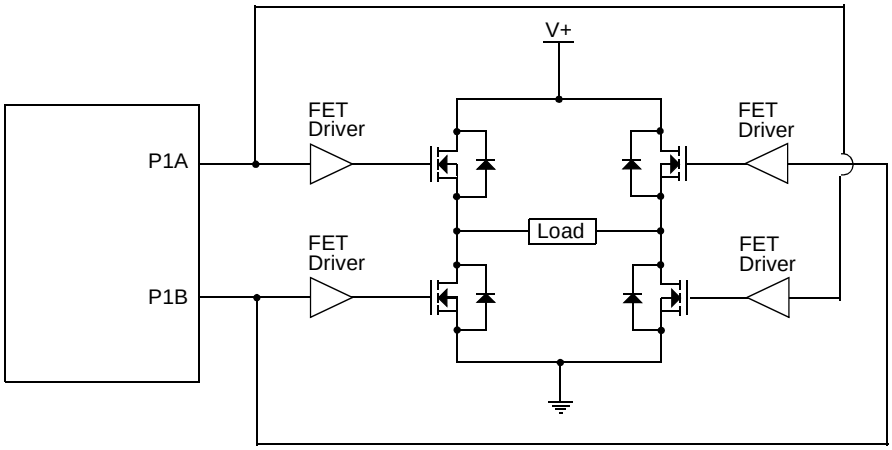
2: Output signals are shown as active-high.

FIGURE 11-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS

Standard Half-Bridge Circuit ("Push-Pull")



Half-Bridge Output Driving a Full-Bridge Circuit



12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Temporary holding registers W_TEMP and STATUS_TEMP should be placed in the last 16 bytes of GPR (see Figure 2-3). These 16 locations are common to all banks and do not require banking. This makes context save and restore operations simpler. The code shown in Example 12-1 can be used to:

- Store the W register
- Store the STATUS register
- Execute the ISR code
- Restore the Status (and Bank Select Bit register)
- Restore the W register

Note:	The PIC12F609/615/617/12HV609/615 does not require saving the PCLATH. However, if computed GOTOs are used in both the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF   W_TEMP              ;Copy W to TEMP register
SWAPF   STATUS,W            ;Swap status to be saved into W
                            ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP         ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                      ;Insert user code here
:
SWAPF   STATUS_TEMP,W       ;Swap STATUS_TEMP register into W
                            ;(sets bank to original state)
MOVWF   STATUS              ;Move W into STATUS register
SWAPF   W_TEMP,F            ;Swap W_TEMP
SWAPF   W_TEMP,W            ;Swap W_TEMP into W
```

12.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time out generates a device Reset. If the device is in Sleep mode, a WDT time out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the Configuration bit, WDTE, as clear (**Section 12.1 “Configuration Bits”**).

12.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device Reset.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time out.

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Description: The contents of register 'f' is moved to a destination dependent upon the status of 'd'. If d = 0, destination is W register. If d = 1, the destination is file register 'f' itself. d = 1 is useful to test a file register since Status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR, 0
```
After Instruction
W = value in FSR register
Z = 1

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 127$

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVW    OPTION
F
```
Before Instruction
OPTION = 0xFF
W = 0x4F
After Instruction
OPTION = 0x4F
W = 0x4F

MOVLW **Move literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Description: The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

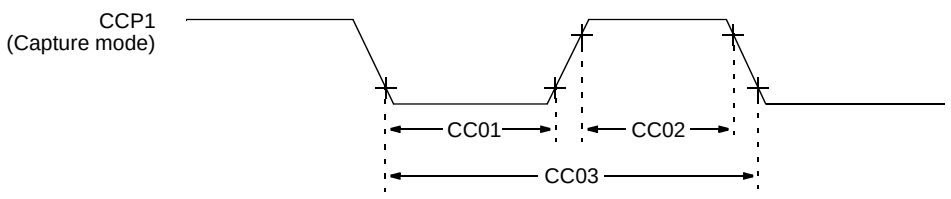
Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```

FIGURE 16-9: PIC12F615/617/HV615 CAPTURE/COMPARE/PWM TIMINGS (ECCP)



Note: Refer to Figure 16-3 for load conditions.

TABLE 16-6: PIC12F615/617/HV615 CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
CC01*	TccL	CCP1 Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		3TCY + 40 N	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 16-7: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	**Sym**	**Characteristics**		**Min**	**Typ†**	**Max**	**Units**	**Comments**
CM01	VOS	Input Offset Voltage(2)		—	± 5.0	± 10	mV	
CM02	VCM	Input Common Mode Voltage		0	—	VDD – 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	TRT	Response Time(1)	Falling	—	150	600	ns	
			Rising	—	200	1000	ns	
CM05*	TMC2COV	Comparator Mode Change to Output Valid		—	—	10	µs	
CM06*	VHYS	Input Hysteresis Voltage		—	45	60	mV	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV. The other input is at (VDD -1.5)/2.

2: Input offset voltage is measured with one comparator input at (VDD - 1.5V)/2.

TABLE 16-12: PIC12F615/617/HV615 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
AD130*	TAD	A/D Clock Period	1.6	—	9.0	µs	TOSC-based, VREF ≥ 3.0V
			3.0	—	9.0	µs	TOSC-based, VREF full range(3)
		A/D Internal RC Oscillator Period					ADCS<1:0> = 11 (ADRC mode)
			3.0	6.0	9.0	µs	At VDD = 2.5V
			1.6	4.0	6.0	µs	At VDD = 5.0V
AD131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO/$\overline{\text{DONE}}$ bit to new data in A/D Result register
AD132*	TACQ	Acquisition Time		11.5	—	µs	
AD133*	TAMP	Amplifier Settling Time	—	—	5	µs	
AD134	TGO	Q4 to A/D Clock Start	—	TOSC/2	—	—	
			—	TOSC/2 + TCY	—	—	If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

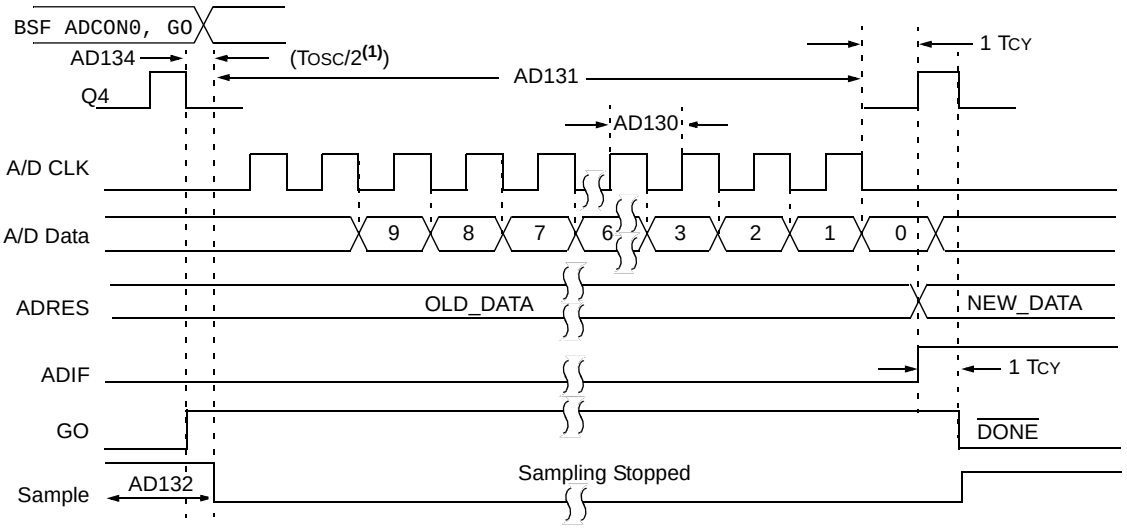
† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following TCY cycle.

2: See **Section 10.3 "A/D Acquisition Requirements"** for minimum conditions.

3: Full range for PIC12HV609/HV615 powered by the shunt regulator is the 5V regulated voltage.

FIGURE 16-10: PIC12F615/617/HV615 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

16.12 High Temperature Operation

This section outlines the specifications for the PIC12F615 device operating in a temperature range between -40°C and 150°C.(4) The specifications between -40°C and 150°C(4) are identical to those shown in DS41288 and DS80329.

Note 1: Writes are **not allowed** for Flash Program Memory above 125°C.

2: All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.

3: The temperature range indicator in the part number is "H" for -40°C to 150°C.(4)

Example: PIC12F615T-H/ST indicates the device is shipped in a TAPE and reel configuration, in the MSOP package, and is rated for operation from -40°C to 150°C.(4)

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

TABLE 16-13: ABSOLUTE MAXIMUM RATINGS

Parameter	Source/Sink	Value	Units
Max. Current: VDD	Source	20	mA
Max. Current: VSS	Sink	50	mA
Max. Current: PIN	Source	5	mA
Max. Current: PIN	Sink	10	mA
Pin Current: at VOH	Source	3	mA
Pin Current: at VOL	Sink	8.5	mA
Port Current: GPIO	Source	20	mA
Port Current: GPIO	Sink	50	mA
Maximum Junction Temperature		155	°C

Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 16-14: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Device Characteristics	Units	Min	Typ	Max	Condition	
						VDD	Note
D010	Supply Current (IDD)	μA	—	13	58	2.0	IDD LP OSC (32 kHz)
			—	19	67	3.0	
			—	32	92	5.0	
D011		μA	—	135	316	2.0	IDD XT OSC (1 MHz)
			—	185	400	3.0	
			—	300	537	5.0	
D012		μA	—	240	495	2.0	IDD XT OSC (4 MHz)
			—	360	680	3.0	
		mA	—	0.660	1.20	5.0	
D013		μA	—	75	158	2.0	IDD EC OSC (1 MHz)
			—	155	338	3.0	
			—	345	792	5.0	
D014		μA	—	185	357	2.0	IDD EC OSC (4 MHz)
			—	325	625	3.0	
		mA	—	0.665	1.30	5.0	
D016		μA	—	245	476	2.0	IDD INTOSC (4 MHz)
			—	360	672	3.0	
			—	620	1.10	5.0	
D017		μA	—	395	757	2.0	IDD INTOSC (8 MHz)
		mA	—	0.620	1.20	3.0	
			—	1.20	2.20	5.0	
D018		μA	—	175	332	2.0	IDD EXTRC (4 MHz)
			—	285	518	3.0	
			—	530	972	5.0	
D019		mA	—	2.20	4.10	4.5	IDD HS OSC (20 MHz)
			—	2.80	4.80	5.0	

TABLE 16-18: OSCILLATOR PARAMETERS FOR PIC12F615-H (High Temp.)

Param No.	Sym	Characteristic	Frequency Tolerance	Units	Min	Typ	Max	Conditions
OS08	INTOSC	Int. Calibrated INTOSC Freq.(1)	±10%	MHz	7.2	8.0	8.8	2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ 150°C

Note 1: To ensure these oscillator frequency tolerances, Vdd and Vss must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

TABLE 16-19: COMPARATOR SPECIFICATIONS FOR PIC12F615-H (High Temp.)

Param No.	Sym	Characteristic	Units	Min	Typ	Max	Conditions
CM01	VOS	Input Offset Voltage	mV	—	±5	±20	(VDD - 1.5)/2

FIGURE 17-16: PIC12F609/615/617 IPD T1OSC vs. VDD

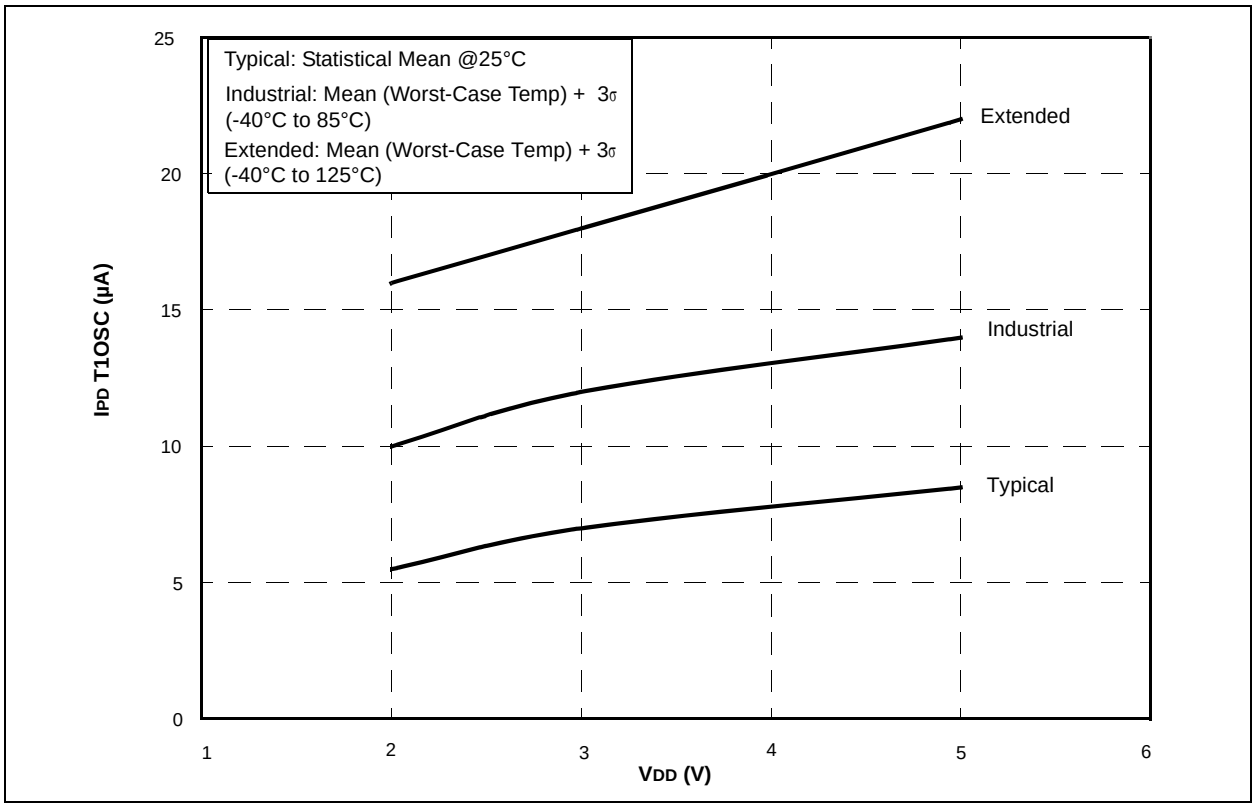


FIGURE 17-17: PIC12F615/617 IPD A/D vs. VDD

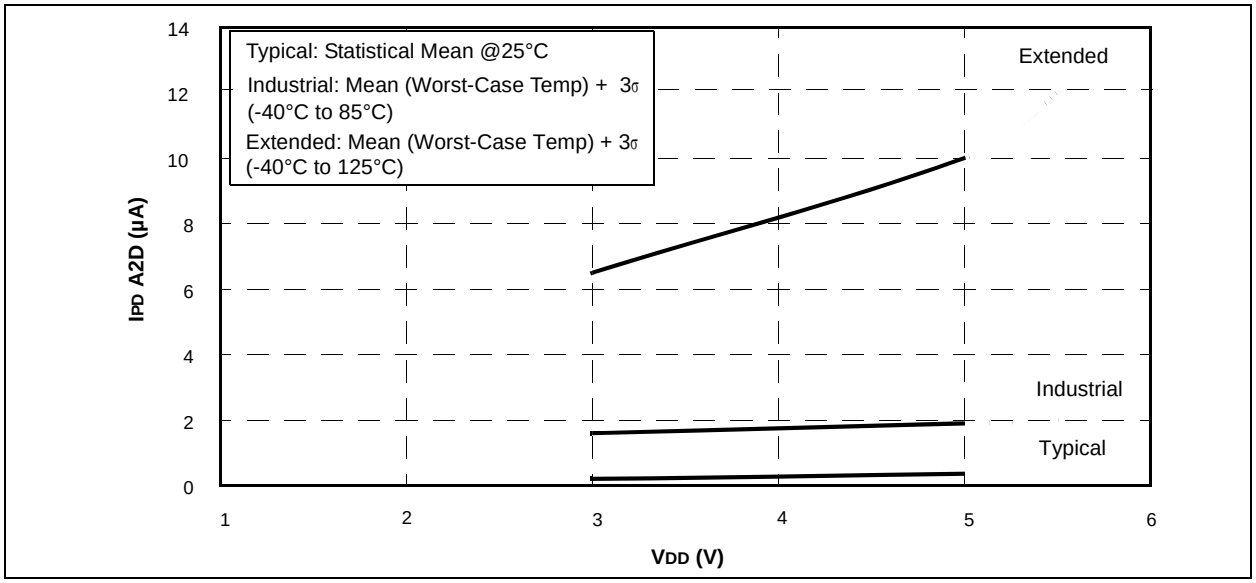


FIGURE 17-47: 0.6V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

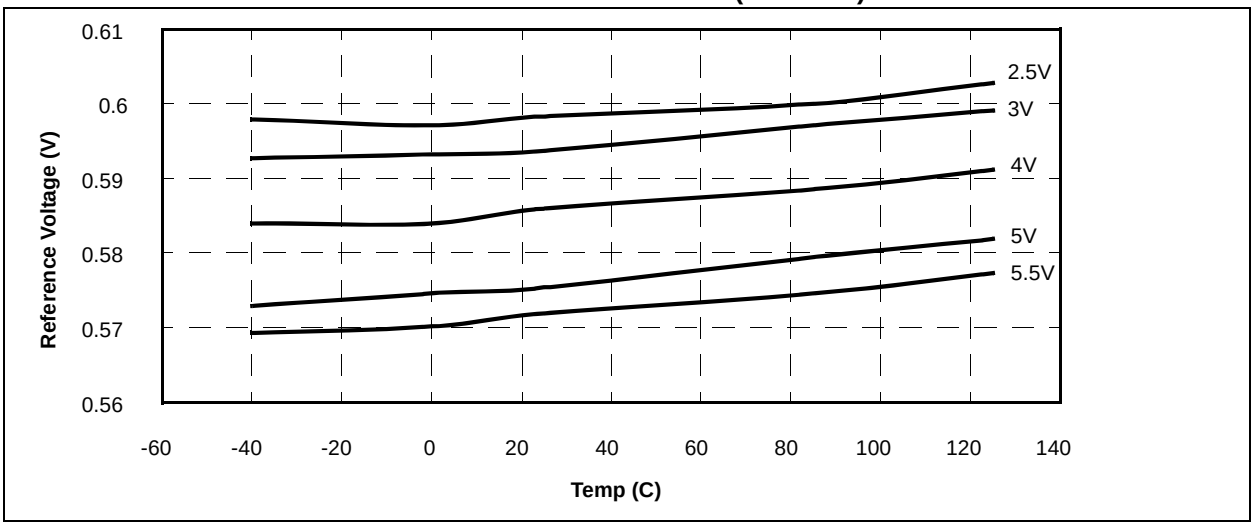


FIGURE 17-48: 1.2V REFERENCE VOLTAGE vs. TEMP (TYPICAL)

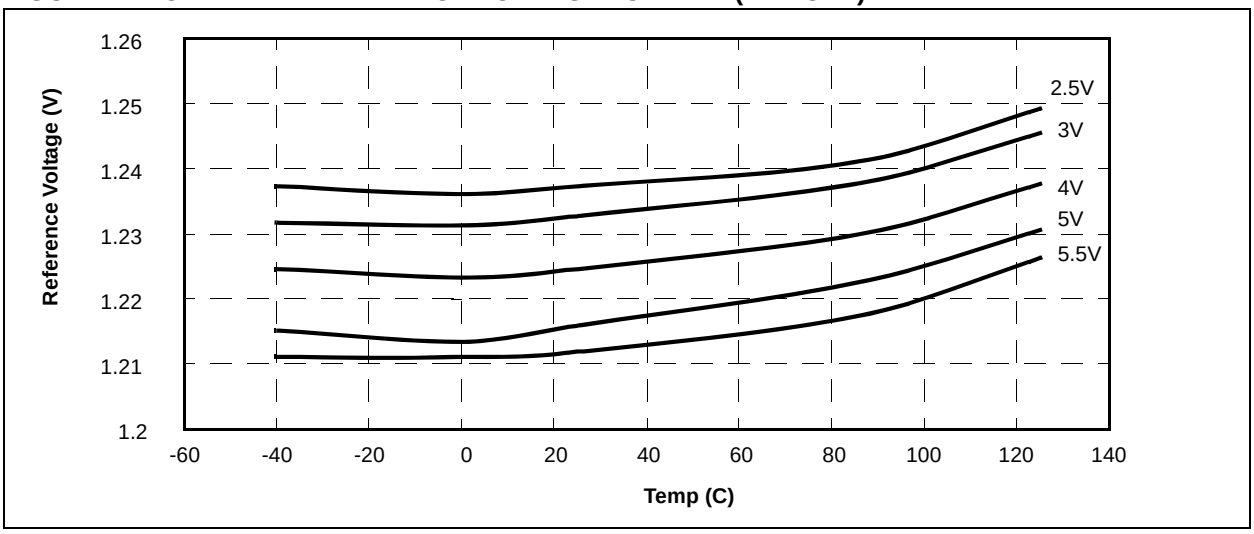
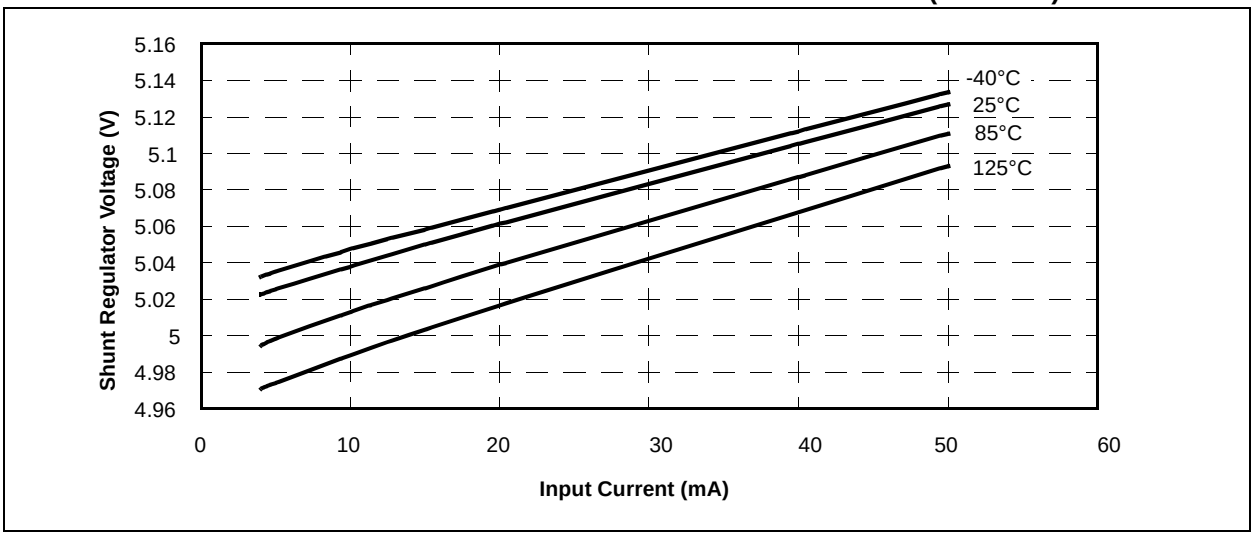


FIGURE 17-49: SHUNT REGULATOR VOLTAGE vs. INPUT CURRENT (TYPICAL)



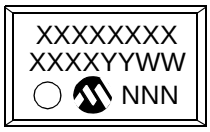
18.0 PACKAGING INFORMATION

18.1 Package Marking Information

8-Lead PDIP (.300”)

Example

8-Lead SOIC (.150”)



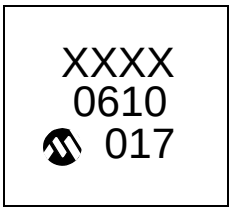
Example

8-Lead MSOP

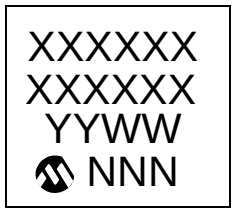
Example

8-Lead DFN (3x3 mm)

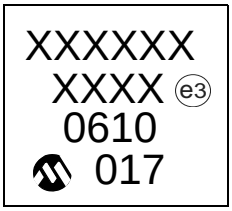
Example



8-Lead DFN (4x4 mm) (for PIC12F609/615/HV609/615 devices only)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC12F609, PIC12F609T(1), PIC12HV609, PIC12HV609T(1), PIC12F615, PIC12F615T(1), PIC12HV615, PIC12HV615T(1), PIC12F617, PIC12F617T(1)	
Temperature Range:	H = -40°C to +150°C	(High Temp)(3)
	I = -40°C to +85°C	(Industrial)
	E = -40°C to +125°C	(Extended)
Package:	P =	Plastic DIP (PDIP)
	SN =	8-lead Small Outline (150 mil) (SOIC)
	MS =	Micro Small Outline (MSOP)
	MF =	8-lead Plastic Dual Flat, No Lead (3x3) (DFN)
	MD =	8-lead Plastic Dual Flat, No Lead (4x4)(DFN)(1,2)
Pattern:	QTP, SQTP or ROM Code; Special Requirements (blank otherwise)	

Examples:

a) PIC12F615-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
b) PIC12F615-I/SN = Industrial Temp., SOIC package, 20 MHz
c) PIC12F615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
d) PIC12F609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
e) PIC12HV615T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
f) PIC12HV609T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
g) PIC12F617T-E/MF = Tape and Reel, Extended Temp., 3x3 DFN, 20 MHz
h) PIC12F617-I/P = Industrial Temp., PDIP package, 20 MHz
i) PIC12F615-H/SN = High Temp., SOIC package, 20 MHz

Note 1: T = in tape and reel for MSOP, SOIC and DFN packages only.
2: Not available for PIC12F617.
3: High Temp. available for PIC12F615 only.