NXP USA Inc. - MK20DX32VLH5 Datasheet





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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 13x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk20dx32vlh5

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins		7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3	1.2	V

3.5 Result of exceeding a rating



Terminology and guidelines



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	 @ −40 to 25°C 	—	0.176	0.859	μA	
	• @ 70°C	—	2.2	13.1	μA	
	• @ 105°C	—	13	23.9	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	_	0.19	0.22	μA	
	• @ 70°C	_	0.49	0.64	uA	
	• @ 105°C	—	2.2	3.2	μA	
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers					9
	• @ 1.8V					
	 @ -40 to 25°C 	_	0.57	0.67	uА	
	• @ 70°C	_	0.90	1.2	μA	
	• @ 105°C	_	2.4	3.5	uA	
	• @ 3.0V					
	 @ -40 to 25°C 	_	0.67	0.94	μA	
	• @ 70°C	_	1.0	1.4	μΑ	
	• @ 105°C	_	2.7	3.9	μA	

Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 2. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
- 4. Max values are measured with CPU executing DSP instructions
- 5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.
- 6. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- USB regulator disabled
- No GPIOs toggled







Figure 6. Test Access Port timing

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	—	400	_	μA	
	• 8 MHz (RANGE=01)	—	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C _x	EXTAL load capacitance					2, 3
Cy	XTAL load capacitance	—	_			2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	—	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	_	_	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1	_	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	_	_	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200	_	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	_	_	_	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
		_	0	_	kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)		0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

Table 14. Oscillator DC electrical specifications (continued)

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

- 3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
- 4. When low power mode is selected, R_F is integrated and must not be attached externally.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes			
	Word-write to FlexRAM for EEPROM operation								
t _{eewr16bers}	Word-write to erased FlexRAM location execution time		175	260	μs				
	Word-write to FlexRAM execution time:								
t _{eewr16b8k}	8 KB EEPROM backup	_	340	1700	μs				
t _{eewr16b16k}	16 KB EEPROM backup	_	385	1800	μs				
t _{eewr16b32k}	32 KB EEPROM backup	—	475	2000	μs				
	Longword-write to FlexRA	M for EEPR	OM operation	ı					
t _{eewr32bers}	Longword-write to erased FlexRAM location execution time		360	540	μs				
	Longword-write to FlexRAM execution time:								
t _{eewr32b8k}	8 KB EEPROM backup	_	545	1950	μs				
t _{eewr32b16k}	16 KB EEPROM backup	—	630	2050	μs				
t _{eewr32b32k}	32 KB EEPROM backup	_	810	2250	μs				

Table 19. Flash command timing specifications (continued)

1. Assumes 25MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash high voltage current behaviors Table 20. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	_	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	_	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 21. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes		
Program Flash								
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	_	years			
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100		years			
n _{nvmcycp}	Cycling endurance	10 K	50 K		cycles	2		
Data Flash								
t _{nvmretd10k}	Data retention after up to 10 K cycles	5	50		years			

Table continues on the next page ...

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
t _{nvmretd1k}	Data retention after up to 1 K cycles	20	100	_	years	
n _{nvmcycd}	Cycling endurance	10 K	50 K	_	cycles	2
	FlexRAM as	s EEPROM				
t _{nvmretee100}	Data retention up to 100% of write endurance	5	50		years	
t _{nvmretee10}	Data retention up to 10% of write endurance	20	100		years	
	Write endurance					3
n _{nvmwree16}	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
n _{nvmwree128}	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
n _{nvmwree512}	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
n _{nvmwree4k}	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
n _{nvmwree8k}	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

Table 21. NVM reliability specifications (continued)

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40°C \leq T_j \leq 125°C.

3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

Writes_FlexRAM =
$$\frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write}_\text{efficiency} \times n_{\text{nvmcycd}}$$

where

• Writes_FlexRAM — minimum number of writes to each FlexRAM location

Num	Description	Min.	Max.	Unit
EP1	EZP_CK frequency of operation (all commands except READ)	—	f _{SYS} /2	MHz
EP1a	EZP_CK frequency of operation (READ command)		f _{SYS} /8	MHz
EP2	EZP_CS negation to next EZP_CS assertion	2 x t _{EZP_CK}	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5		ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	_	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2		ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	_	ns
EP7	EZP_CK low to EZP_Q output valid		17	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	_	12	ns







6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 23 and Table 24 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV _{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} - V _{DDA})	-100	0	+100	mV	2
ΔV _{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} - V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	Reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage		V _{REFL}	_	V _{REFH}	V	
C _{ADIN}	Input	16 bit modes	_	8	10	pF	
	capacitance	• 8/10/12 bit modes	_	4	5		
R _{ADIN}	Input resistance			2	5	kΩ	
R _{AS}	Analog source resistance	13/12 bit modes f _{ADCK} < 4MHz			5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13 bit modes	1.0		18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	_	12.0	MHz	4
C _{rate}	ADC conversion	≤ 13 bit modes					5
	rate	No ADC hardware averaging	20.000	_	818.330	Ksps	
		conversions enabled, subsequent conversion time					

6.6.1.1 16-bit ADC operating conditions Table 23. 16-bit ADC operating conditions

Table continues on the next page...

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
	ADC	ADLPC=1, ADHSC=0	1.2	2.4	3.9	MHz	t _{ADACK} = 1/
	asynchronous clock source	ADLPC=1, ADHSC=1	3.0	4.0	7.3	MHz	f _{ADACK}
[†] ADACK		ADLPC=0, ADHSC=0	2.4	5.2	6.1	MHz	
		ADLPC=0, ADHSC=1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapte	r for sample	times			I
TUE	Total unadjusted	12 bit modes	_	±4	±6.8	LSB ⁴	5
	error	• <12 bit modes	_	±1.4	±2.1		
DNL	Differential non- linearity	12 bit modes	_	±0.7	-1.1 to +1.9	LSB ⁴	5
		• <12 bit modes	_	±0.2	-0.3 to 0.5		
INL	Integral non- linearity • 12 bit modes			±1.0	-2.7 to +1.9	LSB ⁴	5
		 <12 bit modes 	_	±0.5	-0.7 to +0.5		
E _{FS}	Full-scale error	12 bit modes	—	-4	-5.4	LSB ⁴	V _{ADIN} =
		 <12 bit modes 	—	-1.4	-1.8		V _{DDA}
							5
EQ	Quantization error	16 bit modes	_	-1 to 0	_	LSB ⁴	
		 ≤13 bit modes 			±0.5		
ENOB	Effective number	16 bit differential mode					6
	OF DITS	• Avg=32	12.8	14.5	—	bits	
		• Avg=4	11.9	13.8	—	bits	
		16 bit single-ended mode					
		• Avg=32	12.2	13.0		bite	
		• Avg=4	11.4	13.1	_	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02	2 × ENOB +	1.76	dB	
THD	Total harmonic	16 bit differential mode					7
	distortion	• Avg=32	_	-94	_	dB	
		16 bit single-ended mode		-85		dB	
		• Avg=32				60	

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Table continues on the next page...

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
SFDR	Spurious free dynamic range	 16 bit differential mode Avg=32 16 bit single-ended mode Avg=32 	82 78	82 95 78 90		dB dB	7
EIL	Input leakage error			I _{In} × R _{AS}		mV	I _{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	-40°C to 105°C	_	1.715	_	mV/°C	
V _{TEMP25}	Temp sensor voltage	25°C	_	719	_	mV	

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

 The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.

- 4. 1 LSB = $(V_{REFH} V_{REFL})/2^N$
- 5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{out}	Voltage reference output — factory trim	1.1584	_	1.2376	V	
V _{out}	Voltage reference output — user trim	1.193	_	1.197	V	
V _{step}	Voltage reference trim step	—	0.5	_	mV	
V _{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	_	80	mV	
I _{bg}	Bandgap only current	—	_	80	μA	1
I _{lp}	Low-power buffer current	—	_	360	uA	1
I _{hp}	High-power buffer current	—	_	1	mA	1
ΔV_{LOAD}	Load regulation				μV	1, 2
	• current = ± 1.0 mA	—	200	_		
T _{stup}	Buffer startup time	—	_	100	μs	
V _{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	_	2	_	mV	1

Table 27. VREF full-range operating behaviors (continued)

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 28. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T _A	Temperature	0	50	°C	

Table 29. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See General switching specifications.

6.8 Communication interfaces



Figure 15. DSPI classic SPI timing — master mode

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	_	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	_	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	_	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	_	14	ns

Table 33. Slave mode DSPI timing (limited voltage range)



Figure 16. DSPI classic SPI timing — slave mode

6.8.8 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.8.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	_	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	_	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns

Table 36. I2S/SAI master mode timing

Table 40. TSI electrical specifications (continued)

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
T _{Con20}	Response time @ 20 pF	8	15	25	μs	12
I _{TSI_RUN}	Current added in run mode	—	55	_	μA	
I _{TSI_LP}	Low power mode current adder	—	1.3	2.5	μA	13

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.

2. Fixed external capacitance of 20 pF.

3. REFCHRG = 2, EXTCHRG=0.

4. REFCHRG = 0, EXTCHRG = 10.

- 5. $V_{DD} = 3.0 V.$
- 6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
- 7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
- 8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.
- 9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.
- 10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.
- 11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN)

The typical value is calculated with the following configuration:

 $I_{ext} = 6 \ \mu A \ (EXTCHRG = 2), PS = 128, NSCN = 2, I_{ref} = 16 \ \mu A \ (REFCHRG = 7), C_{ref} = 1.0 \ pF$

The minimum value is calculated with the following configuration:

 $I_{ext} = 2 \ \mu A$ (EXTCHRG = 0), PS = 128, NSCN = 32, $I_{ref} = 32 \ \mu A$ (REFCHRG = 15), $C_{ref} = 0.5 \ pF$

The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.

- 12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
- 13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number				
64-pin LQFP	98ASS23234W				
64-pin MAPBGA	98ASA00420D				

Pinout

64 Map Bga	64 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E5	24	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
D5	25	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UARTO_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
G5	26	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
F5	27	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2			I2S0_TX_ BCLK	JTAG_TRST_ b	
H6	28	PTA12	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
G6	29	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
G7	30	VDD	VDD	VDD								
H7	31	VSS	VSS	VSS								
H8	32	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
G8	33	PTA19	XTALO	XTALO	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1		
F8	34	RESET_b	RESET_b	RESET_b								
F7	35	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
F6	36	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
E7	37	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UARTO_RTS_ b			FTM0_FLT3		
E8	38	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2CO_SDA	UARTO_CTS_ b/ UARTO_COL_ b			FTM0_FLT0		
E6	39	PTB16	TSI0_CH9	TSI0_CH9	PTB16		UART0_RX			EWM_IN		
D7	40	PTB17	TSI0_CH10	TSI0_CH10	PTB17		UART0_TX			EWM_OUT_b		
D6	41	PTB18	TSI0_CH11	TSI0_CH11	PTB18			12S0_TX_ BCLK				
C7	42	PTB19	TSI0_CH12	TSI0_CH12	PTB19			I2S0_TX_FS				
D8	43	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG					
C6	44	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0		I2S0_TXD0		
B7	45	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1		I2S0_TX_FS		
C8	46	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2		I2S0_TX_ BCLK		
E3	47	VSS	VSS	VSS								
E4	48	VDD	VDD	VDD								

64 MAP	64 LQFP	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
BGA												
B8	49	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
A8	50	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	12S0_RXD0		CMP0_OUT		
A7	51	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_ BCLK		I2S0_MCLK		
B6	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS				
A6	53	PTC8	CMP0_IN2	CMP0_IN2	PTC8			I2S0_MCLK				
B5	54	PTC9	CMP0_IN3	CMP0_IN3	PTC9			I2S0_RX_ BCLK				
B4	55	PTC10	DISABLED		PTC10			I2S0_RX_FS				
A5	56	PTC11/ LLWU_P11	DISABLED		PTC11/ LLWU_P11							
C3	57	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b					
A4	58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b					
C2	59	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX					
B3	60	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX					
A3	61	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UARTO_RTS_ b	FTM0_CH4		EWM_IN		
C1	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_ b	FTM0_CH5		EWM_OUT_b		
B2	63	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
A2	64	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K20 Pinouts

Pinout

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Revision History

	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11/ LLWU_P11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
В	PTE1/ LLWU_P0	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	В
С	PTD5	PTD2/ LLWU_P13	PTD0/ LLWU_P12	VSS	VDD	PTC1/ LLWU_P6	PTB19	PTC3/ LLWU_P7	С
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	USB0_DP	VOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	ADC0_DM0	ADC0_DM3	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	RESET_b	F
G	ADC0_DP0	ADC0_DP3	VREFL	VREFH	PTA4/ LLWU_P3	PTA13/ LLWU_P4	VDD	PTA19	G
н	VREF_OUT CMP1_IN5/ CMP0_IN5	CMP1_IN3/ ADC0_SE23	XTAL32	EXTAL32	VBAT	PTA12	VSS	PTA18	н
	1	2	3	4	5	6	7	8	•

Figure 24. K20 64 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes		
2	2/2012	Initial public release		
3	4/2012	 Replaced TBDs throughout. Updated "Power mode transition operating behaviors" table. Updated "Power consumption operating behaviors" table. For "Diagram: Typical IDD_RUN operating behavior" section, added "VLPR mode supply current vs. core frequency" figure. Updated "EMC radiated emissions operating behaviors" section. Updated "Thermal operating requirements" section. Updated "MCG specifications" table. Updated "VREF full-range operating behaviors" table. Updated "I2S/SAI Switching Specifications" table. Updated "TSI electrical specifications" table. 		

Table continues on the next page...

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