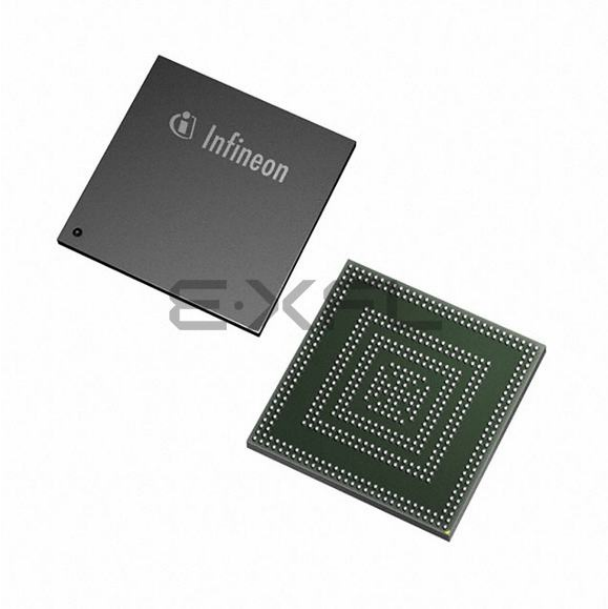
Infineon Technologies - TC1798F512F300EPABKXUMA2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	ASC, CANbus, EBI/EMI, FlexRay, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	238
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	192K x 8
RAM Size	288K x 8
Voltage - Supply (Vcc/Vdd)	1.235V ~ 3.63V
Data Converters	A/D 8x10b, 64x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	516-LFBGA
Supplier Device Package	PG-LFBGA-516-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1798f512f300epabkxuma2

  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 64 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, ADC2, and ADC3)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 238 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1798ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1798N-512F300EP** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 300 MHz operation at full temperature range

- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules

3 Pinning

Figure 4 is showing the TC1798 Logic Symbol.

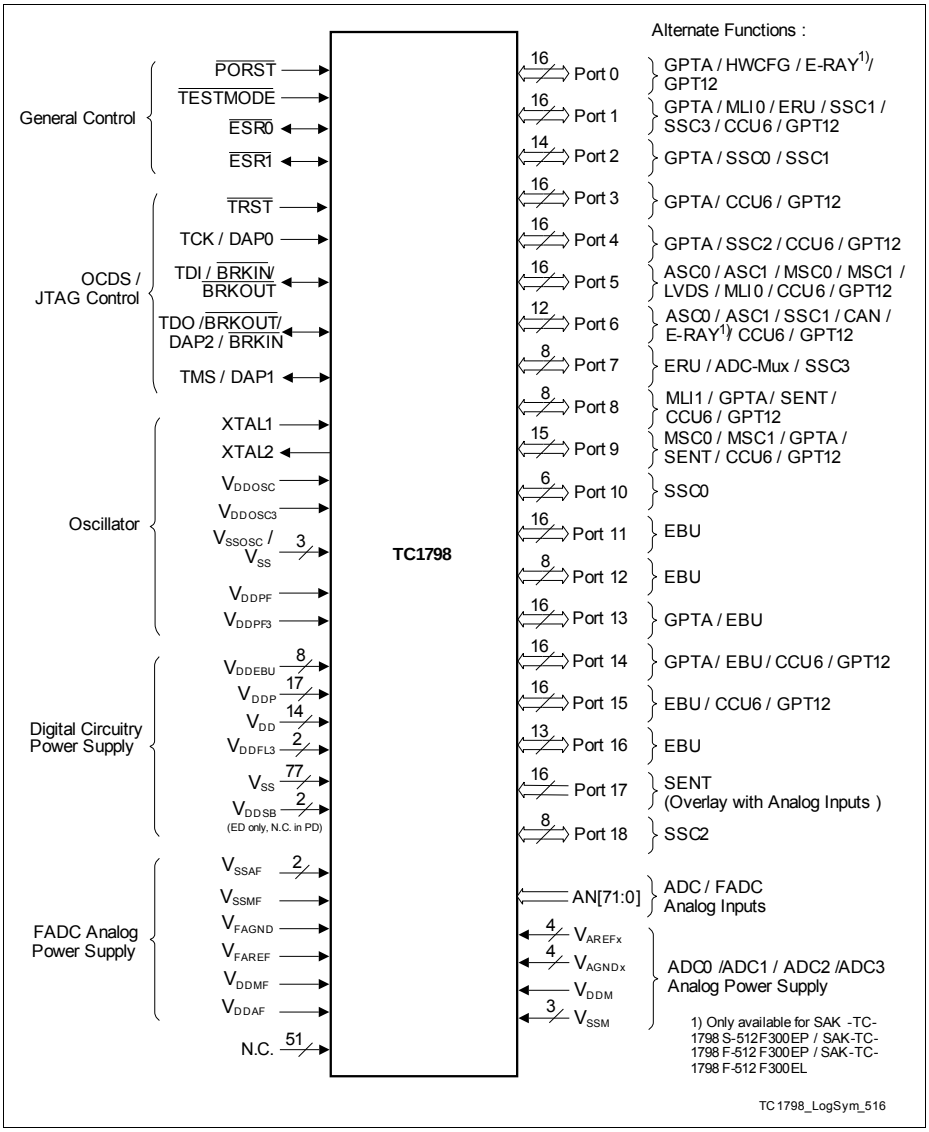

Figure 4 TC1798 Logic Symbol

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J2	P1.5	I/O	A1/ PU	**Port 1 General Purpose I/O Line 35**
	TREADY0A	I		**MLI0 transmit Channel ready Input A**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
M7	P1.6	I/O	A2/ PU	**Port 1 General Purpose I/O Line 6**
	TVALID0A	O1		**MLI0 transmit Channel valid Output A**
	SLSO10	O2		**SSC1 Slave Select Output Line 10**
	COUT60	O3		**CCU60**
M6	P1.7	I/O	A2/ PU	**Port 1 General Purpose I/O Line 7**
	CC61INB	I		**CCU60**
	CC61INA	I		**CCU61**
	TData0	O1		**MLI0 transmit Channel Data Output**
	CC61	O2		**CCU61**
	T3OUT	O3		**GPT120**
L2	P1.8	I/O	A1/ PU	**Port 1 General Purpose I/O Line 8**
	RCLK0A	I		**MLI0 Receive Channel Clock Input A**
	OUT64	O1		**OUT64 Line of GPTA0**
	OUT64	O2		**OUT64 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
M10	P1.9	I/O	A2/ PU	**Port 1 General Purpose I/O Line 9**
	RREADY0A	O1		**MLI0 Receive Channel ready Output A**
	SLSO11	O2		**SSC 1Slave Select Output Line 11**
	OUT65	O3		**OUT65 Line of GPTA0**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F12	P2.8	I/O	A1/ PU	**Port 2 General Purpose I/O Line 8**
	IN0	I		**IN0 Line of GPTA0**
	IN0	I		**IN0 Line of GPTA1**
	IN0	I		**IN0 Line of LTCA2**
	CCPOS0A	I		**CCU62**
	T12HRB	I		**CCU63**
	T3INB	I		**GPT120**
	T3INA	I		**GPT121**
	OUT0	O1		**OUT0 Line of GPTA0**
	OUT0	O2		**OUT0 Line of GPTA1**
	OUT0	O3		**OUT0 Line of LTCA2**
B6	P2.9	I/O	A1/ PU	**Port 2 General Purpose I/O Line 9**
	IN1	I		**IN1 Line of GPTA0**
	IN1	I		**IN1 Line of GPTA1**
	IN1	I		**IN1 Line of LTCA2**
	OUT1	O1		**OUT1 Line of GPTA0**
	OUT1	O2		**OUT1 Line of GPTA1**
	OUT1	O3		**OUT1 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K20	P5.5	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 5**
	SDI0	I		**MSC0 Serial Data Input**
	T12HRC	I		**CCU62**
	T13HRC	I		**CCU62**
	CCPOS2A	I		**CCU63**
	T4EUDB	I		**GPT120**
	T4EUDA	I		**GPT121**
	OUT77	O1		**OUT77 Line of GPTA0**
	OUT77	O2		**OUT77 Line of GPTA1**
	OUT101	O3		**OUT101 Line of LTCA2**
G25	P5.6	I/O	A2/ PU	**Port 5 General Purpose I/O Line 6**
	CC60INA	I		**CCU62**
	CC60INB	I		**CCU63**
	EN10	O1		**MSC1 Device Select Output 0**
	TVALID0B	O2		**MLI0 transmit Channel valid Output B**
	CC60	O3		**CCU62**
J21	P5.7	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 7**
	SDI1	I		**MSC1 Serial Data Input**
	CC61INA	I		**CCU62**
	CC61INB	I		**CCU63**
	OUT79	O1		**OUT79 Line of GPTA0**
	OUT79	O2		**OUT79 Line of GPTA1**
	CC61	O3		**CCU62**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F8	P6.5	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 5**
	MRST1	I		**SSC1 Master Receive Input (Master Mode)**
	MRST1	O1		**SSC1 Slave Transmit Output (Slave Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**
F9	P6.6	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 6**
	SCLK1	I		**SSC1 Clock Input/Output**
	SCLK1	O1		**SSC1 Clock Input/Output**
	Reserved	O2		**-**
	Reserved	O3		**-**
J10	P6.7	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 7**
	SLSI1	I		**SSC1 slave Select Input**
	T6OFL	O1		**GPT120**
	Reserved	O2		**-**
	Reserved	O3		**-**
G10	P6.8	I/O	A2/ PU	**Port 6 General Purpose I/O Line 8**
	RXDCAN0	I		**CAN Node 0 Receiver Input 0** **CAN Node 3 Receiver Input 1**
	RXD0B	I		**ASC0 Receiver Input/Output B**
	CAPINB	I		**GPT120**
	CAPINA	I		**GPT121**
	Reserved	O1		**-**
	RXD0B	O2		**ASC0 Receiver Input/Output B**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H6	P6.13	I/O	A2/ PU	**Port 6 General Purpose I/O Line 13**
	TXDCAN2	O1		**CAN Node 2 Transmitter Output**
	TXDA	O2		**E-Ray Channel A transmit Data Output** [2]
	COUT62	O3		**CCU60**
J6	P6.14	I/O	A1/ PU	**Port 6 General Purpose I/O Line 14**
	RXDCAN3	I		**CAN Node 3 Receiver Input 0** **CAN Node 2 Receiver Input 1**
	RXDB1	I		**E-Ray Channel B Receive Data Input 1** [2]
	Reserved	O1		**-**
	Reserved	O2		**-**
	COUT63	O3		**CCU60**
K6	P6.15	I/O	A2/ PU	**Port 6 General Purpose I/O Line 15**
	CC60INB	I		**CCU60**
	CC60INA	I		**CCU61**
	TXDCAN3	O1		**CAN Node 3 Transmitter Output**
	TXDB	O2		**E-Ray Channel B transmit Data Output** [2]
	CC60	O3		**CCU61**
Port 7				
N10	P7.0	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 0**
	MRST3	I		**SSC3 Master Receive Input (Master Mode)**
	REQ4	I		**External trigger Input 4**
	AD2EMUX2	O1		**ADC2 external multiplexer Control Output 2**
	MRST3	O2		**SSC3 Slave Transmit Output (Slave Mode)**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L9	P8.7	I/O	A1/ PU	**Port 8 General Purpose I/O Line 7**
	IN47	I		**IN47 Line of GPTA0**
	IN47	I		**IN47 Line of GPTA1**
	RDATA1A	I		**MLI1 Receive Channel Data Input A**
	SENT7	I		**SENT Digital Input**
	OUT47	O1		**OUT47 Line of GPTA0**
	COUT61	O2		**CCU61**
	T6OUT	O3		**GPT121**
Port 9				
K22	P9.0	I/O	A2/ PU	**Port 9 General Purpose I/O Line 0**
	IN48	I		**IN48 Line of GPTA0**
	IN48	I		**IN48 Line of GPTA1**
	COUT63	O1		**CCU62**
	OUT48	O2		**OUT48 Line of GPTA1**
	EN12	O3		**MSC1 Device Select Output 2**
J24	P9.1	I/O	A2/ PU	**Port 9 General Purpose I/O Line 1**
	IN49	I		**IN49 Line of GPTA0**
	IN49	I		**IN49 Line of GPTA1**
	CC60INB	I		**CCU62**
	CC60INA	I		**CCU63**
	CC60	O1		**CCU63**
	OUT49	O2		**OUT49 Line of GPTA1**
	EN11	O3		**MSC1 Device Select Output 1**

  - limited to 10000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $1.3V + 7.5\% < V_{DD}$ / V_{DDOSC} / V_{DDPF} / V_{DDAF} < 1.3V + 10% (overvoltage condition):
  - limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- V_{DDP} / V_{DDOSC3} / V_{DDPF3} / V_{DDFL3} / V_{DDMF} / V_{DDEBU}< 3.3 V ± 10%
  - $3.3V + 5\% < V_{DDP}$ / V_{DDOSC3} / V_{DDPF3} / V_{DDFL3} / V_{DDMF} / V_{DDEBU}< 3.3V + 10% (overvoltage condition):
    limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.

Table 13 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P2.[4:2], P6.[6:9]
2	P6.[5:4], P6.[11:10]
3	P6.[15:12]
4	P8.[5:0]
5	P8.[7:6], P1.[15:13]
6	P1.5, P1.[11:8]
7	P1.[4:2], P1.6, P1.12
8	P1.[1:0], P7.[2:0]
9	P7.[7:3]
10	P4.[6:0]
11	P4.[10:7]
12	P4.[15:11]
13	P10.[5:0]
14	P15.[7:4], P16.[1:0]
15	P15.3, P15.[12:11], P16.[5:3]
16	P15.[2:0], P15.[9:8], P16.2, P16.8
17	P15.10, P15.[15:13], P16.[7:6]
18	P14.[15:12]
19	P14.[11:8], P16.12
20	P14.[7:3], P16.11
21	P13.15, P14.[2:0]

Table 13 Pin Groups for Overload / Short-Circuit Current Sum Parameter (cont'd)

Group	Pins
22	P13.[14:11]
23	P13.[10:8], P16.10
24	P13.[7:4], P16.9
25	P12.5, P13.[3:0]
26	P12.[4:0]
27	P11.[15:11]
28	P11.[10:6]
29	P11.[5:2]
30	P11.[1:0], P12.[7:6]
31	P9.10, P9.14
32	P9.7, P9.13
33	P9.[4:2], P9.6
34	P9.1, P9.5, P9.[9:8]
35	P9.0, P9.[12:11]
36	P5.[11:8]
37	P5.6, P5.[15:12]
38	P5.0, P5.[5:2], P5.7
39	P3.[5:0], P5.1
40	P3.[12:6]
41	P0.[3:0], P3.[15:13]
42	P0.[11:4]
43	P0.[14:12]
44	P0.15, P18.[5:0]
45	P2.[15:11], P18.[7:6]
46	P2.[10:5]

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage low class A2 pads	V_{OLA2} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= strong
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 18 Standard_Pads Class_B

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis, B class pads[1)]	$HYSB$ CC	0.05 x V_{DDEBU}	–	–	V	V_{DDEBU}= 1.8 V
		0.08 x V_{DDEBU}	–	–	V	V_{DDEBU}= 2.5 V
		0.1 x V_{DDEBU}	–	–	V	V_{DDEBU}= 3.3 V
Input Leakage Current, class B pads	I_{OZB} CC	-3000	–	3000	nA	V_{DDEBU}= 1.8 V; V_i> 0 V; V_i< V_{DDEBU} V
		-6000	–	6000	nA	V_i> 0 V; V_i> V_{DDEBU}/2 + 0.6 V; V_i≤ V_{DDEBU} V; V_i≤ V_{DDEBU}/2 - 0.6 V
		-3000	–	3000	nA	V_i> V_{DDEBU}/2 - 0.6 V; V_i< V_{DDEBU}/2 + 0.6 V

Table 22 LVDS_Pads Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type LVDS	t_{RL} CC	–	–	2	ns	termination 100 Ω ± 1 %; differential capacitance = 10 pF; input capacitance = 20 pF
Pad set-up time	t_{SET_LVDS} CC	–	–	13	µs	termination 100 Ω ± 1 %
Output Differential Voltage	V_{OD} CC	150	–	400	mV	termination 100 Ω ± 1 %
Output voltage high, pad class F, LVDS mode	V_{OH} CC	–	–	1525	mV	termination 100 Ω ± 1 %
Output voltage low, pad class F, LVDS mode	V_{OL} CC	875	–	–	mV	termination 100 Ω ± 1 %
Output Offset Voltage	V_{OS} CC	1075	–	1325	mV	termination 100 Ω ± 1 %

Table 25 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference ground	V_{FAGND} SR	V_{SSAF} - 0.05	–	V_{SSAF} + 0.05	V	
Analog reference voltage	V_{FAREF} SR	2.97	–	3.63[5) 6)]	V	

1) This value applies in power-down mode.

2) No missing codes.

3) Calibration should be preformed at each power-up. In case of a continous operation, it should be performed minimium once per week.

4) The offser error voltage drifts over the whole temperature range maximum +-3LSB.

5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

6) A running conversion may become inexact in case of violating the nomal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

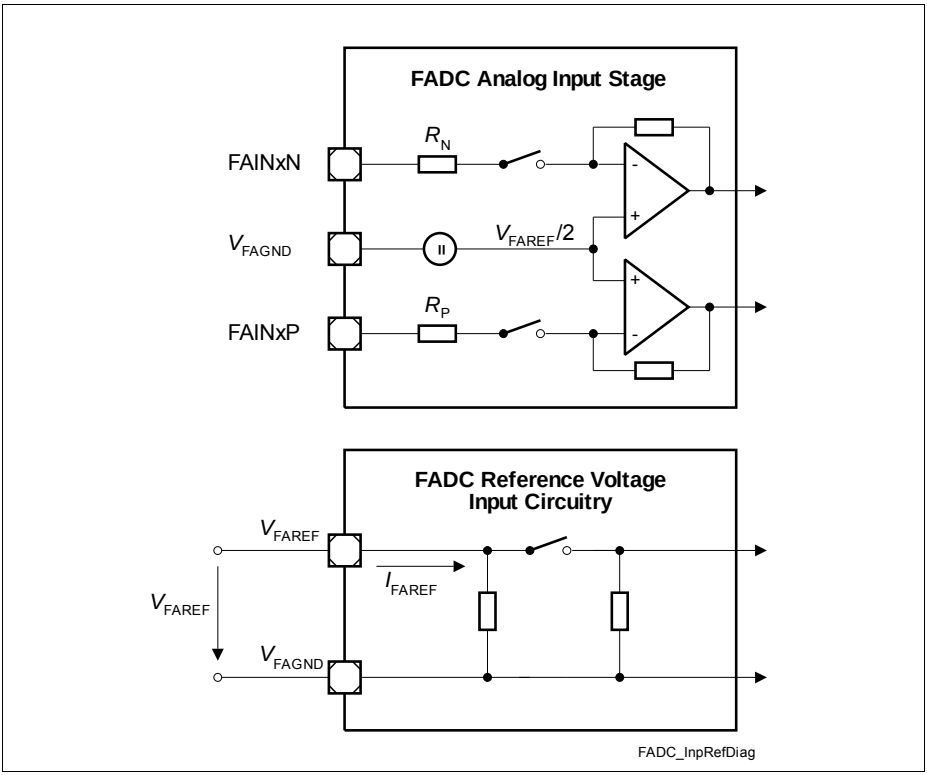

Figure 8 FADC Input Circuits

Table 28 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
E-Ray PLL core supply current	I_{DDPF} CC	–	–	4	mA	
Oscillator core supply current	I_{DDOSC} CC	–	–	3	mA	
FADC core supply current	I_{DDAF} CC	–	–	26	mA	
Sum of all 1.3 V supply currents	I_{DDSUM} CC	–	–	689	mA	power pattern= realistic; fCPU=300 MHz
E-Ray PLL 3.3V supply	I_{DDPF3} CC	–	–	4	mA	
Oscillator power supply current, 3.3V	I_{DDOSC3} CC	–	–	11	mA	
FADC analog supply current, 3.3V	I_{DDMF} CC	–	–	15	mA	
I_{DDEBU} current at PORST Low	I_{DDEBU_PORST} CC	–	–	1	mA	
I_{DDP} current at PORST Low	I_{DDP_PORST} CC	–	–	7	mA	
I_{DDP} current no pad activity, LVDS off [5]	I_{DDP} CC	–	–	I_{DDP_PORST} + 25	mA	including flash read current
		–	–	I_{DDP_PORST} + 55	mA	including flash programming current [6]
		–	–	I_{DDP_PORST} + 40 [7]	mA	including flash erase verify current [6]

Timing for EBU DDR Clock Outputs

The EBU provides three possible DDR clock outputs depending on the type of device being accessed. These are

- Differential clock for accessing devices using a DDRAM type protocol on the DDRCLKO and $\overline{\text{DDRCLKO}}$ pins.
- Differential clock for accessing devices using a burst flash type protocol on the BFCLKO and $\overline{\text{DDRCLKO}}$ pins.
- A single-ended clock on OCLKO (MR/$\overline{\text{W}}$) for interfacing to ONFI 2 compliant devices.

All these clocks operate with identical timing parameters and have a restricted load limit of 10pF for DDR operation.

The rising edge on the differential clocks is defined as when a rising edge on DDRCLKO or BFCLKO transitions past a falling edge on $\overline{\text{DDRCLKO}}$.

Timings apply at VDD_{EBU} = 1.8 volts

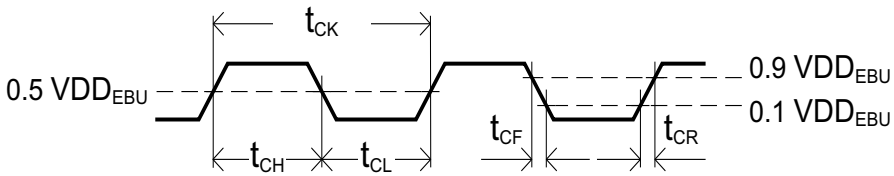

Figure 29 Timing Waveform for DDR Clock Signals

Timing for EBU DDR Control Outputs

The EBU control state machine will ensure that commands and signal transitions are generated in the correct clock cycle to meet device requirements. This section also applies when accessing SDRAM devices.

The EBU will generate address (A[15:0]) and control (CKE, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WR}}$) outputs on the falling edge of the DDR clock to allow nominally symmetric setup and hold margins around the rising edge of the clock. For SDRAM devices, the same address and control signals are required but, in addition, the write data (AD[31:0]) and DQM signals ($\overline{\text{BC}}$[3:0]) are required to meet the same timing requirements.

As these parameters apply to SDRAM as well as DDR devices, the load limit should be taken to be 40pF.

- add parameter t_{POR_APP}
- replace in Operating Conditions Parameter Note MA = modulation amplitude by footnote 1)
- remove the redundant test condition I_{OH} for RDSON NMOS
- remove the redundant test condition I_{OL} for RDSON PMOS
- add parameter V_{ILSD} to class S pads
- remove footnote 2 from FADC
- remove capacitance conditions for LVDS pad parameters as loads are defined by interface (MSC) timings

The following changes where done between Version 0.7 and 1.0 of this document:

- add product options **SAK-TC1798S-512F300EP and SAK-TC1798N-512F300EP**
- remove product options **SAK-TC1798F-512F240EP and SAK-TC1798F-512F240EL**
- update block diagrams to cover new options
- add note to TC1798 Logic Symbol figure and pin list for E-RAY pins availability
- add identification registers for new options
- adapt Absolute Maximum Rating
- clarify pad supply levels in Pin Reliability in Overload section
- correct errors for analog inputs in tables 10 and 11
- add note at the end of Pin Reliability in Overload section
- clarify wording for valid operating conditions
- correct section Extended Range Operating Conditions for the 3.3 V area
- increase limit in Extended Range Operating Conditions from 1 hour to 1000 hours
- add negative limit for class S pad leakage
- removed RDSON parameters for class F pads weak driver as only medium is available and update values
- change description of parameter t_{CAL} for the ADC
- update footnote 10 for the ADC
- update definition of INL and TUE for ADC3
- split FADC DNL parameter into two conditions and change value for gain 4 and 8
- update all current values of table 28 (Power Supply Parameters)
- add footnote 5 to I_{DDP}
- improve parameters I_{DDFL3}
- add footnote for D-Flash currents in power section
- add section 5.2.6.1.
- rework first sentence for chapter 5.3
- increase max values for parameter t_B
- reduce min value for t_L for both PLLs
- split f_{VCO} for the system PLL into two conditions
- change formula 10
- add for MLI and SSC timing parameter: valid strong driver medium edge only
- change MLI parameter t_{17} min value

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