



#### Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx110f016bt-v-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e<sup>®</sup> Support
- · Enhanced JTAG (EJTAG) Controller

#### 3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- · 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

## 3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

## TABLE 3-1:MIPS32<sup>®</sup> M4K<sup>®</sup> PROCESSOR CORE HIGH-PERFORMANCE INTEGERMULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul rt) (div rs)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU,	16 bits	1	1
MSUB/MSUBU	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32



#### FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX150/250 DEVICES (32 KB RAM, 128 KB FLASH)

2: The size of this memory region is programmable (see Section 3. "Memory Organization" (DS60001115) in the "*PIC32 Family Reference Manual*") and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R	R	R	R	R	R	R	R		
31:24				BMXPFN	1SZ<31:24>					
22:46	R	R	R	R	R	R	R	R		
23.10	BMXPFMSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXPFMSZ<15:8>									
7.0	R	R	R	R	R	R	R	R		
7:0		BMXPFMSZ<7:0>								

#### REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

## Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXPFMSZ<31:0>: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes: 0x00004000 = Device has 16 KB Flash 0x00008000 = Device has 32 KB Flash 0x00010000 = Device has 64 KB Flash 0x00020000 = Device has 128 KB Flash 0x00040000 = Device has 256 KB Flash

### REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04.04	R	R	R	R	R	R	R	R			
31:24				BMXBOO	TSZ<31:24>						
22.16	R	R	R	R	R	R	R	R			
23.10		BMXBOOTSZ<23:16>									
45.0	R	R	R	R	R	R	R	R			
15:8	BMXBOOTSZ<15:8>										
7.0	R	R	R	R	R	R	R	R			
7:0		BMXBOOTSZ<7:0>									

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits Static value that indicates the size of the Boot PFM in bytes: 0x00000C00 = Device has 3 KB boot Flash

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31.24	—	—	_	—	—	—	—	—	
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	—	—	—	—	—	—	—	—	
15:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
10.0	—	—	—	—	—	5	SRIPL<2:0> <sup>(1)</sup>		
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0	—	—		VEC<5:0> <sup>(1)</sup>					

#### REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

### Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

- bit 10-8 SRIPL<2:0>: Requested Priority Level bits<sup>(1)</sup>
  - 111-000 = The priority level of the latest interrupt presented to the CPU
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 VEC<5:0>: Interrupt Vector bits<sup>(1)</sup> 11111-00000 = The interrupt vector that is presented to the CPU
- Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31.24				IPTMF	₹<31:24>					
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	IPTMR<23:16>									
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15.0	IPTMR<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7.0		IPTMR<7:0>								

#### REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

## PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## FIGURE 8-1: OSCILLATOR DIAGRAM



 Refer to Section 6. "Oscillator Configuration" (DS60001112) in the "PIC32 Family Reference Manual" for help in determinin best oscillator components.

3. The PBCLK out is only available on the OSC2 pin in certain clock modes.

4. The USB PLL is only available on PIC32MX2XX devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
31:24	—			R	)<2017<20	1,3)			
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
23:16	RODIV<7:0>(1,3)								
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC	
15:8	ON	_	SIDL	OE	RSLP <sup>(2)</sup>	-	DIVSWEN	ACTIVE	
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0		_	_	_	ROSEL<3:0> <sup>(1)</sup>				

#### **REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

Legend:	HC = Hardware Clearable	HS = Hardware Settable		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31 Unimplemented: Read as '0'

bit 30-16	RODIV<14:0> Reference Clock Divider bits <sup>(1,3)</sup>
	The value selects the reference clock divider bits. See Figure 8-1 for information.
bit 15	ON: Output Enable bit
	1 = Reference Oscillator module is enabled
	0 = Reference Oscillator module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Peripheral Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
  - 0 =Continue module operation when the device enters lide mode
- bit 12 **OE:** Reference Clock Output Enable bit
  - 1 = Reference clock is driven out on REFCLKO pin
  - 0 = Reference clock is not driven out on REFCLKO pin
- bit 11 RSLP: Reference Oscillator Module Run in Sleep bit<sup>(2)</sup>
  - 1 = Reference Oscillator module output continues to run in Sleep
  - 0 = Reference Oscillator module output is disabled in Sleep
- bit 10 Unimplemented: Read as '0'
- bit 9 DIVSWEN: Divider Switch Enable bit
  - 1 = Divider switch is in progress
    - 0 = Divider switch is complete
- bit 8 ACTIVE: Reference Clock Request Status bit
  - 1 = Reference clock request is active
  - 0 = Reference clock request is not active
- bit 7-4 Unimplemented: Read as '0'
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
  - **2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
  - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24				ROTRI	√<8:1>			
22:16	R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	ROTRIM<0>	—	—	—	—	—	-	—
45.0	U-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	_	_	_	_	_	_	—
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	_	_	_	_	_	_	_	_

#### REGISTER 8-4: REFOTRIM: REFERENCE OSCILLATOR TRIM REGISTER

#### Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 ROTRIM<8:0>: Reference Oscillator Trim bits

**Note:** While the ON (REFOCON<15>) bit is '1', writes to this register do not take effect until the DIVSWEN bit is also set to '1'.

#### 11.3.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPnR registers (Register 11-2) are used to control output mapping. Like the [*pin name*]R registers, each register contains sets of 4 bit fields. The value of the bit field corresponds to one of the peripherals, and that peripheral's output is mapped to the pin (see Table 11-2 and Figure 11-3).

A null output is associated with the output register reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

#### FIGURE 11-3: EXAMPLE OF MULTIPLEXING OF REMAPPABLE OUTPUT FOR RPA0



## 11.3.6 CONTROLLING CONFIGURATION CHANGES

Because peripheral remapping can be changed during run time, some restrictions on peripheral remapping are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to the peripheral map:

- Control register lock sequence
- Configuration bit select lock

## 11.3.6.1 Control Register Lock Sequence

Under normal operation, writes to the RPnR and [*pin name*]R registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the Configuration bit, IOLOCK (CFGCON<13>). Setting IOLOCK prevents writes to the control registers; clearing IOLOCK allows writes.

To set or clear the IOLOCK bit, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

## 11.3.6.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the RPnR and [*pin name*]R registers. The Configuration bit, IOL1WAY (DEVCFG3<29>), blocks the IOLOCK bit from being cleared after it has been set once. If IOLOCK remains set, the register unlock procedure does not execute, and the PPS control registers cannot be written to. The only way to clear the bit and reenable peripheral remapping is to perform a device Reset.

In the default (unprogrammed) state, IOL1WAY is set, restricting users to one write session.

## 12.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications.

FIGURE 12-1: TIMER1 BLOCK DIAGRAM

The following modes are supported:

- · Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

## 12.1 Additional Supported Features

- · Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

Figure 12-1 illustrates a general block diagram of Timer1.



NOTES:

## PIC32MX1XX/2XX 28/36/44-PIN FAMILY

#### REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	-	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	_	—
15.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7.0	AUDEN <sup>(1)</sup>	—	—	—	AUDMONO <sup>(1,2)</sup>	—	AUDMOD	)<1:0> <sup>(1,2)</sup>

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit
  - 1 = Data from RX FIFO is sign extended
  - 0 = Data from RX FIFO is not sign extended
- bit 14-13 Unimplemented: Read as '0'
- bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
  - 1 = Frame Error overflow generates error events
  - 0 = Frame Error does not generate error events
- bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit
  - 1 = Receive overflow generates error events
    - 0 = Receive overflow does not generate error events
- bit 10 SPITUREN: Enable Interrupt Events via SPITUR bit
  - 1 = Transmit underrun generates error events
  - 0 = Transmit underrun does not generate error events
- bit 9 IGNROV: Ignore Receive Overflow bit (for Audio Data Transmissions)
  - 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
     0 = A ROV is a critical error that stops SPI operation
- bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
  - 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
  - 0 = A TUR is a critical error that stops SPI operation
- bit 7 AUDEN: Enable Audio CODEC Support bit<sup>(1)</sup>
- 1 = Audio protocol enabled
  - 0 = Audio protocol disabled
- bit 6-5 Unimplemented: Read as '0'
- bit 3 AUDMONO: Transmit Audio Data Format bit<sup>(1,2)</sup>
  - 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
  - 0 = Audio data is stereo
- bit 2 Unimplemented: Read as '0'
- bit 1-0 AUDMOD<1:0>: Audio Protocol Mode bit<sup>(1,2)</sup>
  - 11 = PCM/DSP mode
  - 10 = Right-Justified mode
  - 01 = Left-Justified mode
  - $00 = I^2S \mod$
- **Note 1:** This bit can only be written when the ON bit = 0.
  - 2: This bit is only valid for AUDEN = 1.

#### TABLE 26-2: PERIPHERAL MODULE DISABLE REGISTER MAP

ess											Bits								\$
Virtual Addr (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F0.40		31:16	—	—	_	_	—	_	_	—	_	_	_		_	—		—	0000
F240	FIVIDI	15:0	_	_		CVRMD	_		_	CTMUMD	—	_			_	-		AD1MD	0000
5050		31:16	_	-			_		_	—	_	_			_	-		_	0000
F230	FIVIDZ	15:0	_	_	_	_	—	_	_	—	_	—	_	_	_	CMP3MD	CMP2MD	CMP1MD	0000
E260	PMD3	31:16	—	—	_	_	—	_	—	—	—	—	_	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
F200	T WID5	15:0	—	—	_	_	—	_	—	—	—	—	_	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	0000
E270		31:16	—	—	_	_	—	_	—	—	—	—	_	_	—	—	-	—	0000
F270		15:0	—	—	_	_	—	_	—	—	—	—	_	T5MD	T4MD	T3MD	T2MD	T1MD	0000
E200		31:16	—	—	_	_	—	_	—	USB1MD	—	—	_	_	—	—	I2C1MD	I2C1MD	0000
F200	T WID5	15:0	—	—	_	_	—	_	SPI2MD	SPI1MD	—	—	_	_	—	—	U2MD	U1MD	0000
E200	PMD6	31:16	_	_	_	_	_	_	_	—	_	_	-	_	_	_	-	PMPMD	0000
F290		15:0	_	_	_	_	_	_	_	—	_	_	-	_	_	_	REFOMD	RTCCMD	0000

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

## 27.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX 28/36/44-pin Family devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX 28/36/44-pin Family family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 30.1 "DC Characteristics"**.

Note:	It is important that the low-ESR capacitor
	is placed as close as possible to the VCAP
	pin.

## 27.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

## 27.3.2 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX 28/36/44-pin Family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 30.1 "DC Characteristics"**.

## FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



## 27.4 **Programming and Diagnostics**

PIC32MX1XX/2XX 28/36/44-pin Family devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

Figure 27-2 illustrates a block diagram of the programming, debugging, and trace ports.





NOTES:

## PIC32MX1XX/2XX 28/36/44-PIN FAMILY





#### TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

АС СНА	RACTER	ISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industria $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param. No.	Symbol	Charact	eristics	Min. <sup>(1)</sup>	Max.	Units	Conditions		
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)	_	μs	_		
			400 kHz mode	Трв * (BRG + 2)	_	μs	—		
			1 MHz mode <b>(Note 2)</b>	Трв * (BRG + 2)	—	μs	_		
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	—	μS	—		
			400 kHz mode	Трв * (BRG + 2)	—	μS	—		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS	_		
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be		
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF		
			1 MHz mode (Note 2)	_	100	ns			
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be		
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF		
			1 MHz mode (Note 2)	—	300	ns			
IM25	TSU:DAT	Data Input	100 kHz mode	250		ns			
		Setup Time	400 kHz mode	100	—	ns			
			1 MHz mode (Note 2)	100	—	ns			
IM26	THD:DAT	Data Input	100 kHz mode	0	—	μS	—		
		Hold Time	400 kHz mode	0	0.9	μS			
			1 MHz mode (Note 2)	0	0.3	μS			
IM30	TSU:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)	—	μS	Only relevant for		
		Setup Time	400 kHz mode	Трв * (BRG + 2)	—	μS	Repeated Start		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs			
IM31	THD:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)		μs	After this period, the		
		Hold Time	400 kHz mode	Трв * (BRG + 2)	—	μS	first clock pulse is		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	generaleu		
IM33	Tsu:sto	Stop Condition	100 kHz mode	Трв * (BRG + 2)		μs			
		Setup Time	400 kHz mode	Трв * (BRG + 2)		μs			
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS			
IM34	THD:STO	Stop Condition	100 kHz mode	Трв * (BRG + 2)		ns	—		
		Hold Time	400 kHz mode	Трв * (BRG + 2)		ns			
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	ns			

**Note 1:** BRG is the value of the  $I^2C$  Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**3:** The typical value for this parameter is 104 ns.

### TABLE 30-34: ADC MODULE SPECIFICATIONS

	AC CHAF	ACTERISTICS	Standard Operating Conditions (see Note 5): 2.5V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions		
ADC Ac	curacy – N	leasurements with Inter	nal VREF+/V	REF-					
AD20d	Nr	Resolution		10 data bits	6	bits	(Note 3)		
AD21d	INL	Integral Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)		
AD22d	DNL	Differential Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Notes 2,3)		
AD23d	Gerr	Gain Error	> -4	_	< 4	LSb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)		
AD24d	Eoff	Offset Error	> -2	_	< 2	Lsb	VINL = AVSS = 0V, AVDD = 2.5V to 3.6V (Note 3)		
AD25d	—	Monotonicity	—	—	—		Guaranteed		
Dynami	c Performa	ance	·				·		
AD32b	SINAD	Signal to Noise and Distortion	55	58.5		dB	(Notes 3,4)		
AD34b	ENOB	Effective Number of bits	9.0	9.5		bits	(Notes 3,4)		

**Note 1:** These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

4: Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

## PIC32MX1XX/2XX 28/36/44-PIN FAMILY



### FIGURE 30-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





	Units	N	<b>IILLIMETER</b>	S		
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	N		28			
Pitch	е		1.27 BSC			
Overall Height	A	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E		10.30 BSC			
Molded Package Width	E1		7.50 BSC			
Overall Length	D		17.90 BSC			
Chamfer (Optional)	h	0.25	-	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1		1.40 REF			
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	-	15°		

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

# 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS	6
Dimension	n Limits	MIN	NOM	MAX
Number of Pins	Ν		28	
Pitch	е		0.65 BSC	
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	К	0.20	-	-

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B