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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx110f016ct-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

			_0,0	Rem	annah	le Pe	rinhe	rals			/		1				1	l	1
Device	Pins	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Pins	Timers ⁽²⁾ /Capture/Compare	UART	SPI/I ² S	External Interrupts ⁽³⁾	Analog Comparators	USB On-The-Go (OTG)	I ² C	dWd	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels	RTCC	I/O Pins	JTAG	Packages
PIC32MX110F016B	28	16+3	4	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX110F016C	36	16+3	4	24	5/5/5	2	2	5	3	Ν	2	Υ	4/0	Y	12	Y	25	Y	VTLA
PIC32MX110F016D	44	16+3	4	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX120F032B	28	32+3	8	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX120F032C	36	32+3	8	24	5/5/5	2	2	5	3	Ν	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX120F032D	44	32+3	8	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX130F064B	28	64+3	16	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX130F064C	36	64+3	16	24	5/5/5	2	2	5	3	Ν	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX130F064D	44	64+3	16	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX150F128B	28	128+3	32	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX150F128C	36	128+3	32	24	5/5/5	2	2	5	3	Ν	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX150F128D	44	128+3	32	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX130F256B	28	256+3	16	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX130F256D	44	256+3	16	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX170F256B	28	256+3	64	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX170F256D	44	256+3	64	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN

TABLE 1: PIC32MX1XX 28/36/44-PIN GENERAL PURPOSE FAMILY FEATURES

Note 1: This device features 3 KB of boot Flash memory.

2: Four out of five timers are remappable.

3: Four out of five external interrupts are remappable.

TABLE 5: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES

28-PIN QFN (TOP VIEW)^(1,2,3.4)

PIC32MX110F016B PIC32MX120F032B PIC32MX130F064B PIC32MX130F256B PIC32MX150F128B PIC32MX170F256B

28

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	16	Vss
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	18	PGED2/RPB10/CTED11/PMD2/RB10
5	Vss	19	PGEC2/TMS/RPB11/PMD1/RB11
6	OSC1/CLKI/RPA2/RA2	20	AN12/PMD0/RB12
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	Vdd	24	AVss
11	PGED3/RPB5/PMD7/RB5	25	AVdd
12	PGEC3/RPB6/PMD6/RB6	26	MCLR
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	VREF-/CVREF-/AN1/RPA1/CTED2/RA1
Note	1: The RPn pins can be used by remappable peripherals. See T	able 1 for th	e available peripherals and Section 11.3 "Peripheral Pin

1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES

28-PIN QFN (TOP VIEW)^(1,2,3,4)

PIC32MX210F016B PIC32MX220F032B PIC32MX230F064B PIC32MX230F256B PIC32MX250F128B PIC32MX250F128B

28

1

Pin #	Full Pin Name	Pin #	Full Pin Name					
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9					
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	16	Vss					
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	VCAP					
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	PGED2/RPB10/D+/CTED11/RB10					
5	Vss	19	PGEC2/RPB11/D-/RB11					
6	OSC1/CLKI/RPA2/RA2	20	VUSB3V3					
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13					
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14					
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15					
10	VDD	24	AVss					
11	TMS/RPB5/USBID/RB5	25	AVDD					
12	VBUS	26	MCLR					
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0					
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1					
Note	te 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin							

1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

TABLE 10: PIN NAMES FOR 44-PIN USB DEVICES

44-PIN QFN (TOP VIEW)^(1,2,3,5)

PIC32MX210F016D PIC32MX220F032D PIC32MX230F064D PIC32MX230F256D PIC32MX250F128D PIC32MX270F256D

			44 1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4/TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4/TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVdd	39	Vss
18	MCLR	40	VDD
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	VBUS
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

TABLE 11: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

44-PIN TQFP (TOP VIEW)^(1,2,3,5)

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

44

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1		22	
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/C1ED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	Vdd
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	Vdd
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

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PIC32MX1XX/2XX 28/36/44-PIN FAMILY

		Pin Nu	mber ⁽¹⁾	-			
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
SDA1	15	18	19	1	I/O	ST	Synchronous serial data input/output for I2C1
SCL2	4	7	2	24	I/O	ST	Synchronous serial clock input/output for I2C2
SDA2	3	6	1	23	I/O	ST	Synchronous serial data input/output for I2C2
TMS	19 ⁽²⁾ 11 ⁽³⁾	22 ⁽²⁾ 14 ⁽³⁾	25 ⁽²⁾ 15 ⁽³⁾	12	I	ST	JTAG Test mode select pin
TCK	14	17	18	13	I	ST	JTAG test clock input pin
TDI	13	16	17	35	0	—	JTAG test data input pin
TDO	15	18	19	32	0	—	JTAG test data output pin
RTCC	4	7	2	24	0	ST	Real-Time Clock alarm output
CVREF-	28	3	34	20	I	Analog	Comparator Voltage Reference (low)
CVREF+	27	2	33	19		Analog	Comparator Voltage Reference (high)
CVREFOUT	22	25	28	14	0	Analog	Comparator Voltage Reference output
C1INA	4	7	2	24	I	Analog	Comparator Inputs
C1INB	3	6	1	23		Analog	1
C1INC	2	5	36	22	I	Analog	1
C1IND	1	4	35	21	I	Analog	1
C2INA	2	5	36	22	I	Analog	1
C2INB	1	4	35	21	I	Analog	1
C2INC	4	7	2	24	I	Analog	1
C2IND	3	6	1	23	I	Analog	
C3INA	23	26	29	15	I	Analog	
C3INB	22	25	28	14	I	Analog	
C3INC	27	2	33	19	I	Analog	
C3IND	1	4	35	21	I	Analog	
C10UT	PPS	PPS	PPS	PPS	0		Comparator Outputs
C2OUT	PPS	PPS	PPS	PPS	0	—]
C3OUT	PPS	PPS	PPS	PPS	0]
Legend:	CMOS = CI ST = Schmi	MOS compa itt Trigger in	atible input	or output MOS levels		Analog = O = Outp	Analog input P = Power out I = Input

DINOUT 1/0 DECODIDITIONS (CONTINUED)

TTL = TTL input buffer PPS = Peripheral Pin Select Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

— = N/A



FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX170/270 DEVICES (64 KB RAM, 256 KB FLASH)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
31.24	CHSSA<31:24>											
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
23:10	CHSSA<23:16>											
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
15:8	CHSSA<15:8>											
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
				CHSSA	<7:0>							

REGISTER 9-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 bit 31-0
 CHSSA<31:0> Channel Source Start Address bits

 Channel source start address.

 Note: This must be the physical address of the source.

REGISTER 9-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24				CHDSA<	31:24>						
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10	CHDSA<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHDSA<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0		CHDSA<7:0>									

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits Channel destination start address.

 $\ensuremath{\textbf{Note:}}$ This must be the physical address of the destination.

12.0 TIMER1

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 14. "Timers"** (DS60001105), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This family of PIC32 devices features one synchronous/asynchronous 16-bit timer that can operate as a free-running interval timer for various timing applications and counting external events. This timer can also be used with the Low-Power Secondary Oscillator (Sosc) for Real-Time Clock (RTC) applications.

FIGURE 12-1: TIMER1 BLOCK DIAGRAM

The following modes are supported:

- · Synchronous Internal Timer
- Synchronous Internal Gated Timer
- Synchronous External Timer
- Asynchronous External Timer

12.1 Additional Supported Features

- · Selectable clock prescaler
- Timer operation during CPU Idle and Sleep mode
- Fast bit manipulation using CLR, SET and INV registers
- Asynchronous mode can be used with the Sosc to function as a Real-Time Clock (RTC)

Figure 12-1 illustrates a general block diagram of Timer1.



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
15.6	ON ⁽¹⁾	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
7:0	TGATE		TCKP	S<1:0>		TSYNC	TCS	_

REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Timer On bit⁽¹⁾
 - 1 = Timer is enabled
 - 0 = Timer is disabled

bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit

- 1 = Writes to Timer1 are ignored until pending write operation completes
- 0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

- 1 = Asynchronous write to the Timer1 register in progress
- 0 = Asynchronous write to Timer1 register is complete
- In Synchronous Timer mode:

This bit is read as '0'.

- bit 10-8 **Unimplemented:** Read as '0'
- bit 7 TGATE: Timer Gated Time Accumulation Enable bit
 - When TCS = 1:

This bit is ignored.

When TCS = 0:

- 1 = Gated time accumulation is enabled
- 0 = Gated time accumulation is disabled

bit 6 Unimplemented: Read as '0'

bit 5-4 TCKPS<1:0>: Timer Input Clock Prescale Select bits

- 11 = 1:256 prescale value
- 10 = 1:64 prescale value
- 01 = 1:8 prescale value
- 00 = 1:1 prescale value
- **Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

INPUT CAPTURE 15.0

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 15. "Input Capture" (DS60001122), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Input Capture module is useful in applications requiring frequency (period) and pulse measurement.

The Input Capture module captures the 16-bit or 32-bit value of the selected Time Base registers when an event occurs at the ICx pin. The following events cause capture events:

- · Simple capture event modes:
 - Capture timer value on every rising and falling edge of input at ICx pin
 - Capture timer value on every edge (rising and falling)
 - Capture timer value on every edge (rising and falling), specified edge first.

- Prescaler capture event modes:
 - Capture timer value on every 4th rising edge of input at ICx pin
 - Capture timer value on every 16th rising edge of input at ICx pin

Each input capture channel can select between one of two 16-bit timers (Timer2 or Timer3) for the time base, or two 16-bit timers (Timer2 and Timer3) together to form a 32-bit timer. The selected timer can use either an internal or external clock.

Other operational features include:

- · Device wake-up from capture pin during Sleep and Idle modes
- · Interrupt on input capture event
- 4-word FIFO buffer for capture values (interrupt optionally generated after 1, 2, 3, or 4 buffer locations are filled)
- · Input capture can also be used to provide additional sources of external interrupts

Figure 15-1 illustrates a general block diagram of the Input Capture module.



REGIST	ER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)				
bit 17	SPIFE: Frame Sync Pulse Edge Select bit (Framed SPI mode only)				
	1 = Frame synchronization pulse coincides with the first bit clock				
bit 16	Frame synchronization pulse precedes the first bit clock ENHBLIE: Enhanced Buffer Enable bit ⁽²⁾				
Sit 10	1 = Enhanced Buffer mode is enabled				
	0 = Enhanced Buffer mode is disabled				
bit 15	ON: SPI Peripheral On bit ⁽¹⁾				
	1 = SPI Peripheral is enabled				
hit 14	Unimplemented: Read as '0'				
bit 13	SIDL: Stop in Idle Mode bit				
	1 = Discontinue module operation when the device enters Idle mode				
	0 = Continue module operation when the device enters Idle mode				
bit 12	DISSDO: Disable SDOx pin bit				
	1 = SDOx pin is not used by the module. Pin is controlled by associated PORT register $0 = SDOx pin is controlled by the module$				
bit 11-10	MODE<32.16>: 32/16-Bit Communication Select bits				
	When AUDEN = 1:				
	MODE32 MODE16 Communication				
	1 1 24-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame				
	1 0 32-bit Data, 32-bit FIFO, 32-bit Channel/64-bit Frame				
	0 0 16-bit Data, 16-bit FIFO, 16-bit Channel/32-bit Frame				
	When AUDEN = 0:				
	MODE32 MODE16 Communication				
	1 x 32-bit				
	0 0 8-bit				
bit 9	SMP: SPI Data Input Sample Phase bit				
	Master mode (MSTEN = 1):				
	1 = Input data sampled at end of data output time				
	Slave mode (MSTEN = 0):				
	SMP value is ignored when SPI is used in Slave mode. The module always uses SMP = 0.				
	To write a '1' to this bit, the MSTEN value = 1 must first be written.				
bit 8	CKE: SPI Clock Edge Select bit ⁽³⁾				
	1 = Serial output data changes on transition from active clock state to Idle clock state (see the CKP bit)				
bit 7	SSEN: Slave Select Enable (Slave mode) bit				
bit i	1 = SSx pin used for Slave mode				
	$0 = \overline{SSx}$ pin not used for Slave mode, pin controlled by port function.				
bit 6	CKP: Clock Polarity Select bit ⁽⁴⁾				
	1 = Idle state for clock is a high level; active state is a low level				
Note 1:	When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in				
	the SYSCLK cycle immediately following the instruction that clears the module's ON bit.				
2:	This bit can only be written when the ON bit = 0.				
3:	I his bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).				
4:	When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value				
	of CKP.				

2

18.0 INTER-INTEGRATED CIRCUIT (I²C)

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 24. "Inter-
	Integrated Circuit (I ² C)" (DS60001116),
	which is available from the Documentation
	> Reference Manual section of the Micro-
	chip PIC32 web site
	(www.microchip.com/pic32).

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard. Figure 18-1 illustrates the I^2C module block diagram.

Each I^2C module has a 2-pin interface: the SCLx pin is clock and the SDAx pin is data.

Each I²C module offers the following key features:

- I²C interface supporting both master and slave operation
- I²C Slave mode supports 7-bit and 10-bit addressing
- I²C Master mode supports 7-bit and 10-bit addressing
- I²C port allows bidirectional transfers between master and slaves
- Serial clock synchronization for the I²C port can be used as a handshake mechanism to suspend and resume serial transfer (SCLREL control)
- I²C supports multi-master operation; detects bus collision and arbitrates accordingly
- · Provides support for address bit masking

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)

- bit 5-4 **Unimplemented:** Read as '0'
- bit 3 RTCWREN: RTC Value Registers Write Enable bit⁽⁴⁾
 - 1 = RTC Value registers can be written to by the user
 - 0 = RTC Value registers are locked out from being written to by the user
- bit 2 RTCSYNC: RTCC Value Registers Read Synchronization bit
 - 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read
 If the register is read twice and results in the same data, the data can be assumed to be valid
 - 0 = RTC Value registers can be read without concern about a rollover ripple
- bit 1 HALFSEC: Half-Second Status bit⁽⁵⁾
 - 1 = Second half period of a second
 - 0 = First half period of a second
- bit 0 **RTCOE:** RTCC Output Enable bit
 - 1 = RTCC clock output enabled clock presented onto an I/O
 - 0 = RTCC clock output disabled
- **Note 1:** The ON bit is only writable when RTCWREN = 1.
 - 2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - **3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.
 - 4: The RTCWREN bit can be set only when the write sequence is enabled.
 - 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- · MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- · Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

TABLE 30-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Comments
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	_		10	μs	See Note 1
D313	D313 DACREFH	CVREF Input Voltage Reference Range	AVss	—	AVDD	V	CVRSRC with CVRSS = 0
			VREF-	—	VREF+	V	CVRSRC with CVRSS = 1
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size
			0.25 x DACREFH	—	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size
D315	DACRES	Resolution	—	—	DACREFH/24	-	CVRCON <cvrr> = 1</cvrr>
			_	—	DACREFH/32	_	CVRCON <cvrr> = 0</cvrr>
D316	DACACC	Absolute Accuracy ⁽²⁾		_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>
			—	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>

Note 1: Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

2: These parameters are characterized but not tested.

TABLE 30-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHARACTERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ -40^\circ C \leq TA \leq +105^\circ C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.







PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

Revision J (April 2016)

This revision includes the following major changes as described in Table A-8, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-8: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	The PIC32MX270FDB device and Note 4 were added to TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features".
2.0 "Guidelines for Getting Started with 32-bit MCUs"	EXAMPLE 2-1: "Crystal Load Capacitor Calculation" was updated.
30.0 "Electrical Characteristics"	Parameter DO50a (Csosc) was removed from the Capacitive Loading Requirements on Output Pins AC Characteristics (see Table 30-16).
"Product Identification System"	The device mapping was updated to include type B for Software Targeting.