What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

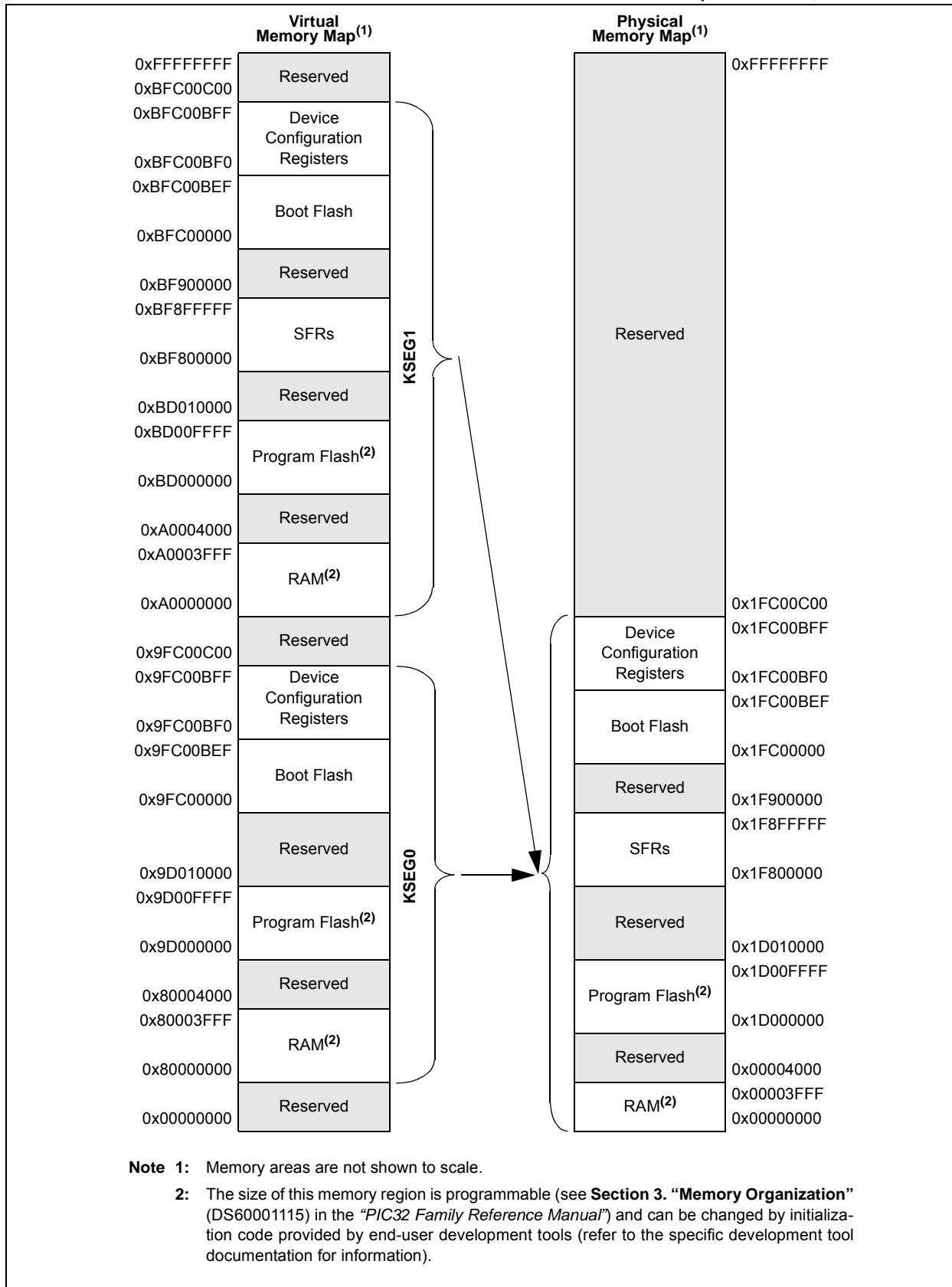| Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx110f016d-i-ml

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES

28-PIN QFN (TOP VIEW)[1,2,3,4]

PIC32MX210F016B
PIC32MX220F032B
PIC32MX230F064B
PIC32MX230F256B
PIC32MX250F128B
PIC32MX270F256B

28   1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	16	V_{SS}
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	V_{CAP}
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	PGED2/RPB10/D+/CTED11/RB10
5	V_{SS}	19	PGEC2/RPB11/D-/RB11
6	OSC1/CLKI/RPA2/RA2	20	V_{USB3V3}
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CV$_{REFOUT}$/AN10/C3INB/RPB14/V_{BUSON}/SCK1/CTED5/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	V_{DD}	24	AV$_{SS}$
11	TMS/RPB5/USBID/RB5	25	AV$_{DD}$
12	V_{BUS}	26	$\overline{MCLR}$
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/V$_{REF}$+/CV$_{REF}$+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/V$_{REF}$-/CV$_{REF}$-/AN1/RPA1/CTED2/PMD6/RA1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.

4: Shaded pins are 5V tolerant.

FIGURE 4-3:   MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 64 KB FLASH)

Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

8.1 Oscillator Control Regiters

TABLE 8-1: OSCILLATOR CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>			x1xx[2]
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK[3]	SLOCK	SLPEN	CF	UFRCEN[3]	SOSCEN	OSWEN	xxxx[2]
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
F020	REFOCON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
F030	REFOTRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This bit is only available on PIC32MX2XX devices.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

9.1 DMA Control Registers

TABLE 9-1: DMA GLOBAL REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3000	DMACON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	—	SUSPEND	DMABUSY	—	—	—	—	—	—	—	—	—	—	—	0000
3010	DMASTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RDWR	DMACH<2:0>[2]			0000
3020	DMAADDR	31:16	DMAADDR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

TABLE 9-2: DMA CRC REGISTER MAP

Virtual Address (BF88_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
3030	DCRCCON	31:16	—	—	BYTO<1:0>		WBO	—	—	BITO	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	PLEN<4:0>					CRCEN	CRCAPP	CRCTYP	—	—	CRCCH<2:0>			0000
3040	DCRCDATA	31:16	DCRCDATA<31:0>																0000
		15:0																	0000
3050	DCRCXOR	31:16	DCRCXOR<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 10-6: U1IR: USB INTERRUPT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R/WC-0, HS	R-0	R/WC-0, HS
	STALLIF	ATTACHIF[1]	RESUMEIF[2]	IDLEIF	TRNIF[3]	SOFIF	UERRIF[4]	URSTIF[5]
								DETACHIF[6]

Legend:		
	WC = Write '1' to clear	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7   **STALLIF:** STALL Handshake Interrupt bit
          1 = In Host mode a STALL handshake was received during the handshake phase of the transaction
          In Device mode a STALL handshake was transmitted during the handshake phase of the transaction
          0 = STALL handshake has not been sent

bit 6   **ATTACHIF:** Peripheral Attach Interrupt bit[1]
          1 = Peripheral attachment was detected by the USB module
          0 = Peripheral attachment was not detected

bit 5   **RESUMEIF:** Resume Interrupt bit[2]
          1 = K-State is observed on the D+ or D- pin for 2.5 µs
          0 = K-State is not observed

bit 4   **IDLEIF:** Idle Detect Interrupt bit
          1 = Idle condition detected (constant Idle state of 3 ms or more)
          0 = No Idle condition detected

bit 3   **TRNIF:** Token Processing Complete Interrupt bit[3]
          1 = Processing of current token is complete; a read of the U1STAT register will provide endpoint information
          0 = Processing of current token not complete

bit 2   **SOFIF:** SOF Token Interrupt bit
          1 = SOF token received by the peripheral or the SOF threshold reached by the host
          0 = SOF token was not received nor threshold reached

bit 1   **UERRIF**: USB Error Condition Interrupt bit[4]
          1 = Unmasked error condition has occurred
          0 = Unmasked error condition has not occurred

bit 0   **URSTIF:** USB Reset Interrupt bit (Device mode)[5]
          1 = Valid USB Reset has occurred
          0 = No USB Reset has occurred
          DETACHIF: USB Detach Interrupt bit (Host mode)[6]
          1 = Peripheral detachment was detected by the USB module
          0 = Peripheral detachment was not detected

Note 1:   This bit is valid only if the HOSTEN bit is set (see Register 10-11), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.

   2:   When not in Suspend mode, this interrupt should be disabled.

   3:   Clearing this bit will cause the STAT FIFO to advance.

   4:   Only error conditions enabled through the U1EIE register will set this bit.

   5:   Device mode.

   6:   Host mode.

REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN	DEVADDR<6:0>						

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8   **Unimplemented:** Read as '0'

bit 7   **LSPDEN:** Low-Speed Enable Indicator bit
- 1 = Next token command to be executed at Low-Speed
- 0 = Next token command to be executed at Full-Speed

bit 6-0   **DEVADDR<6:0>:** 7-bit USB Device Address bits

REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
	FRML<7:0>							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8   **Unimplemented:** Read as '0'

bit 7-0   **FRML<7:0>:** The 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

REGISTER 17-2: **SPIxCON2: SPI CONTROL REGISTER 2**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN[1]	—	—	—	AUDMONO[1,2]	—	AUDMOD<1:0>[1,2]	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit

1 = Data from RX FIFO is sign extended
0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit

1 = Frame Error overflow generates error events
0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit

1 = Receive overflow generates error events
0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit

1 = Transmit underrun generates error events
0 = Transmit underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)

1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error that stops SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)

1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error that stops SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit[1]

1 = Audio protocol enabled
0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit[1,2]

1 = Audio data is mono (Each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit[1,2]

11 = PCM/DSP mode
10 = Right-Justified mode
01 = Left-Justified mode
00 = I^{2}S mode

Note 1: This bit can only be written when the ON bit = 0.
 2: This bit is only valid for AUDEN = 1.

REGISTER 18-1:   I2CxCON: I²C CONTROL REGISTER (CONTINUED)

bit 7   **GCEN:** General Call Enable bit (when operating as I²C slave)

1 = Enable interrupt when a general call address is received in the I2CxRSR
(module is enabled for reception)
0 = General call address is disabled

bit 6   **STREN:** SCLx Clock Stretch Enable bit (when operating as I²C slave)

Used in conjunction with SCLREL bit.
1 = Enable software or receive clock stretching
0 = Disable software or receive clock stretching

bit 5   **ACKDT:** Acknowledge Data bit (when operating as I²C master, applicable during master receive)

Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Send a NACK during an Acknowledge sequence
0 = Send an ACK during an Acknowledge sequence

bit 4   **ACKEN:** Acknowledge Sequence Enable bit (when operating as I²C master, applicable during master receive)

1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit.
Hardware clear at end of master Acknowledge sequence.
0 = Acknowledge sequence not in progress

bit 3   **RCEN:** Receive Enable bit (when operating as I²C master)

1 = Enables Receive mode for I²C. Hardware clear at end of eighth bit of master receive data byte.
0 = Receive sequence not in progress

bit 2   **PEN:** Stop Condition Enable bit (when operating as I²C master)

1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.
0 = Stop condition not in progress

bit 1   **RSEN:** Repeated Start Condition Enable bit (when operating as I²C master)

1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of
master Repeated Start sequence.
0 = Repeated Start condition not in progress

bit 0   **SEN:** Start Condition Enable bit (when operating as I²C master)

1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.
0 = Start condition not in progress

Note 1:   When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the
SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 20-5: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E

Legend:		HSC = Set by Hardware; Cleared by Software	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **IBF:** Input Buffer Full Status bit

1 = All writable input buffer registers are full
0 = Some or all of the writable input buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit

1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IBxF:** Input Buffer 'x' Status Full bits

1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
0 = Input Buffer does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit

1 = All readable output buffer registers are empty
0 = Some or all of the readable output buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit

1 = A read occurred from an empty output byte buffer (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits

1 = Output buffer is empty (writing data to the buffer will clear this bit)
0 = Output buffer contains data that has not been transmitted

REGISTER 22-1: AD1CON1: ADC CONTROL REGISTER 1 (CONTINUED)

bit 4 **CLRASAM:** Stop Conversion Sequence bit (when the first ADC interrupt is generated)

1 = Stop conversions when the first ADC interrupt is generated. Hardware clears the ASAM bit when the ADC interrupt is generated.

0 = Normal operation, buffer contents will be overwritten by the next conversion sequence

bit 3 **Unimplemented:** Read as '0'

bit 2 **ASAM:** ADC Sample Auto-Start bit

1 = Sampling begins immediately after last conversion completes; SAMP bit is automatically set.

0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADC Sample Enable bit[2]

1 = The ADC sample and hold amplifier is sampling

0 = The ADC sample/hold amplifier is holding

When ASAM = 0, writing '1' to this bit starts sampling.

When SSRC = 000, writing '0' to this bit will end sampling and start conversion.

bit 0 **DONE:** Analog-to-Digital Conversion Status bit[3]

1 = Analog-to-digital conversion is done

0 = Analog-to-digital conversion is not done or has not started

Clearing this bit will not affect any operation in progress.

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: If ASAM = 0, software can write a '1' to start sampling. This bit is automatically set by hardware if ASAM = 1. If SSRC = 0, software can write a '0' to end sampling and start conversion. If SSRC ≠ '0', this bit is automatically cleared by hardware to end sampling and start conversion.

3: This bit is automatically set by hardware when analog-to-digital conversion is complete. Software can write a '0' to clear this bit (a write of '1' is not allowed). Clearing this bit does not affect any operation already in progress. This bit is automatically cleared by hardware at the start of a new conversion.

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NB	—	—	—	CH0SB<3:0>			
23:16	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	CH0NA	—	—	—	CH0SA<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **CH0NB:** Negative Input Select bit for Sample B

    1 = Channel 0 negative input is AN1
    0 = Channel 0 negative input is V$_{REFL}$

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **CH0SB<3:0>:** Positive Input Select bits for Sample B

    1111 = Channel 0 positive input is Open[1]
    1110 = Channel 0 positive input is IV$_{REF}$[2]
    1101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)[3]
    1100 = Channel 0 positive input is AN12[4]
    •
    •
    •
    0001 = Channel 0 positive input is AN1
    0000 = Channel 0 positive input is AN0

bit 23 **CH0NA:** Negative Input Select bit for Sample A Multiplexer Setting[2]

    1 = Channel 0 negative input is AN1
    0 = Channel 0 negative input is V$_{REFL}$

bit 22-20 **Unimplemented:** Read as '0'

bit 19-16 **CH0SA<3:0>:** Positive Input Select bits for Sample A Multiplexer Setting

    1111 = Channel 0 positive input is Open[1]
    1110 = Channel 0 positive input is IV$_{REF}$[2]
    1101 = Channel 0 positive input is CTMU temperature (CTMUT)[3]
    1100 = Channel 0 positive input is AN12[4]
    •
    •
    •
    0001 = Channel 0 positive input is AN1
    0000 = Channel 0 positive input is AN0

bit 15-0 **Unimplemented:** Read as '0'

Note 1: This selection is only used with CTMU capacitive and time measurement.
    2: See **Section 24.0 "Comparator Voltage Reference (CV$_{REF}$)"** for more information.
    3: See **Section 25.0 "Charge Time Measurement Unit (CTMU)"** for more information.
    4: AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 25-1.

FIGURE 25-1: CTMU BLOCK DIAGRAM

Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMUT	0	EDG1STAT = EDG2STAT
CTMUI	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
No Connect	1	EDG1STAT = EDG2STAT

NOTES:

26.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 26.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

27.2 Configuration Registers

TABLE 27-1: DEVCFG: DEVICE CONFIGURATION WORD SUMMARY

Virtual Address (BFC0_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0BF0	DEVCFG3	31:16	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—	—	—	—	—	—	—	—	—	xxxx
		15:0	USERID<15:0>																xxxx
0BF4	DEVCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	FPLLODIV<2:0>			xxxx
		15:0	UPLLEN[1]	—	—	—	—	UPLLIDIV<2:0>[1]			—	FPLLMUL<2:0>			—	FPLLIDIV<2:0>			xxxx
0BF8	DEVCFG1	31:16	—	—	—	—	—	—	FWDTWINSZ<1:0>		FWDTEN	WINDIS	—	WDTPS<4:0>					xxxx
		15:0	FCKSM<1:0>		FPBDIV<1:0>		—	OSCIOFNC	POSCMOD<1:0>		IESO	—	FSOSCEN	—	—	FNOSC<2:0>			xxxx
0BFC	DEVCFG0	31:16	—	—	—	CP	—	—	—	BWP	—	—	—	—	—	PWP<8:6>[2]			xxxx
		15:0	PWP<5:0>						—	—	—	—	ICESEL<1:0>		JTAGEN	DEBUG<1:0>			xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: This bit is only available on PIC32MX2XX devices.
2: PWP<8:7> are only available on devices with 256 KB of Flash.

TABLE 27-2: DEVICE ID, REVISION, AND CONFIGURATION SUMMARY

Virtual Address (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets[1]
F220	DEVID	31:16	VER<3:0>				DEVID<27:16>												xxxx[1]
		15:0	DEVID<15:0>																xxxx[1]
F200	CFGCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	IOLOCK	PMDLOCK	—	—	—	—	—	—	—	—	JTAGEN	—	—	TDOEN	000B
F230	SYSKEY[3]	31:16	SYSKEY<31:0>																0000
		15:0																	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: Reset values are dependent on the device variant.

28.0 INSTRUCTION SET

The PIC32MX1XX/2XX family instruction set complies with the MIPS32® Release 2 instruction set architecture. The PIC32 device family does not support the following features:

- Core extend instructions
- Coprocessor 1 instructions
- Coprocessor 2 instructions

Note:	Refer to *"MIPS32® Architecture for Programmers Volume II: The MIPS32® Instruction Set"* at www.imgtec.com for more information.

FIGURE 30-8: **OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**

OCx
(Output Compare
or PWM mode)

OC11 → ← OC10 →

Note: Refer to Figure 30-1 for load conditions.
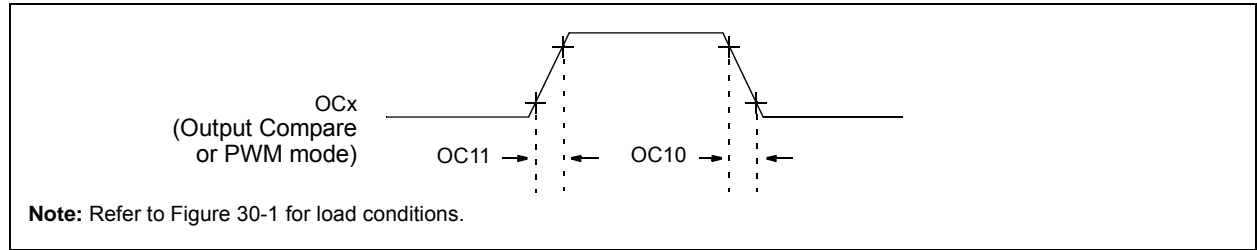
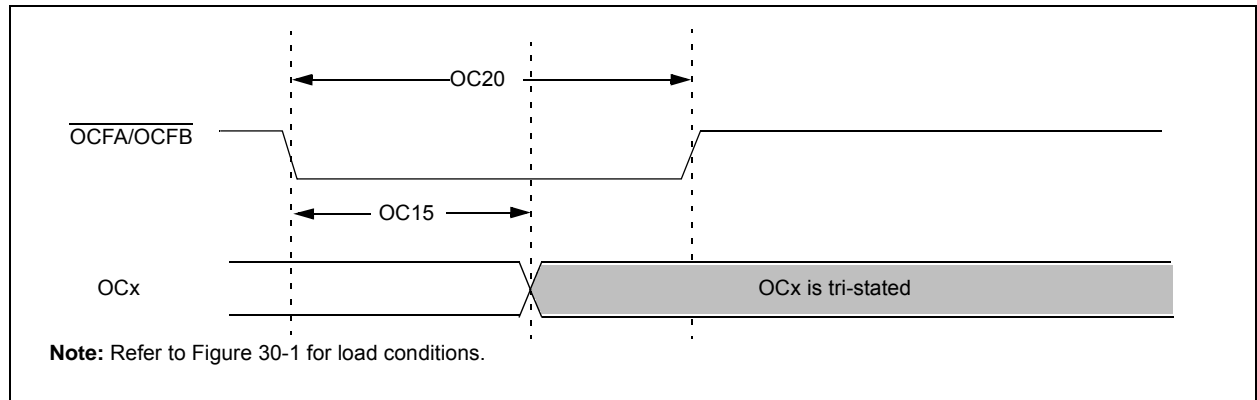**TABLE 30-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typical[2]	Max.	Units	Conditions
OC10	T_{CCF}	OCx Output Fall Time	—	—	—	ns	See parameter DO32
OC11	T_{CCR}	OCx Output Rise Time	—	—	—	ns	See parameter DO31

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-9: **OCx/PWM MODULE TIMING CHARACTERISTICS**

OC20

OCFA/OCFB

OC15

OCx

OCx is tri-stated

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	Symbol	Characteristics[1]	Min	Typical[2]	Max	Units	Conditions
OC15	T_{FD}	Fault Input to PWM I/O Change	—	—	50	ns	—
OC20	T_{FLT}	Fault Input Pulse Width	50	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 30-41: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3):2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
CTMU CURRENT SOURCE							
CTMUI1	IOUT1	Base Range[1]	—	0.55	—	µA	CTMUCON<9:8> = 01
CTMUI2	IOUT2	10x Range[1]	—	5.5	—	µA	CTMUCON<9:8> = 10
CTMUI3	IOUT3	100x Range[1]	—	55	—	µA	CTMUCON<9:8> = 11
CTMUI4	IOUT4	1000x Range[1]	—	550	—	µA	CTMUCON<9:8> = 00
CTMUFV1	VF	Temperature Diode Forward Voltage[1,2]	—	0.598	—	V	TA = +25ºC, CTMUCON<9:8> = 01
			—	0.658	—	V	TA = +25ºC, CTMUCON<9:8> = 10
			—	0.721	—	V	TA = +25ºC, CTMUCON<9:8> = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change[1,2]	—	-1.92	—	mV/ºC	CTMUCON<9:8> = 01
			—	-1.74	—	mV/ºC	CTMUCON<9:8> = 10
			—	-1.56	—	mV/ºC	CTMUCON<9:8> = 11

Note 1: Nominal value at center point of current trim range (CTMUCON<15:10> = 000000).

   2: Parameters are characterized but not tested in manufacturing. Measurements taken with the following conditions:
   - VREF+ = AVDD = 3.3V
   - ADC module configured for conversion speed of 500 ksps
   - All PMD bits are cleared (PMDx = 0)
   - Executing a while(1) statement
   - Device operating from the FRC with no PLL

   3: The CTMU module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]
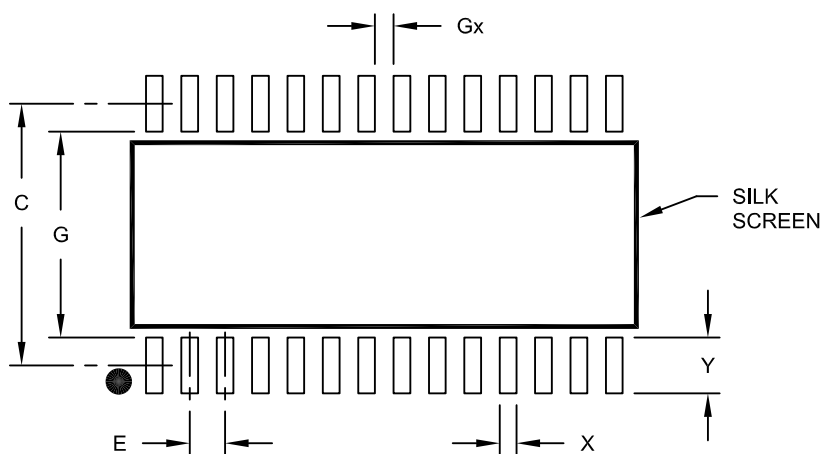
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

APPENDIX A: REVISION HISTORY

Revision A (May 2011)

This is the initial released version of this document.

Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to V$_{CORE}$ have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40ºC to +105ºC) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX230F064B
- PIC32MX130F064C
- PIC32MX230F064C
- PIC32MX130F064D
- PIC32MX230F064D
- PIC32MX150F128B
- PIC32MX250F128B
- PIC32MX150F128C
- PIC32MX250F128C
- PIC32MX150F128D
- PIC32MX250F128D

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2). Added the SPDIP package reference (see Table 1, Table 2, and **"Pin Diagrams"**). Added the new devices to the applicable pin diagrams. Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices.
1.0 "Device Overview"	Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1). Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1).
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).