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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032b-50i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 8: **PIN NAMES FOR 36-PIN USB DEVICES**

36-PIN VTLA (TOP VIEW)^(1,2,3,5)

PIC32MX210F016C

	PIC32MX220F032C PIC32MX230F064C PIC32MX250F128C		
			36
			1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	19	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	20	RPC9/CTED7/RC9
3	PGED4 ⁽⁴⁾ /AN6/RPC0/RC0	21	Vss
4	PGEC4 ⁽⁴⁾ /AN7/RPC1/RC1	22	VCAP
5	VDD	23	Vdd
6	Vss	24	PGED2/RPB10/D+/CTED11/RB10
7	OSC1/CLKI/RPA2/RA2	25	PGEC2/RPB11/D-/RB11
8	OSC2/CLKO/RPA3/PMA0/RA3	26	VUSB3V3
9	SOSCI/RPB4/RB4	27	AN11/RPB13/CTPLS/PMRD/RB13
10	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	28	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14
11	AN12/RPC3/RC3	29	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
12	Vss	30	AVss
13	DD	31	AVdd
14	DD	32	MCLR
15	TMS/RPB5/USBID/RB5	33	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
16	VBUS	34	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1
17	TDI/RPB7/CTED3/PMD5/INT0/RB7	35	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0
18	TCK/RPB8/SCL1/CTED10/PMD4/RB8	36	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1
		L	

Note The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin 1: Select" for restrictions.

Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information. 2:

The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally. 3:

4: This pin function is not available on PIC32MX210F016C and PIC32MX120F032C devices.

5: Shaded pins are 5V tolerant.

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.



FIGURE 1-1: BLOCK DIAGRAM

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB[®] ICD 3 or MPLAB REAL ICETM.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

- "Using MPLAB[®] ICD 3" (poster) (DS50001765)
- *"MPLAB[®] ICD 3 Design Advisory"* (DS50001764)
- "MPLAB[®] REAL ICE™ In-Circuit Debugger User's Guide" (DS50001616)
- "Using MPLAB[®] REAL ICE™ Emulator" (poster) (DS50001749)

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

REGIST	ER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER (CONTINUED)
bit 9-8	IS01<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0
bit 7-5	Unimplemented: Read as '0'
bit 4-2	IP00<2:0>: Interrupt Priority bits
	<pre>111 = Interrupt priority is 7</pre>
	010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled
bit 1-0	IS00<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0
Note:	This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bir definitions.

TABLE 9-3: DMA CHANNELS 0-3 REGISTER MAP (CONTINUED)

ess										Bi	ts								
Virtual Addre (BF88_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
3170	DCH1SSIZ	31:16	_	—		_	_	_	—	—		_	—	_	_	_	_	—	0000
0170	DOITIOOIZ	15:0		i		i			i	CHSSIZ	2<15:0>		t					i	0000
3180	DCH1DSIZ	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
0.00	50115012	15:0								CHDSIZ	Z<15:0>								0000
3190	DCH1SPTR	31:16				_		_		—	—	—	—	—	_	—	—		0000
		15:0								CHSPTI	≺<15:0>								0000
31A0	DCH1DPTR	31:16						_				_	_	_	_	_	_		0000
		10.0									~~15.0>								0000
31B0	DCH1CSIZ	15.0				_	_			CHCSIZ	 7<15:0>		_						0000
		31:16	_		_	_	_	_		_		_	_	_	_	_	_		0000
31C0	DCH1CPTR	15:0								CHCPTI	R<15:0>								0000
	DOLUDAT	31:16	_		_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
31D0	DCH1DAT	15:0	_	_	_	_	_	_	_	_				CHPDA	T<7:0>				0000
2150		31:16	_	_	_	—	_	_	—	_	_	_	_	_	_	_	_	—	0000
SIEU	DCH2CON	15:0	CHBUSY	—	—	—	—	-	—	CHCHNS	CHEN	CHAED	CHCHN	CHAEN	-	CHEDET	CHPR	l<1:0>	0000
31E0	DCH2ECON	31:16	—	_	—	—	—	—	_	—			1	CHAIR	Q<7:0>				OOFF
011 0	DONZEOON	15:0				CHSIR	Q<7:0>				CFORCE	CABORT	PATEN	SIRQEN	AIRQEN	—	—		FF00
3200	DCH2INT	31:16				_	_		—		CHSDIE	CHSHIE	CHDDIE	CHDHIE	CHBCIE	CHCCIE	CHTAIE	CHERIE	0000
		15:0	_		—	—	—	—		—	CHSDIF	CHSHIF	CHDDIF	CHDHIF	CHBCIF	CHCCIF	CHTAIF	CHERIF	0000
3210	DCH2SSA	31:16								CHSSA	<31:0>								0000
		15:0																	0000
3220	DCH2DSA	15.0								CHDSA	<31:0>								0000
		31.16	_			_	_	_		_		_		_	_	_	_		0000
3230	DCH2SSIZ	15.0								CHSSIZ	/<15:0>								0000
		31:16	_	_		_	_	_		_	_	—	_	_	_	_	_	_	0000
3240	DCH2DSIZ	15:0								CHDSIZ	Z<15:0>								0000
0050	DOLIGODITO	31:16	_	_	_	—	_	_		_	_	_	_	_	_	_	_		0000
3250	DCH2SPTR	15:0								CHSPTI	R<15:0>								0000
3260		31:16	—	—	—	—	—	-	—	_	_		_	_	-	-		_	0000
5200		15:0								CHDPT	R<15:0>								0000
3270	DCH2CSI7	31:16		—	—	—	_	—		—	—	—	—	—	—	—	—		0000
00	_ 5.12001L	15:0								CHCSIZ	Z<15:0>								0000

Legend:

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—		—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	_	_	_		_	—	_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	-	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS

REGISTER 10-4: U10TGCON: USB OTG CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	DPP	ULUP	: D+ F	Pull-Up I	Enable	bit	

1 = D+ data line pull-up resistor is enabled
 0 = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit

- It 6 DIMPOLOP: D- Pull-Op Enable bit
 - 1 = D- data line pull-up resistor is enabled
 0 = D- data line pull-up resistor is disabled
- bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
 - 1 = D + data line pull-down resistor is enabled
 - 0 = D + data line pull-down resistor is disabled
- bit 4 **DMPULDWN:** D- Pull-Down Enable bit
 - 1 = D- data line pull-down resistor is enabled
 - 0 = D- data line pull-down resistor is disabled
- bit 3 VBUSON: VBUS Power-on bit
 - 1 = VBUS line is powered
 - 0 = VBUS line is not powered
- bit 2 OTGEN: OTG Functionality Enable bit
 - 1 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
 - 0 = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control
- bit 1 VBUSCHG: VBUS Charge Enable bit
 - 1 = VBUS line is charged through a pull-up resistor
 - 0 = VBUS line is not charged through a resistor
- bit 0 VBUSDIS: VBUS Discharge Enable bit
 - 1 = VBUS line is discharged through a pull-down resistor
 - 0 = VBUS line is not discharged through a resistor

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	JSTATE	SEO	PKTDIS ⁽⁴⁾	LISBDST		DESIME(3)	PPBRST	USBEN ⁽⁴⁾
		SEU	TOKBUSY ^(1,5)	USDKSI		RESUMENT		SOFEN ⁽⁵⁾

REGISTER 10-11: U1CON: USB CONTROL REGISTER

Legend:

3			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit 1 = JSTATE was detected on the USB
 - 0 = No JSTATE was detected on the
- bit 6 **SE0:** Live Single-Ended Zero flag bit 1 = Single-Ended Zero was detected on the USB
 - 0 = No Single-Ended Zero was detected
- bit 5 **PKTDIS:** Packet Transfer Disable bit⁽⁴⁾
 - 1 = Token and packet processing is disabled (set upon SETUP token received)
 - 0 = Token and packet processing is enabled
 - TOKBUSY: Token Busy Indicator bit^(1,5)
 - 1 = Token is being executed by the USB module
 - 0 = No token is being executed

bit 4 USBRST: Module Reset bit⁽⁵⁾

- 1 = USB reset generated
- 0 = USB reset terminated
- bit 3 HOSTEN: Host Mode Enable bit⁽²⁾
 - 1 = USB host capability is enabled
 - 0 = USB host capability is disabled
- bit 2 RESUME: RESUME Signaling Enable bit⁽³⁾
 - 1 = RESUME signaling is activated
 - 0 = RESUME signaling is disabled
- **Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
 - 2: All host control logic is reset any time that the value of this bit is toggled.
 - 3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
 - 4: Device mode.
 - 5: Host mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	—	—		—	—			—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	_	—		_	_			_	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15:8	—	—	-	—	—		-	—	
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
7:0				BDTPTR	H<23:16>				

REGISTER 10-18: U1BDTP2: USB BUFFER DESCRIPTOR TABLE PAGE 2 REGISTER

Legend:R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRH<23:16>:** Buffer Descriptor Table Base Address bits This 8-bit value provides address bits 23 through 16 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23.10	_	—	_	—	—	_	—	—	
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15:8	—	—	—	—	—	—	—	—	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
				BDTPTR	U<31:24>				

REGISTER 10-19: U1BDTP3: USB BUFFER DESCRIPTOR TABLE PAGE 3 REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **BDTPTRU<31:24>:** Buffer Descriptor Table Base Address bits This 8-bit value provides address bits 31 through 24 of the Buffer Descriptor Table base address, defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

11.3 Peripheral Pin Select

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin-count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient workarounds in application code or a complete redesign may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to these I/O pins. PPS is performed in software and generally does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.3.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable port number.

11.3.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digitalonly peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the PPS feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I²C among others. A similar requirement excludes all modules with analog inputs, such as the Analog-to-Digital Converter (ADC).

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin.

Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.3.3 CONTROLLING PERIPHERAL PIN SELECT

PPS features are controlled through two sets of SFRs: one to map peripheral inputs, and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.3.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The [*pin name*]R registers, where [*pin name*] refers to the peripheral pins listed in Table 11-1, are used to configure peripheral input mapping (see Register 11-1). Each register contains sets of 4 bit fields. Programming these bit fields with an appropriate value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field is shown in Table 11-1.

For example, Figure 11-2 illustrates the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT EXAMPLE FOR U1RX



17.1 SPI Control Registers

TABLE 17-1: SPI1 AND SPI2 REGISTER MAP

ess		6								Bi	ts								
Virtual Addr (BF80_#)	Register Name ⁽¹⁾	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
5800	SPI1CON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FI	RMCNT<2:	0>	MCLKSEL	—	_	—	—	—	SPIFE	ENHBUF	0000
3000	SFILCON	15:0	ON	-	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISI	EL<1:0>	0000
E010	QDI1QTAT	31:16	_	_	_		RXE	BUFELM<4:	:0>		_	_	_		TX	BUFELM<4	:0>		0000
0100	SFIISTAI	15:0	—	—	—	FRMERR	SPIBUSY	-	_	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	0008
5020	SDI1BUE	31:16									31.05								0000
5620		15:0								DAIA	51.04								0000
5830	SPI1BRG	31:16	—		—	—	—	—	—	—	—	—	—	—	-	—		—	0000
3030		15:0	—	—	—						E	3RG<12:0>							0000
		31:16	_	—	—	—	—	_	—	—	—	—	—	—	—	—	_	—	0000
5840	SPI1CON2	15:0	SPI SGNEXT	—	—	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	—	—	—	AUD MONO	—	AUDMO	DC<1:0>	0000
	SDISCON	31:16	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FI	RMCNT<2:	0>	MCLKSEL	_	_	_	_	_	SPIFE	ENHBUF	0000
5AUU	SFIZCON	15:0	ON	_	SIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	STXISE	EL<1:0>	SRXISI	EL<1:0>	0000
	CDIPCTAT	31:16		—	—		RXE	BUFELM<4:	:0>		—	_	_		TX	BUFELM<4	:0>		0000
5A10	3F1231AI	15:0		—	—	FRMERR	SPIBUSY	_	—	SPITUR	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	8000
E A 20		31:16									31.05								0000
5AZU	3F12D01	15:0								DAIA	51.0~								0000
EA 20	SDISEDC	31:16	_	—	—	—	_	_	—	—	_	—	—	—	—	—	_	—	0000
5A30		15:0	—		—			-			E	3RG<12:0>		-		-			0000
		31:16	—	-	—	—	-	—	—	-	-	-	—	—	-	—	—	—	0000
5A40	SPI2CON2	15:0	SPI SGNEXT	-	_	FRM ERREN	SPI ROVEN	SPI TUREN	IGNROV	IGNTUR	AUDEN	_	-	_	AUD MONO	_	AUDMO)D<1:0>	0000

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table except SPIxBUF have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER (CONTINUED)

- bit 4 Unimplemented: Read as '0' CS1P: Chip Select 0 Polarity bit⁽²⁾ bit 3 1 = Active-high (PMCS1) $0 = \text{Active-low}(\overline{PMCS1})$ bit 2 Unimplemented: Read as '0' bit 1 WRSP: Write Strobe Polarity bit For Slave Modes and Master mode 2 (MODE<1:0> = 00,01,10): 1 = Write strobe active-high (PMWR) 0 = Write strobe active-low (PMWR) For Master mode 1 (MODE<1:0> = 11): 1 = Enable strobe active-high (PMENB) 0 = Enable strobe active-low (PMENB) bit 0 RDSP: Read Strobe Polarity bit For Slave modes and Master mode 2 (MODE<1:0> = 00,01,10): 1 = Read Strobe active-high (PMRD) $0 = \text{Read Strobe active-low}(\overline{PMRD})$ For Master mode 1 (MODE<1:0> = 11): 1 = Read/write strobe active-high (PMRD/PMWR)
 - 0 = Read/write strobe active-low (PMRD/PMWR)
 - **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.





The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- · On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

- Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.
 - 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator startup delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

26.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid. To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 26-1 for more information.

Note: Disabling a peripheral module while it's ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TARI E 26-1·	PERIPHERAL MODULE DISABLE BITS AND LOCATIONS
TADLL 20-1.	FERIFILICAL MODULE DISABLE DITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
СТМU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Comparator 3	CMP3MD	PMD2<2>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
12C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features" and TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features" for the lists of available peripherals.

2: The module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
31:24	—	—	—	—	—	—	—	—
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
23:10	—	—	—	—	—	FPLLODIV<2:0>		
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
15:8	UPLLEN ⁽¹⁾	—	—	_	_	UF	PLLIDIV<2:0>	.(1)
7.0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
7:0	_	F	PLLMUL<2:0>	•	_	F	PLLIDIV<2:0	>

DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 27-3:

Legend:	r = Reserved bit	P = Programmable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit⁽¹⁾ 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits⁽¹⁾ 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider000 = 1x divider Reserved: Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
 - 111 = 24x multiplier 110 = 21x multiplier
 - 101 = 20x multiplier
 - 100 = 19x multiplier
 - 011 = 18x multiplier
 - 010 = 17x multiplier
 - 001 = 16x multiplier
 - 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.







NOTES:

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units			S
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimensior	Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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