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Details

-XF

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032b-i-ss

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 12: PIN NAMES FOR 44-PIN USB DEVICES

44-PIN TQFP (TOP VIEW)^(1,2,3,5)

PIC32MX210F016D PIC32MX220F032D PIC32MX230F064D PIC32MX230F256D PIC32MX250F128D PIC32MX270F256D

44

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 ⁽⁴⁾ /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 ⁽⁴⁾ /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	VDD
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	VBUS
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX210F016D and PIC32MX220F032D devices.

5: Shaded pins are 5V tolerant.

TABLE 1-1: **PINOUT I/O DESCRIPTIONS**

		Pin Nu	mber ⁽¹⁾								
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description				
AN0	27	2	33	19	Ι	Analog	Analog input channels.				
AN1	28	3	34	20	I	Analog					
AN2	1	4	35	21	I	Analog					
AN3	2	5	36	22	I	Analog					
AN4	3	6	1	23	I	Analog					
AN5	4	7	2	24	I	Analog					
AN6		_	3	25	I	Analog					
AN7		_	4	26	I	Analog					
AN8	—		—	27	I	Analog					
AN9	23	26	29	15	I	Analog					
AN10	22	25	28	14	I	Analog					
AN11	21	24	27	11	I	Analog					
AN12	20 ⁽²⁾	23 ⁽²⁾	26 ⁽²⁾ 11 ⁽³⁾	10 ⁽²⁾ 36 ⁽³⁾	- 1	Analog					
CLKI	6	9	7	30	I	ST/CMOS	External clock source input. Always associated with OSC1 pin function.				
CLKO	7	10	8	31	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.				
OSC1	6	9	7	30	I	ST/CMOS	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.				
OSC2	7	10	8	31	0	_	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.				
SOSCI	8	11	9	33	I	ST/CMOS	32.768 kHz low-power oscillator crystal input; CMOS otherwise.				
SOSCO	9	12	10	34	0	-	32.768 kHz low-power oscillator crystal output.				
REFCLKI	PPS	PPS	PPS	PPS	I	ST	Reference Input Clock				
REFCLKO	PPS	PPS	PPS	PPS	0	_	Reference Output Clock				
IC1	PPS	PPS	PPS	PPS	I	ST	Capture Inputs 1-5				
IC2	PPS	PPS	PPS	PPS		ST	1				
IC3	PPS	PPS	PPS	PPS		ST	1				
IC4	PPS	PPS	PPS	PPS		ST	1				
IC5	PPS	PPS	PPS	PPS	I	ST	1				
Legend:	CMOS = CM	MOS compa	atible input	or output		Analog =	Analog input P = Power				
:	ST = Schmitt Trigger input with CMOS levels O = Output I = Input										
	TTL = TTL i	TL = TTL input buffer PPS = Peripheral Pin Select — = N/A									

TTL = TTL input buffer

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability. 2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:



FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX110/210 DEVICES (4 KB RAM, 16 KB FLASH)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31.24	NVMDATA<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	NVMDATA<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	NVMDATA<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0				NVMD	ATA<7:0>						

REGISTER 5-4: NVMDATA: FLASH PROGRAM DATA REGISTER

Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMDATA<31:0>: Flash Programming Data bits

Note: The bits in this register are only reset by a Power-on Reset (POR).

REGISTER 5-5: NVMSRCADDR: SOURCE DATA ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	NVMSRCADDR<31:24>										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23:10	NVMSRCADDR<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	NVMSRCADDR<15:8>										
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
				NVMSRC	ADDR<7:0>						

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMSRCADDR<31:0>: Source Data Address bits

The system physical address of the data to be programmed into the Flash when the NVMOP<3:0> bits (NVMCON<3:0>) are set to perform row programming.

REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

- bit 3-0 ROSEL<3:0>: Reference Clock Source Select bits⁽¹⁾
 - 1111 = Reserved; do not use
 - 1001 = Reserved; do not use 1000 = REFCLKI 0111 = System PLL output 0110 = USB PLL output 0101 = Sosc 0100 = LPRC 0011 = FRC 0010 = POSC 0001 = PBCLK 0000 = SYSCLK
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
 - 2: This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
 - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—		—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	-	—
7.0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
7:0	UTEYE	UOEMON	—	USBSIDL	—	—	—	UASUSPND

REGISTER 10-20: U1CNFG1: USB CONFIGURATION 1 REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 UTEYE: USB Eye-Pattern Test Enable bit

- 1 = Eye-Pattern Test is enabled
- 0 = Eye-Pattern Test is disabled

bit 6 **UOEMON:** USB OE Monitor Enable bit

1 = OE signal is active; it indicates intervals during which the D+/D- lines are driving
 0 = OE signal is inactive

bit 5 Unimplemented: Read as '0'

- bit 4 USBSIDL: Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode

bit 3-1 Unimplemented: Read as '0'

bit 0 UASUSPND: Automatic Suspend Enable bit

- 1 = USB module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC<1>) in Register 10-5.
- 0 = USB module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC<1>) to suspend the module, including the USB 48 MHz clock.

IABL		PEI			1 SELEC		PUIRE	GISTER		CONTR									
SS										В	its								
Virtual Addre (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
FB4C	RPB8R	31:16	—	—	—	-	—	—	—	—	—	—	_	—	_	—	—	—	0000
		15:0		_									_			RPB8	<3:0>		0000
FB50	RPB9R	31:16		_	_	_	_	_			_	_			_			—	0000
		15:0	—	_	—	_	_	_	_	_	_	_	_	_		RPB9	<3:0>		0000
FB54	RPB10R	31:16	—	—	-	-	—	—	_	—	—	—	_	—	—	—	—	—	0000
	-	15:0	_	_	—		_	—	_	_	_	_	_	_		RPB10)<3:0>		0000
FB58	RPB11R	31:16	_	_	—		_	—	_	_	_	_	_	_	_	—	_	_	0000
		15:0		_	_		—	—	_				—	_		RPB1 ⁻	1<3:0>		0000
FB60	RPB13R	31:16		—	—	—	—	—	—	—	—	—	—	—	—				0000
		15:0		—	—	—	—	—	—	—	—	—	—	—		RPB1	3<3:0>		0000
FB64	RPB14R	31:16		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0		—	—	—	—	—	—	—	—	—	—	—		RPB14	4<3:0>		0000
FB68	RPB15R	31:16	—	—	—	—	-		—	—				—	—		—	—	0000
	1. 5101	15:0	—	—	—	—	-		—	—				—		RPB1	5<3:0>		0000
FB6C	RPCOR(3)	31:16	—	—	—	-	—	—	—	—	—	—	—	—	—	—	—	—	0000
. 200		15:0	—	—	—	-	—	—	—	—	—	—	—	—		RPC0	<3:0>		0000
EB70	RPC1R(3)	31:16	_	—	—	—	_	_	_	_	—	—	_	—	_	—	_	—	0000
1 870	NI OIIX	15:0	_	—	—	—	—	_	_	_	_	_	_	—		RPC1	<3:0>		0000
FB74		31:16	_	—	—	—	—	_	_	_	_	_	_	—	_	—	_	—	0000
1014		15:0	_	—	—	—	—	_	_	_	_	_	_	—		RPC2	<3:0>		0000
EB78		31:16		—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	0000
1 870		15:0		—	—	—	—	—	—	—	—	—	—	—		RPC3	<3:0>		0000
FB7C		31:16		—	—	—	—	—	—	—	—	—	—	—	_	—	—	—	0000
1 B/C		15:0	_	—	—	—	—	—	—	—	—	—	—	—		RPC4	<3:0>		0000
EDOO		31:16	-	—	—	—	—	—	—	—	—	—	—	—	-	—	-	-	0000
1 000	NF GOINT	15:0	_	—	—	—	—	—	—	—	—	—	—	—		RPC5	<3:0>		0000
ED94		31:16	—	—	—	—	—	—	_	—	—	—	—	—	—	—	—	—	0000
гро4	NFOUR	15:0	—	—	—	—	—	—	_	—	—	—	—	—		RPC6	<3:0>		0000
ED80		31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
F 000	KFU/KU	15:0	_	_	_	_	_	_		_	_	_	_	_		RPC7	<3:0>		0000

OT AUTOUT DEALATED MAD

x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal. Legend:

This register is only available on 44-pin devices. Note 1:

2: 3:

This register is only available on PIC32MX1XX devices. This register is only available on 36-pin and 44-pin devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	—	—	—	FEDGE	C32
7.0	R/W-0	R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0
7:0	ICTMR	ICI<	1:0>	ICOV	ICBNE	ICM<2:0>		

REGISTER 15-1: ICxCON: INPUT CAPTURE 'x' CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Bit Value at POR: ('0', '1', x = unkno	own)	P = Programmable bit	r = Reserved bit

bit 31-16	Unimplemented: Read as '0'
bit 15	ON: Input Capture Module Enable bit ⁽¹⁾
	1 = Module is enabled
	0 = Disable and reset module, disable clocks, disable interrupt generation and allow SFR modifications
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Stop in Idle Control bit
	 1 = Halt in Idle mode 0 = Continue to operate in Idle mode
bit 12-10	Unimplemented: Read as '0'
bit 9	FEDGE: First Capture Edge Select bit (only used in mode 6, ICM<2:0> = 110)
	1 = Capture rising edge first
	0 = Capture falling edge first
bit 8	C32: 32-bit Capture Select bit
	1 = 32-bit timer resource capture
	0 = 16-bit timer resource capture
bit 7	ICTMR: Timer Select bit (Does not affect timer selection when C32 (ICxCON<8>) is '1')
	0 = Timer3 is the counter source for capture
DIT 6-5	ICI<1:0>: Interrupt Control bits
	10 = Interrupt on every tourth capture event
	01 = Interrupt on every second capture event
	00 = Interrupt on every capture event
bit 4	ICOV: Input Capture Overflow Status Flag bit (read-only)
	1 = Input capture overflow has occurred
	0 = No input capture overflow has occurred
bit 3	ICBNE: Input Capture Buffer Not Empty Status bit (read-only)
	 1 = Input capture buffer is not empty; at least one more capture value can be read 0 = Input capture buffer is empty
Note 1:	When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the
	STOCK Cycle infinediately following the instruction that deals the module's ON bit.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 22-3: AD1CON3: ADC CONTROL REGISTER 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	_	—	_	_
45.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ADRC	—	—			SAMC<4:0> ⁽¹⁾		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W	R/W-0
	ADCS<7:0>(2)							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ADRC:** ADC Conversion Clock Source bit
 - 1 = Clock derived from FRC
 - 0 = Clock derived from Peripheral Bus Clock (PBCLK)
- bit 14-13 Unimplemented: Read as '0'
- - 00000001 =TPB • 2 • (ADCS<7:0> + 1) = 4 • TPB = TAD 00000000 =TPB • 2 • (ADCS<7:0> + 1) = 2 • TPB = TAD
- **Note 1:** This bit is only used if the SSRC<2:0> bits (AD1CON1<7:5>) = 111.
 - 2: This bit is not used if the ADRC (AD1CON3<15>) bit = 1.

REGISTER 25-1: CTMUCON: CTMU CONTROL REGISTER (CONTINUED) bit 24 EDG1STAT: Edge1 Status bit Indicates the status of Edge1 and can be written to control edge source 1 = Edge1 has occurred 0 = Edge1 has not occurred EDG2MOD: Edge2 Edge Sampling Select bit bit 23 1 = Input is edge-sensitive 0 = Input is level-sensitive bit 22 EDG2POL: Edge 2 Polarity Select bit 1 = Edge2 programmed for a positive edge response 0 = Edge2 programmed for a negative edge response bit 21-18 EDG2SEL<3:0>: Edge 2 Source Select bits 1111 = C3OUT pin is selected 1110 = C2OUT pin is selected 1101 = C1OUT pin is selected 1100 = PBCLK clock is selected 1011 = IC3 Capture Event is selected 1010 = IC2 Capture Event is selected 1001 = IC1 Capture Event is selected 1000 = CTED13 pin is selected 0111 = CTED12 pin is selected 0110 = CTED11 pin is selected 0101 = CTED10 pin is selected 0100 = CTED9 pin is selected 0011 = CTED1 pin is selected 0010 = CTED2 pin is selected 0001 = OC1 Compare Event is selected 0000 = Timer1 Event is selected bit 17-16 Unimplemented: Read as '0' bit 15 **ON:** ON Enable bit 1 = Module is enabled 0 = Module is disabled bit 14 Unimplemented: Read as '0' bit 13 CTMUSIDL: Stop in Idle Mode bit 1 = Discontinue module operation when the device enters Idle mode 0 = Continue module operation when the device enters Idle mode TGEN: Time Generation Enable bit⁽¹⁾ bit 12 1 = Enables edge delay generation 0 = Disables edge delay generation bit 11 EDGEN: Edge Enable bit 1 = Edges are not blocked 0 = Edges are blocked

- **Note 1:** When this bit is set for Pulse Delay Generation, the EDG2SEL<3:0> bits must be set to '1110' to select C2OUT.
 - 2: The ADC module Sample and Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitive measurement, must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC module must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.
 - 3: Refer to the CTMU Current Source Specifications (Table 30-41) in Section 30.0 "Electrical Characteristics" for current values.
 - 4: This bit setting is not available for the CTMU temperature diode.

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. However, it is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Configuration" Section 32. Section (DS60001124) and 33. "Programming and **Diagnostics**" (DS60001129), which are available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family devices include the following features intended to maximize application flexibility, reliability and minimize cost through elimination of external components.

- Flexible device configuration
- Joint Test Action Group (JTAG) interface
- In-Circuit Serial Programming[™] (ICSP[™])

27.1 Configuration Bits

The Configuration bits can be programmed using the following registers to select various device configurations.

- DEVCFG0: Device Configuration Word 0
- DEVCFG1: Device Configuration Word 1
- DEVCFG2: Device Configuration Word 2
- DEVCFG3: Device Configuration Word 3
- · CFGCON: Configuration Control Register

In addition, the DEVID register (Register 27-6) provides device and revision information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
31:24	—	—	—	—	—	—	—	—
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
23:10	—	—	—	—	—	FPLLODIV<2:0>		
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
15:8	UPLLEN ⁽¹⁾	—	—	_	_	UF	PLLIDIV<2:0>	.(1)
7.0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
7:0	_	FPLLMUL<2:0>			_	FPLLIDIV<2:0>		

DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 27-3:

Legend:	r = Reserved bit	P = Programmable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit⁽¹⁾ 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits⁽¹⁾ 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider000 = 1x divider Reserved: Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
 - 111 = 24x multiplier 110 = 21x multiplier
 - 101 = 20x multiplier
 - 100 = 19x multiplier
 - 011 = 18x multiplier
 - 010 = 17x multiplier
 - 001 = 16x multiplier
 - 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

27.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX 28/36/44-pin Family devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX 28/36/44-pin Family family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 30.1 "DC Characteristics"**.

Note:	It is important that the low-ESR capacitor
	is placed as close as possible to the VCAP
	pin.

27.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

27.3.2 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX 28/36/44-pin Family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 30.1 "DC Characteristics"**.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



27.4 **Programming and Diagnostics**

PIC32MX1XX/2XX 28/36/44-pin Family devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming[™] (ICSP[™]) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

Figure 27-2 illustrates a block diagram of the programming, debugging, and trace ports.





AC CHARACTERISTICS			Standard Op (unless othe Operating ter	perating Co erwise state mperature	onditions: 2.3 ed) -40°C ≤ TA ≤ -40°C ≤ TA ≤	√ to 3.6\ +85°C fc +105°C	/ or Industrial for V-temp
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
OS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		40 40	MHz MHz	EC (Note 4) ECPLL (Note 3)
OS11		Oscillator Crystal Frequency	3	_	10	MHz	XT (Note 4)
OS12			4	—	10	MHz	XTPLL (Notes 3,4)
OS13			10	—	25	MHz	HS (Note 5)
OS14			10	—	25	MHz	HSPLL (Notes 3,4)
OS15			32	32.768	100	kHz	Sosc (Note 4)
OS20	Tosc	Tosc = 1/Fosc = Tcy (Note 2)	_	_			See parameter OS10 for Fosc value
OS30	TosL, TosH	External Clock In (OSC1) High or Low Time	0.45 x Tosc	—	_	ns	EC (Note 4)
OS31	TosR, TosF	External Clock In (OSC1) Rise or Fall Time	—	—	0.05 x Tosc	ns	EC (Note 4)
OS40	Тоѕт	Oscillator Start-up Timer Period (Only applies to HS, HSPLL, XT, XTPLL and Sosc Clock Oscillator modes)	_	1024	_	Tosc	(Note 4)
OS41	TFSCM	Primary Clock Fail Safe Time-out Period	—	2	—	ms	(Note 4)
OS42	Gм	External Oscillator Transconductance (Primary Oscillator only)		12		mA/V	VDD = 3.3V, TA = +25°C (Note 4)

TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are characterized but are not tested.

2: Instruction cycle period (Tcr) equals the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin.

3: PLL input requirements: 4 MHz \leq FPLLIN \leq 5 MHz (use PLL prescaler to reduce FOSC). This parameter is characterized, but tested at 10 MHz only at manufacturing.

4: This parameter is characterized, but not tested in manufacturing.

TABLE 30-32:	I2Cx BUS DATA	TIMING REQUIREMENTS	(MASTER MODE)	(CONTINUED)	
			((001111010)	

AC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM40	TAA:SCL	Output Valid	100 kHz mode	_	3500	ns	—
		from Clock	400 kHz mode	—	1000	ns	—
			1 MHz mode (Note 2)	—	350	ns	—
IM45	TBF:SDA	DA Bus Free Time	100 kHz mode	4.7	—	μS	The amount of time the
			400 kHz mode	1.3		μS	bus must be free
			1 MHz mode (Note 2)	0.5	—	μS	transmission can start
IM50	Св	Bus Capacitive Loading		_	400	pF	—
IM51	TPGD	Pulse Gobbler D	elay	52	312	ns	See Note 3

Note 1: BRG is the value of the I^2C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

NOTES:

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		MILLIM	ETERS	
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

Revision J (April 2016)

This revision includes the following major changes as described in Table A-8, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-8: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	The PIC32MX270FDB device and Note 4 were added to TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features".
2.0 "Guidelines for Getting Started with 32-bit MCUs"	EXAMPLE 2-1: "Crystal Load Capacitor Calculation" was updated.
30.0 "Electrical Characteristics"	Parameter DO50a (Csosc) was removed from the Capacitive Loading Requirements on Output Pins AC Characteristics (see Table 30-16).
"Product Identification System"	The device mapping was updated to include type B for Software Targeting.

Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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