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#### Details

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Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032b-v-so

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#### TABLE 9: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

## 44-PIN QFN (TOP VIEW)<sup>(1,2,3,5)</sup>

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	Vdd
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 <sup>(4)</sup> /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 <sup>(4)</sup> /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	Vdd
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

44

1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

## 7.0 INTERRUPT CONTROLLER

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 8. "Interrupt Controller" (DS60001108), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family devices generate interrupt requests in response to interrupt events from peripheral modules. The interrupt control module exists externally to the CPU logic and prioritizes the interrupt events before presenting them to the CPU.

The PIC32MX1XX/2XX 28/36/44-pin Family interrupt module includes the following features:

- Up to 64 interrupt sources
- Up to 44 interrupt vectors
- · Single and multi-vector mode operations
- Five external interrupts with edge polarity control
- Interrupt proximity timer
- Seven user-selectable priority levels for each vector
- Four user-selectable subpriority levels within each priority
- · Software can generate any interrupt
- User-configurable Interrupt Vector Table (IVT) location
- User-configurable interrupt vector spacing

A simplified block diagram of the Interrupt Controller module is illustrated in Figure 7-1.



#### FIGURE 7-1: INTERRUPT CONTROLLER MODULE BLOCK DIAGRAM

Note: The dedicated shadow register set is not present on PIC32MX1XX/2XX 28/36/44-pin Family devices.

## 8.1 Oscillator Control Regiters

ТАВ	LE 8-1:	0	SCILL	ATOR (	CONTR	OL REG	ISTER	MAP														
ess		ė									Bits								s			
Virtual Addr (BF80_#)	Register Name <sup>(1)</sup>	Bit Rang	Bit Range	Bit Rang	Bit Ranç	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F000		31:16	_	_	Р	LLODIV<2:	)>	F	FRCDIV<2:0>		—	SOSCRDY	PBDIVRDY	PBDI\	/<1:0>	PLLMULT<2:0>			x1xx(2)			
	USCCON	15:0	—		COSC<2:0	)>	_		NOSC<2:0>			ULOCK <sup>(3)</sup>	SLOCK	SLPEN	CF	UFRCEN <sup>(3)</sup>	SOSCEN	OSWEN	xxxx(2)			
E010		31:16	_	_			_	_			_	_	_	_	—	_		_	0000			
1 0 10	030101	15:0	_	_			_	_			_	_			TUN	<b>\&lt;</b> 5:0>			0000			
<b>F000</b>		31:16	_								RODIV<1	4:0>							0000			
F020	REFUCUN	15:0	ON		SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	-				ROSE	L<3:0>		0000			
F000	DEEOTDIM	31:16				F	OTRIM<8:	0>				_	_	_	_	_		_	0000			
F030	REFUTRIM	15:0	_	_	_		_	_	_	_	_	_	_	_	_	_	_	_	0000			

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This bit is only available on PIC32MX2XX devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
31:24	—	RODIV<14:8>(1,3)										
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
23:16	RODIV<7:0> <sup>(1,3)</sup>											
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R-0, HS, HC				
15:8	ON	_	SIDL	OE	RSLP <sup>(2)</sup>	-	DIVSWEN	ACTIVE				
	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0				
7:0						ROSEL<3:0> <sup>(1)</sup>						

#### **REGISTER 8-3: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

Legend:	HC = Hardware Clearable	HS = Hardware Settable	
R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 Unimplemented: Read as '0'

bit 30-16	RODIV<14:0> Reference Clock Divider bits <sup>(1,3)</sup>
	The value selects the reference clock divider bits. See Figure 8-1 for information.
bit 15	ON: Output Enable bit
	1 = Reference Oscillator module is enabled
	0 = Reference Oscillator module is disabled
bit 14	Unimplemented: Read as '0'
bit 13	SIDL: Peripheral Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
  - 0 =Continue module operation when the device enters lide mode
- bit 12 **OE:** Reference Clock Output Enable bit
  - 1 = Reference clock is driven out on REFCLKO pin
  - 0 = Reference clock is not driven out on REFCLKO pin
- bit 11 RSLP: Reference Oscillator Module Run in Sleep bit<sup>(2)</sup>
  - 1 = Reference Oscillator module output continues to run in Sleep
  - 0 = Reference Oscillator module output is disabled in Sleep
- bit 10 Unimplemented: Read as '0'
- bit 9 DIVSWEN: Divider Switch Enable bit
  - 1 = Divider switch is in progress
    - 0 = Divider switch is complete
- bit 8 ACTIVE: Reference Clock Request Status bit
  - 1 = Reference clock request is active
  - 0 = Reference clock request is not active
- bit 7-4 Unimplemented: Read as '0'
- **Note 1:** The ROSEL and RODIV bits should not be written while the ACTIVE bit is '1', as undefined behavior may result.
  - **2:** This bit is ignored when the ROSEL<3:0> bits = 0000 or 0001.
  - 3: While the ON bit is set to '1', writes to these bits do not take effect until the DIVSWEN bit is also set to '1'.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
31.24	CHSSA<31:24>											
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
23:10	CHSSA<23:16>											
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
15:8	CHSSA<15:8>											
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
7:0		CHSSA<7:0>										

#### **REGISTER 9-10: DCHxSSA: DMA CHANNEL 'x' SOURCE START ADDRESS REGISTER**

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

 bit 31-0
 CHSSA<31:0> Channel Source Start Address bits

 Channel source start address.

 Note: This must be the physical address of the source.

#### **REGISTER 9-11: DCHxDSA: DMA CHANNEL 'x' DESTINATION START ADDRESS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
01.04	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
31:24	CHDSA<31:24>										
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
23.10	CHDSA<23:16>										
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
15:8	CHDSA<15:8>										
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	CHDSA<7:0>										

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 **CHDSA<31:0>:** Channel Destination Start Address bits Channel destination start address.

 $\ensuremath{\textbf{Note:}}$  This must be the physical address of the destination.

#### TABLE 10-1: USB REGISTER MAP (CONTINUED)

ess											Bit	s							
Virtual Addr (BF88_#)	Registe Name <sup>(1</sup> )	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
5390	LI1EP9	31:16	—	—	—	—	—	—	-		_	_	—	—	—	-	—	—	0000
0000	UTER 9	15:0	_	—	—	—		—	_	—	_		—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5340		31:16	_	—	—	—	—	—	_	—	_	_	—		_	_	—		0000
5570	UTEL TO	15:0	-	—	_	—	_	_	-	_	_	_	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0		31:16		_	_	_	_	_		_			_	—			_	—	0000
5560	UILFII	15:0		—	_	_	_	_		_	-	-	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5300		31:16		_	_	_	_	_		_			_	—			_	—	0000
5500	UILF 12	15:0		—	_	_	_	_		_	-	-	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5200		31:16		—	_	_	_	_		_	-	-	—	—		-		—	0000
5500	UILF 13	15:0		—	_	_	_	_		_	-	-	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_	_	_	_	_	_	_	_	_	_	—	_	_	_	—	0000
53E0	UTEP14	15:0	_	_		_			_		_	_	_	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
5050		31:16	_	_		_			_		_	_	_	_	_	_	_	—	0000
53FU	UTEP15	15:0	_						_			-		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	LSPDEN			D	EVADDR<6:0	)>		

## REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

## Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 LSPDEN: Low-Speed Enable Indicator bit

1 = Next token command to be executed at Low-Speed

0 = Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
04-04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	_	—	—	—	—	—	_	—			
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23:10	_	—	—	—	—	—	_	—			
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
15:8	—	—	—	—	—	—		—			
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0			
7.0		FRML<7:0>									

#### REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

#### TABLE 11-1: INPUT PIN SELECTION

Peripheral Pin	[pin name]R SFR	[pin name]R bits	[ <i>pin name</i> ]R Value to RPn Pin Selection
INT4	INT4R	INT4R<3:0>	0000 = RPA0 0001 = RPB3
T2CK	T2CKR	T2CKR<3:0>	0010 = RPB4 0011 = RPB15 0100 = RPB7
IC4	IC4R	IC4R<3:0>	$0101 = RPC7^{(2)}$ $0110 = RPC0^{(1)}$ $0111 = RPC5^{(2)}$
SS1	SS1R	SS1R<3:0>	1000 = Reserved
REFCLKI	REFCLKIR	REFCLKIR<3:0>	: 1111 = Reserved
INT3	INT3R	INT3R<3:0>	0000 = RPA1 0001 = RPB5
ТЗСК	T3CKR	T3CKR<3:0>	0010 = RPB1 0011 = RPB11
IC3	IC3R	IC3R<3:0>	0100 = RPB8 $0101 = RPA8^{(2)}$
U1CTS	U1CTSR	U1CTSR<3:0>	$0110 = RPC8^{(2)}$ $0111 = RPA9^{(2)}$
U2RX	U2RXR	U2RXR<3:0>	•
SDI1	SDI1R	SDI1R<3:0>	• 1111 = Reserved
INT2	INT2R	INT2R<3:0>	0000 = RPA2
T4CK	T4CKR	T4CKR<3:0>	
IC1	IC1R	IC1R<3:0>	0011 = RPB13
IC5	IC5R	IC5R<3:0>	$0101 = \text{RPC6}^{(2)}$
U1RX	U1RXR	U1RXR<3:0>	$-0110 = \text{RPC1}^{(1)}$ 0111 = RPC3(1)
U2CTS	U2CTSR	U2CTSR<3:0>	1000 = Reserved
SDI2	SDI2R	SDI2R<3:0>	
OCFB	OCFBR	OCFBR<3:0>	• 1111 = Reserved
INT1	INT1R	INT1R<3:0>	0000 = RPA3 0001 = RPB14
T5CK	T5CKR	T5CKR<3:0>	0010 = RPB0 0011 = RPB10 0100 = RPB9
IC2	IC2R	IC2R<3:0>	$0101 = RPC9^{(1)}$ $0110 = RPC2^{(2)}$ $0111 = PPC4^{(2)}$
SS2	SS2R	SS2R<3:0>	1000 = Reserved
OCFA	OCFAR	OCFAR<3:0>	1111 = Reserved

Note 1: This pin is not available on 28-pin devices.

2: This pin is only available on 44-pin devices.

#### REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

- bit 3 T32: 32-Bit Timer Mode Select bit<sup>(2)</sup>
  - 1 = Odd numbered and even numbered timers form a 32-bit timer
  - 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit<sup>(3)</sup>
  - 1 = External clock from TxCK pin
  - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
  - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
  - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

## 14.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog, Deadman, and Power-up Timers" (DS60001114), which are available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32). The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- · Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle mode

Figure 14-1 illustrates a block diagram of the WDT and Power-up timer.

## FIGURE 14-1: WATCHDOG TIMER AND POWER-UP TIMER BLOCK DIAGRAM



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	-	—
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—		—
45.0	R-0	R/W-0, HSC	U-0	U-0	R-0	R-0	R-0	R-0
15:8	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
7:0	R-1	R/W-0, HSC	U-0	U-0	R-1	R-1	R-1	R-1
	OBE	OBUF	_	_	OB3E	OB2E	OB1E	OB0E

#### REGISTER 20-5: PMSTAT: PARALLEL PORT STATUS REGISTER (SLAVE MODES ONLY)

Legend:	HSC = Set by Hardware; Cleared by Software				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 IBF: Input Buffer Full Status bit
  - 1 = All writable input buffer registers are full
  - 0 = Some or all of the writable input buffer registers are empty
- bit 14 IBOV: Input Buffer Overflow Status bit
  - 1 = A write attempt to a full input byte buffer occurred (must be cleared in software)
     0 = No overflow occurred
- bit 13-12 Unimplemented: Read as '0'
- bit 11-8 IBxF: Input Buffer 'x' Status Full bits
  - 1 = Input Buffer contains data that has not been read (reading buffer will clear this bit)
  - 0 = Input Buffer does not contain any unread data
- bit 7 **OBE:** Output Buffer Empty Status bit
  - 1 = All readable output buffer registers are empty
  - 0 = Some or all of the readable output buffer registers are full
- bit 6 **OBUF:** Output Buffer Underflow Status bit
  - 1 = A read occurred from an empty output byte buffer (must be cleared in software)
     0 = No underflow occurred
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-0 **OBxE:** Output Buffer 'x' Status Empty bits
  - 1 = Output buffer is empty (writing data to the buffer will clear this bit)
  - 0 = Output buffer contains data that has not been transmitted

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
31.24	—			<3:0>				
00.40	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
23:10	—	MIN10<2:0>				MIN01<3:0>		
45.0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
15:8	—	SEC10<2:0>				SEC0 <sup>2</sup>	1<3:0>	
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
7:0	—	—	—	—	—		—	—
Legend:								

#### REGISTER 21-3: RTCTIME: RTC TIME VALUE REGISTER

# R = Readable bitW = Writable bitU = Unimplemented bit, read as '0'-n = Value at POR'1' = Bit is set'0' = Bit is clearedx = Bit is

bit 31-30 Unimplemented: Read as '0'

bit 29-28 HR10<1:0>: Binary-Coded Decimal Value of Hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary-Coded Decimal Value of Hours bits, 1s place digit; contains a value from 0 to 9 bit 23 **Unimplemented:** Read as '0'

bit 22-20 MIN10<2:0>: Binary-Coded Decimal Value of Minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary-Coded Decimal Value of Minutes bits, 1s place digit; contains a value from 0 to 9 bit 15 **Unimplemented:** Read as '0'

bit 14-12 SEC10<2:0>: Binary-Coded Decimal Value of Seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary-Coded Decimal Value of Seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 Unimplemented: Read as '0'

**Note:** This register is only writable when RTCWREN = 1 (RTCCON<3>).

x = Bit is unknown

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	CH0NB	—	—	—		CH0SB	<3:0>	
00.40	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	CH0NA	—	—	—	CH0SA<3:0>			
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	_	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
						_		

### REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

CHONB: Negative Input Select bit for Sample B

# Legend:

bit 31

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

		<ul> <li>1 = Channel 0 negative input is AN1</li> <li>0 = Channel 0 negative input is VREFL</li> </ul>
bit 30	-28	Unimplemented: Read as '0'
bit 27	-24	CH0SB<3:0>: Positive Input Select bits for Sample B
		<pre>1111 = Channel 0 positive input is Open<sup>(1)</sup> 1110 = Channel 0 positive input is IVREF<sup>(2)</sup> 1101 = Channel 0 positive input is CTMU temperature sensor (CTMUT)<sup>(3)</sup> 1100 = Channel 0 positive input is AN12<sup>(4)</sup></pre>
		•
		•
		•
		0001 = Channel 0 positive input is AN1 0000 = Channel 0 positive input is AN0
bit 23		CH0NA: Negative Input Select bit for Sample A Multiplexer Setting <sup>(2)</sup>
		<ul><li>1 = Channel 0 negative input is AN1</li><li>0 = Channel 0 negative input is VREFL</li></ul>
bit 22	-20	Unimplemented: Read as '0'
bit 19	-16	CH0SA<3:0>: Positive Input Select bits for Sample A Multiplexer Setting 1111 = Channel 0 positive input is Open <sup>(1)</sup> 1110 = Channel 0 positive input is IVREF <sup>(2)</sup> 1101 = Channel 0 positive input is CTMU temperature (CTMUT) <sup>(3)</sup> 1100 = Channel 0 positive input is AN12 <sup>(4)</sup>
		•
		•
		•
		0001 = Channel 0 positive input is AN1 0000 = Channel 0 positive input is AN0
bit 15	-0	Unimplemented: Read as '0'
Note	1: 2: 3: 4:	This selection is only used with CTMU capacitive and time measurement. See Section 24.0 "Comparator Voltage Reference (CVREF)" for more information. See Section 25.0 "Charge Time Measurement Unit (CTMU)" for more information. AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:16	—	—	—	—	—	—	—	—	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
15:8	CSSL15	CSSL14	CSSL13	CSSL12	CSSL11	CSSL10	CSSL9	CSSL8	
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	CSSL7	CSSL6	CSSL5	CSSL4	CSSL3	CSSL2	CSSL1	CSSL0	

#### REGISTER 22-5: AD1CSSL: ADC INPUT SCAN SELECT REGISTER

## Legend:

Logena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-0 CSSL<15:0>: ADC Input Pin Scan Selection bits<sup>(1,2)</sup>

1 = Select ANx for input scan

0 = Skip ANx for input scan

- **Note 1:** CSSL = ANx, where 'x' = 0-12; CSSL13 selects CTMU input for scan; CSSL14 selects IVREF for scan; CSSL15 selects Vss for scan.
  - 2: On devices with less than 13 analog inputs, all CSSLx bits can be selected; however, inputs selected for scan without a corresponding input on the device will convert to VREFL.

## 26.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 10. "Power-
	Saving Features" (DS60001130), which
	is available from the Documentation >
	Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

## 26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

## 26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

## 26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

## 26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See Section 26.3.3 "Peripheral Bus Scaling Method" for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

#### **30.1 DC Characteristics**

#### TABLE 30-1: OPERATING MIPS VS. VOLTAGE

Characteristic	VDD Range	Temp. Range	Max. Frequency		
Characteristic	(in Volts) <sup>(1)</sup> (in °C)		PIC32MX1XX/2XX 28/36/44-pin Family		
DC5	2.3-3.6V	-40°C to +85°C	40 MHz		
DC5b	2.3-3.6V	-40°C to +105°C	40 MHz		

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

## TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typical	Max.	Unit
Industrial Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
V-temp Temperature Devices					
Operating Junction Temperature Range	TJ	-40	_	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+105	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – S IOH)	PD	PINT + PI/O		W	
I/O Pin Power Dissipation: I/O = S (({VDD – VOH} x IOH) + S (VOL x IOL))					
Maximum Allowed Power Dissipation	PDMAX	(	TJ — TA)/θJ	A	W

#### TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristics	Symbol	Typical	Max.	Unit	Notes
Package Thermal Resistance, 28-pin SSOP	θJA	71	_	°C/W	1
Package Thermal Resistance, 28-pin SOIC	θJA	50	_	°C/W	1
Package Thermal Resistance, 28-pin SPDIP	θJA	42		°C/W	1
Package Thermal Resistance, 28-pin QFN	θJA	35		°C/W	1
Package Thermal Resistance, 36-pin VTLA	θJA	31	—	°C/W	1
Package Thermal Resistance, 44-pin QFN	θJA	32		°C/W	1
Package Thermal Resistance, 44-pin TQFP	θJA	45		°C/W	1
Package Thermal Resistance, 44-pin VTLA	θJA	30	—	°C/W	1

**Note 1:** Junction to ambient thermal resistance, Theta-JA ( $\theta$ JA) numbers are achieved by package simulations.

## TABLE 30-14: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$					
Param. No.	Symbol	Characteristics	Min. Typ. Max. Units Comments					
D312	TSET	Internal 4-bit DAC Comparator Reference Settling time	_		10	μs	See Note 1	
D313	DACREFH	CVREF Input Voltage	AVss	—	AVDD	V	CVRSRC with CVRSS = 0	
		Reference Range	VREF-	—	VREF+	V	CVRSRC with CVRSS = 1	
D314	DVREF	CVREF Programmable Output Range	0	—	0.625 x DACREFH	V	0 to 0.625 DACREFH with DACREFH/24 step size	
			0.25 x DACREFH	_	0.719 x DACREFH	V	0.25 x DACREFH to 0.719 DACREFH with DACREFH/32 step size	
D315	DACRES	Resolution	—	—	DACREFH/24	-	CVRCON <cvrr> = 1</cvrr>	
			_	—	DACREFH/32	_	CVRCON <cvrr> = 0</cvrr>	
D316	DACACC	Absolute Accuracy <sup>(2)</sup>		_	1/4	LSB	DACREFH/24, CVRCON <cvrr> = 1</cvrr>	
			—	_	1/2	LSB	DACREFH/32, CVRCON <cvrr> = 0</cvrr>	

**Note 1:** Settling time was measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'. This parameter is characterized, but is not tested in manufacturing.

**2:** These parameters are characterized but not tested.

#### TABLE 30-15: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

DC CHA	RACTERIS	STICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$				: <b>2.3V to 3.6V</b> TA $\leq$ +85°C for Industrial TA $\leq$ +105°C for V-temp
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Comments
D321	Cefc	External Filter Capacitor Value	8	10	_	μF	Capacitor must be low series resistance (1 ohm). Typical voltage on the VCAP pin is 1.8V.



#### FIGURE 30-11: SPIX MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

#### TABLE 30-29: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard (unless of Operating	d Operatin otherwise g temperat	<b>ng Condit</b> stated) ture -40 -40	tions: 2. °C ≤ Ta °C ≤ Ta	<b>3V to 3.6V</b> ≤ +85°C for Industrial ≤ +105°C for V-temp
Param. No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Тур. <sup>(2)</sup>	Max.	Units	Conditions
SP10	TscL	SCKx Output Low Time (Note 3)	Tsck/2	—		ns	
SP11	TscH	SCKx Output High Time (Note 3)	Tsck/2		_	ns	—
SP20	TscF	SCKx Output Fall Time (Note 4)	—	—	_	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time (Note 4)	_		_	ns	See parameter DO31
SP30	TDOF	SDOx Data Output Fall Time (Note 4)	_	—		ns	See parameter DO32
SP31	TDOR	SDOx Data Output Rise Time (Note 4)	_	—	_	ns	See parameter DO31
SP35	TscH2doV,	SDOx Data Output Valid after	_		15	ns	VDD > 2.7V
	TscL2DoV	SCKx Edge	_		20	ns	VDD < 2.7V
SP36	TDOV2SC, TDOV2SCL	SDOx Data Output Setup to First SCKx Edge	15	—		ns	—
SP40	TDIV2scH,	Setup Time of SDIx Data Input to	15		_	ns	VDD > 2.7V
	TDIV2scL	SCKx Edge	20	—	_	ns	VDD < 2.7V
SP41	TscH2DIL,	Hold Time of SDIx Data Input	15	—	_	ns	VDD > 2.7V
	TscL2DIL	to SCKx Edge	20	—	_	ns	VDD < 2.7V

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

#### TABLE 30-37: PARALLEL SLAVE PORT REQUIREMENTS

АС СН	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature-40°C $\leq$ TA $\leq$ +85°C for Indu -40°C $\leq$ TA $\leq$ +105°C for V-t					t <b>o 3.6V</b> 35°C for Industrial 105°C for V-temp		
Para m.No.	Symbol	Characteristics <sup>(1)</sup>	Min. Typ. Max. Units Conditions					
PS1	TdtV2wr H	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20			ns	_	
PS2	TwrH2dt I	WR or CS Inactive to Data-In Invalid (hold time)	40		—	ns	—	
PS3	TrdL2dt V	RD and CS Active to Data-Out Valid	—		60	ns	—	
PS4	TrdH2dtl	RD Active or CS Inactive to Data-Out Invalid	0	_	10	ns	—	
PS5	Tcs	CS Active Time	Трв + 40		—	ns	—	
PS6	TwR	WR Active Time	Трв + 25		_	ns	_	
PS7	Trd	RD Active Time	Трв + 25	_	_	ns	_	

**Note 1:** These parameters are characterized, but not tested in manufacturing.

## FIGURE 30-21: PARALLEL MASTER PORT READ TIMING DIAGRAM



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