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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032b-v-ss

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 6: PIN NAMES FOR 28-PIN USB DEVICES

28-PIN QFN (TOP VIEW) ^(1,2,3,4)			
PIC32MX210F016B PIC32MX220F032B PIC32MX230F064B PIC32MX230F256B PIC32MX250F128B PIC32MX270F256B		28	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	16	VSS
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	VCAP
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	PGED2/RPB10/D+/CTED11/RB10
5	VSS	19	PGEC2/RPB11/D-/RB11
6	OSC1/CLKI/RPA2/RA2	20	VUSB3V3
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CVREFOUT/AN10/C3INB/RPB14/VBUSEN/SCK1/CTED5/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	VDD	24	AVSS
11	TMS/RPB5/USBID/RB5	25	AVDD
12	VBUS	26	MCLR
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/VREF-/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Referenced Sources

This device data sheet is based on the following individual chapters of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the <i>Documentation > Reference Manuals</i> section of the Microchip PIC32 website: http://www.microchip.com/pic32

- **Section 1. “Introduction”** (DS60001127)
- **Section 2. “CPU”** (DS60001113)
- **Section 3. “Memory Organization”** (DS60001115)
- **Section 5. “Flash Program Memory”** (DS60001121)
- **Section 6. “Oscillator Configuration”** (DS60001112)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Compare”** (DS60001111)
- **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116)
- **Section 27. “USB On-The-Go (OTG)”** (DS60001126)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 37. “Charge Time Measurement Unit (CTMU)”** (DS60001167)

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 4-1: SFR MEMORY MAP

Peripheral	Virtual Address	
	Base	Offset Start
Watchdog Timer	0xBF80	0x0000
RTCC		0x0200
Timer1-5		0x0600
Input Capture 1-5		0x2000
Output Compare 1-5		0x3000
IC1 and IC2		0x5000
SPI1 and SPI2		0x5800
UART1 and UART2		0x6000
PMP		0x7000
ADC		0x9000
CVREF		0x9800
Comparator		0xA000
CTMU		0xA200
Oscillator		0xF000
Device and Revision ID		0xF220
Peripheral Module Disable		0xF240
Flash Controller		0xF400
Reset		0xF600
PPS		0xFA04
Interrupts	0xBF88	0x1000
Bus Matrix		0x2000
DMA		0x3000
USB		0x5050
PORTA-PORTC		0x6000
Configuration	0xBFC0	0x0BF0

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP03<2:0>			IS03<1:0>	
23:16	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP02<2:0>			IS02<1:0>	
15:8	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP01<2:0>			IS01<1:0>	
7:0	U-0 —	U-0 —	U-0 —	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
				IP00<2:0>			IS00<1:0>	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 25-24 **IS03<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

bit 17-16 **IS02<1:0>**: Interrupt Subpriority bits

11 = Interrupt subpriority is 3

10 = Interrupt subpriority is 2

01 = Interrupt subpriority is 1

00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP01<2:0>**: Interrupt Priority bits

111 = Interrupt priority is 7

.

010 = Interrupt priority is 2

001 = Interrupt priority is 1

000 = Interrupt is disabled

Note: This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit

1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle

0 = A "type A" OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit

1 = USB line state (SE0 (U1CON<6>) bit and JSTATE (U1CON<7>)) bit has been stable for previous 1 ms

0 = USB line state (SE0 and JSTATE) has not been stable for previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A or B device

0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit

1 = VBUS voltage is below Session Valid on the B device

0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A device

0 = VBUS voltage is below Session Valid on the A device

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 10-11: U1CON: USB CONTROL REGISTER (CONTINUED)

- bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
 1 = Reset all Even/Odd buffer pointers to the EVEN Buffer Descriptor banks
 0 = Even/Odd buffer pointers are not Reset
- bit 0 **USBEN:** USB Module Enable bit⁽⁴⁾
 1 = USB module and supporting circuitry is enabled
 0 = USB module and supporting circuitry is disabled
- SOFEN:** SOF Enable bit⁽⁵⁾
 1 = SOF token is sent every 1 ms
 0 = SOF token is disabled

- Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
- 2:** All host control logic is reset any time that the value of this bit is toggled.
- 3:** Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
- 4:** Device mode.
- 5:** Host mode.

16.0 OUTPUT COMPARE

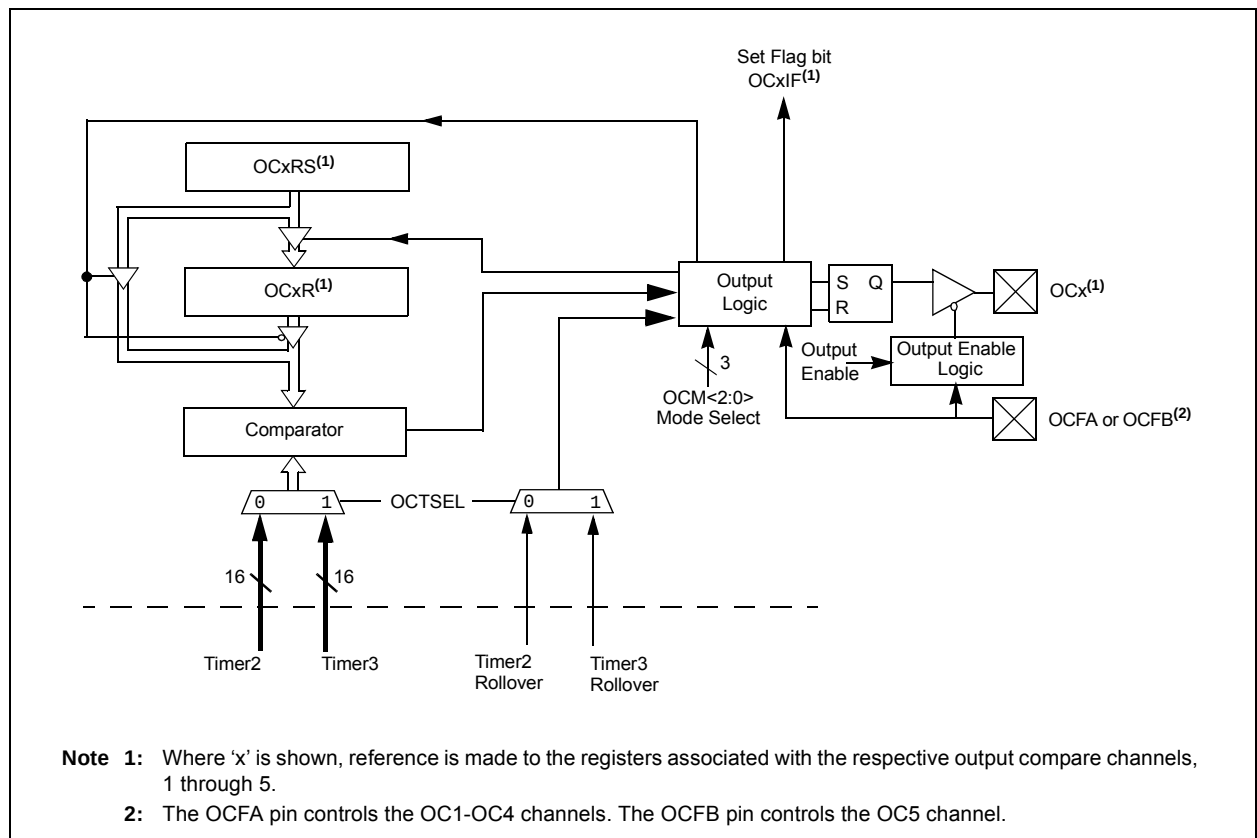
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 16. “Output Compare”** (DS60001111), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

The Output Compare module is used to generate a single pulse or a train of pulses in response to selected time base events. For all modes of operation, the Output Compare module compares the values stored in the OCxR and/or the OCxRS registers to the value in the selected timer. When a match occurs, the Output Compare module generates an event based on the selected mode of operation.

The following are some of the key features:

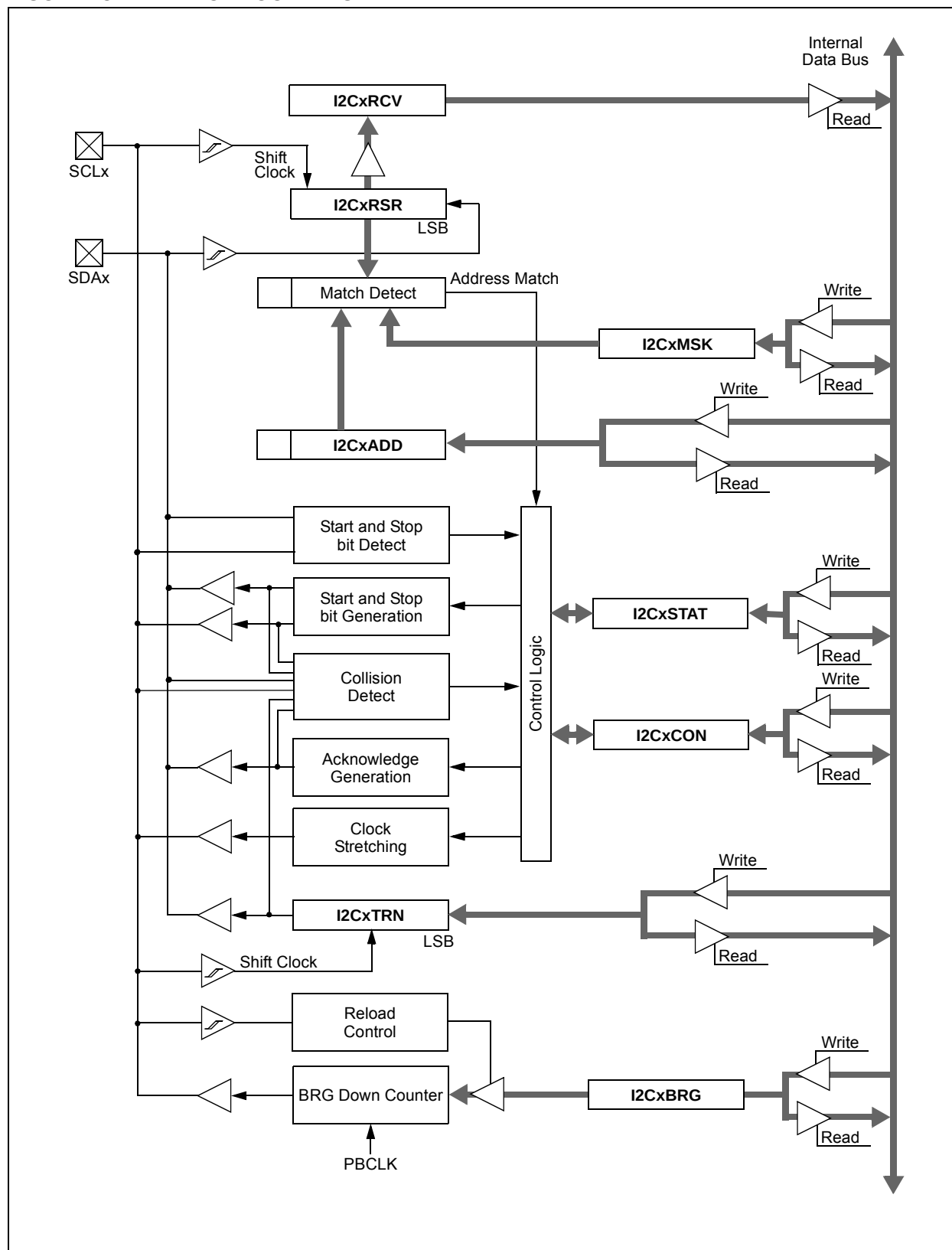
- Multiple Output Compare Modules in a device
- Programmable interrupt generation on compare event
- Single and Dual Compare modes
- Single and continuous output pulse generation
- Pulse-Width Modulation (PWM) mode
- Hardware-based PWM Fault detection and automatic output disable
- Can operate from either of two available 16-bit time bases or a single 32-bit time base

FIGURE 16-1: OUTPUT COMPARE MODULE BLOCK DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 18-1: I²C BLOCK DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	CAL<9:8>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CAL<7:0>							
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON ^(1,2)	—	SIDL	—	—	—	—	—
7:0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0
	RTSECSEL ⁽³⁾	RTCCLKON	—	—	RTCWREN ⁽⁴⁾	RTCSYNC	HALFSEC ⁽⁵⁾	RTCOE

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** RTC Drift Calibration bits, which contain a signed 10-bit integer value

0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute

.

.

0000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute

0000000000 = No adjustment

1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute

.

.

1000000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute

bit 15 **ON:** RTCC On bit^(1,2)

1 = RTCC module is enabled

0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables the PBCLK to the RTCC when the device enters Idle mode

0 = Continue normal operation when the device enters Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **RTSECSEL:** RTCC Seconds Clock Output Select bit⁽³⁾

1 = RTCC Seconds Clock is selected for the RTCC pin

0 = RTCC Alarm Pulse is selected for the RTCC pin

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit

1 = RTCC Clock is actively running

0 = RTCC Clock is not running

Note 1: The ON bit is only writable when RTCWREN = 1.

2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSClk cycle immediately following the instruction that clears the module's ON bit.

3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

4: The RTCWREN bit can be set only when the write sequence is enabled.

5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions
Program Flash Memory⁽³⁾							
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	—	411	—	FRC Cycles	See Note 4
D136	TRW	Row Write Cycle Time	—	6675	—		See Note 2,4
D137	TPE	Page Erase Cycle Time	—	20011	—		See Note 4
	TCE	Chip Erase Cycle Time	—	80180	—		See Note 4

Note 1: Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to the “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode (Note 2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_B$	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	ns	—
			400 kHz mode	$TPB * (BRG + 2)$	—	ns	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	ns	

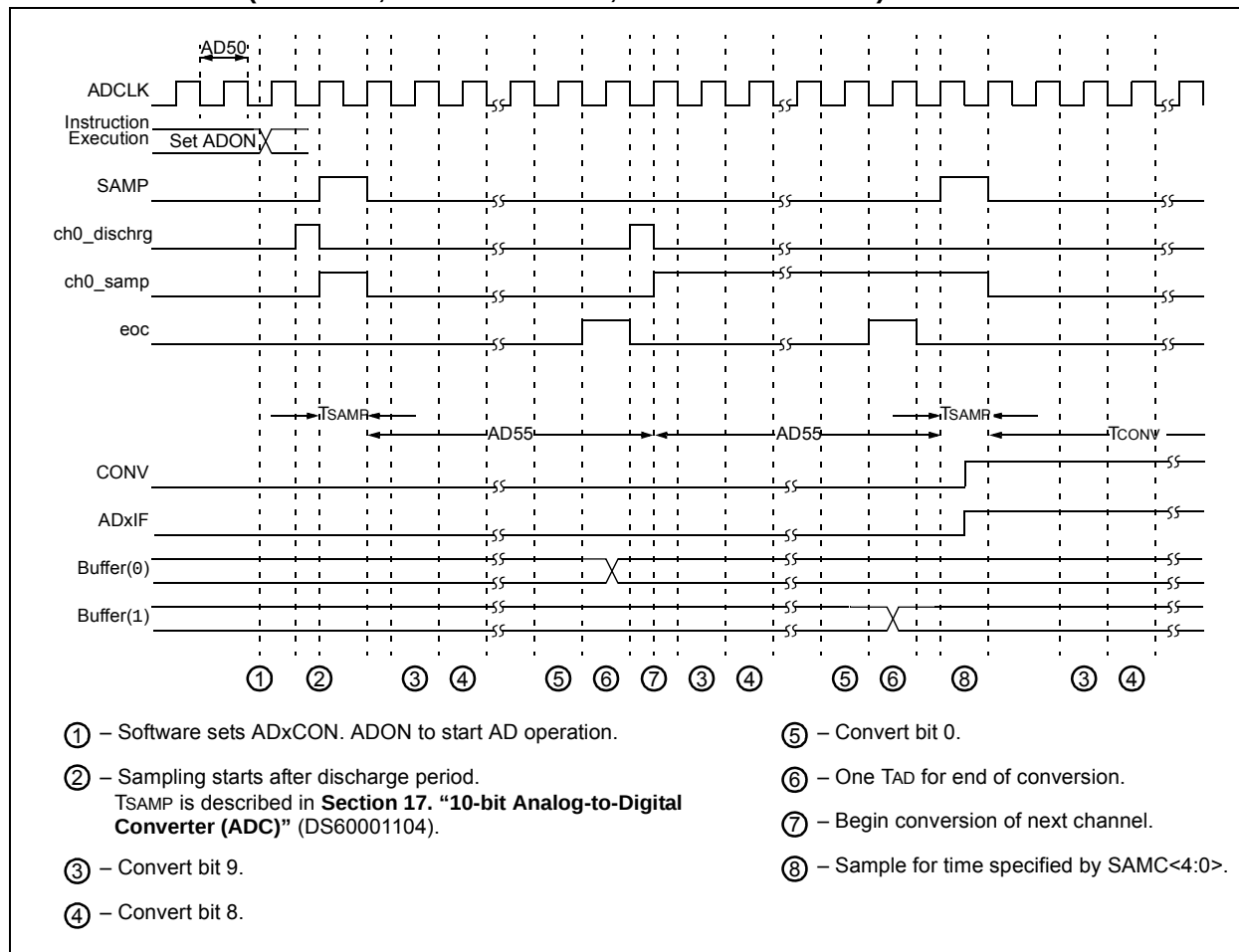
Note 1: BRG is the value of the I²C Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 30-19: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 1, SSRC<2:0> = 111, SAMC<4:0> = 00001)



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 30-23: EJTAG TIMING CHARACTERISTICS

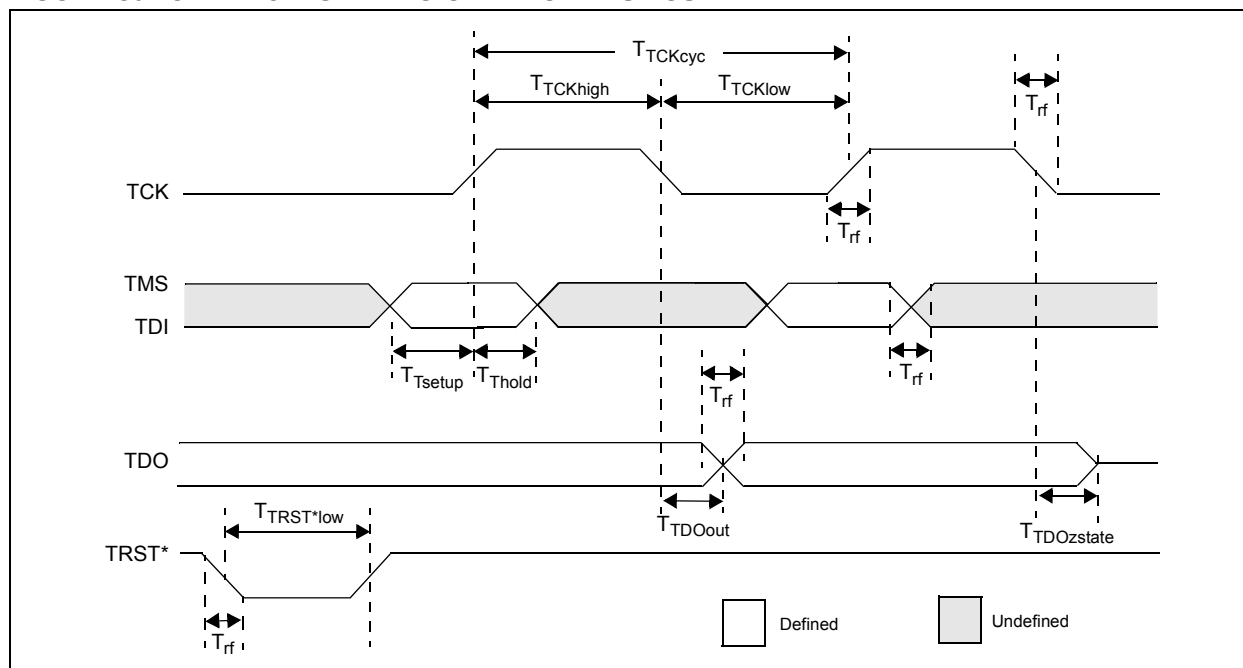


TABLE 30-42: EJTAG TIMING REQUIREMENTS

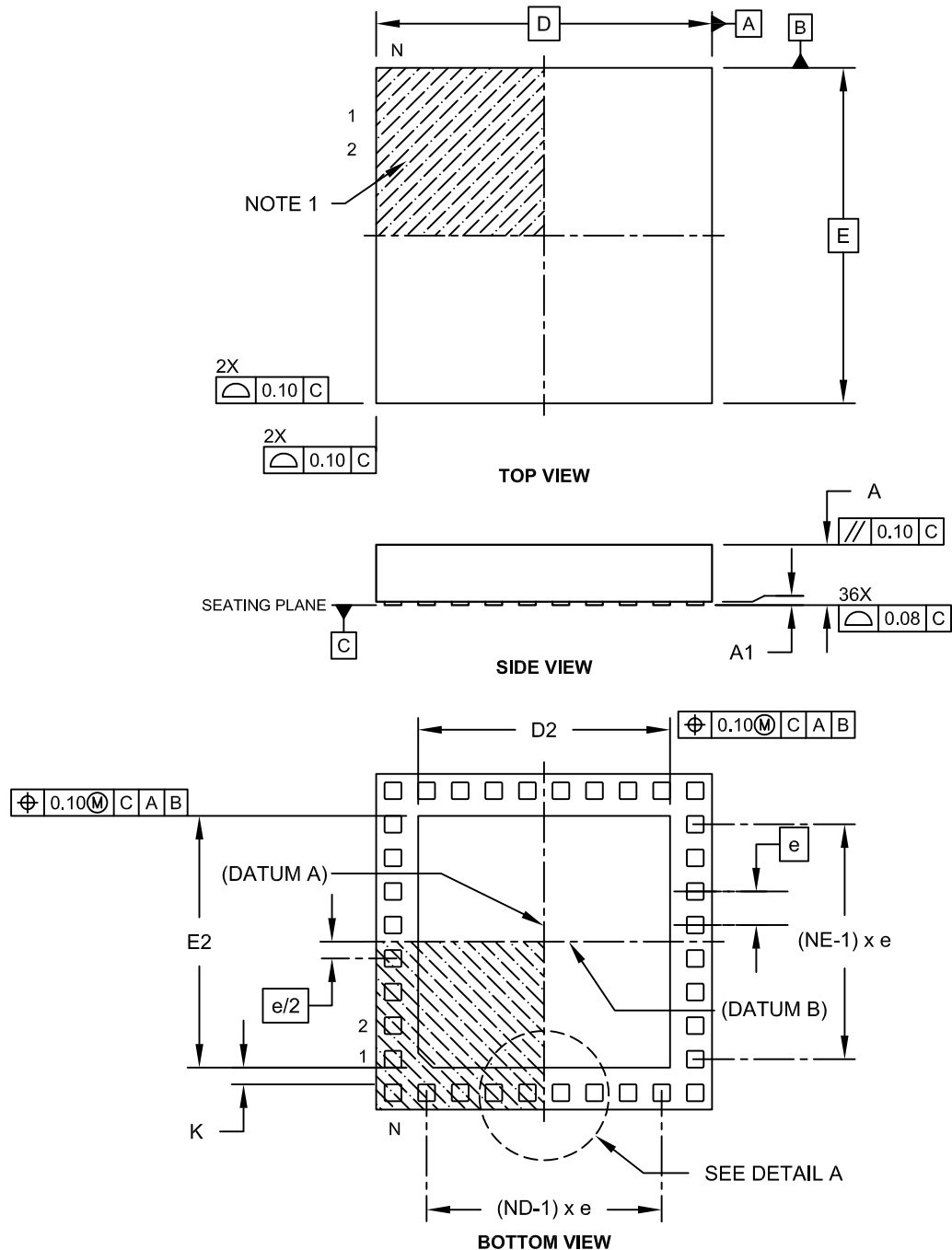
AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp			
Param. No.	Symbol	Description ⁽¹⁾	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

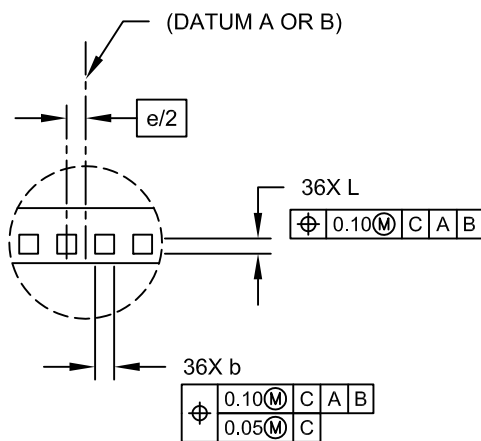


Microchip Technology Drawing C04-187C Sheet 1 of 2

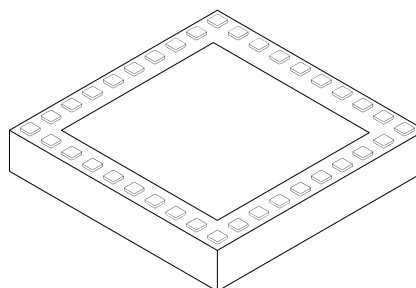
PIC32MX1XX/2XX 28/36/44-PIN FAMILY

36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



DETAIL A



Dimension	Units	MILLIMETERS		
	Limits	MIN	NOM	MAX
Number of Pins	N	36		
Number of Pins per Side	ND	10		
Number of Pins per Side	NE	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.025	-	0.075
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.60	3.75	3.90
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.60	3.75	3.90
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

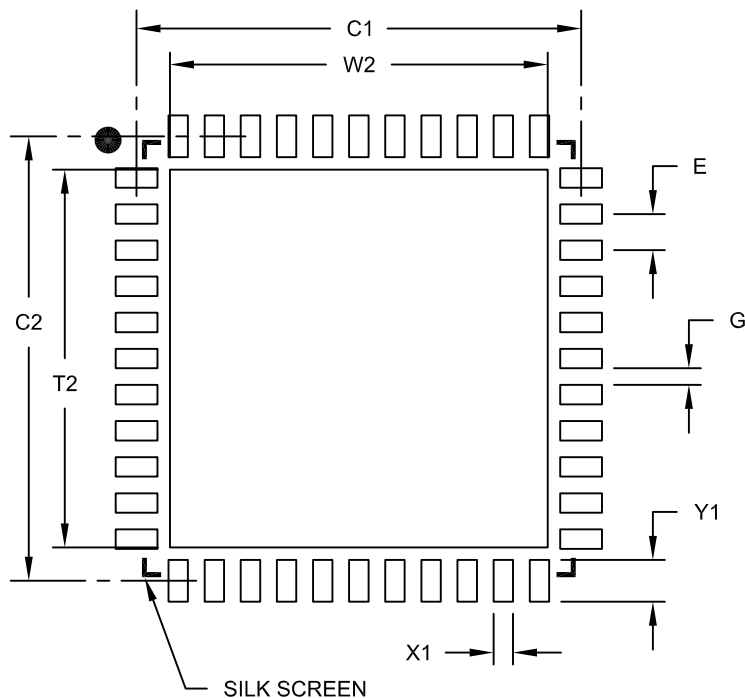
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Revision G (April 2015)

This revision includes the addition of the following devices:

- PIC32MX130F256B
- PIC32MX230F256B
- PIC32MX130F256D
- PIC32MX230F256D

The title of the document was updated to avoid confusion with the PIC32MX1XX/2XX/5XX 64/100-pin Family data sheet.

All peripheral SFR maps have been relocated from the Memory chapter to their respective peripheral chapters.

In addition, this revision includes the following major changes as described in Table A-6, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-6: MAJOR SECTION UPDATES

Section	Update Description
32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see Pin Diagrams).
2.0 “Guidelines for Getting Started with 32-bit MCUs”	Updated these sections: 2.2 “Decoupling Capacitors” , 2.3 “Capacitor on Internal Voltage Regulator (VCAP)” , 2.4 “Master Clear (MCLR) Pin” , 2.8.1 “Crystal Oscillator Design Consideration”
4.0 “Memory Organization”	Added Memory Map for new devices (see Figure 4-6).
14.0 “Watchdog Timer (WDT)”	New chapter created from content previously located in the Special Features chapter.
30.0 “Electrical Characteristics”	Removed parameter D312 (TSET) from the Comparator Specifications (see Table 30-12). Added the Comparator Voltage Reference Specifications (see Table 30-13). Updated Table 30-12.

Revision H (July 2015)

This revision includes the following major changes as described in Table A-7, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-7: MAJOR SECTION UPDATES

Section	Update Description
2.0 “Guidelines for Getting Started with 32-bit MCUs”	Section 2.9 “Sosc Design Recommendation” was removed.
8.0 “Oscillator Configuration”	The Primary Oscillator (Posc) logic in the Oscillator diagram was updated (see Figure 8-1).
30.0 “Electrical Characteristics”	The Power-Down Current (IPD) DC Characteristics parameter DC40k was updated (see Table 30-7). Table 30-9: “DC Characteristics: I/O Pin Input Injection current Specifications” was added.

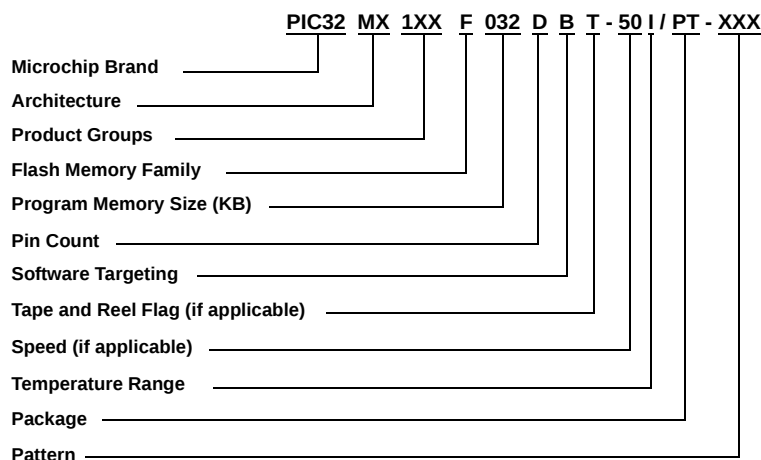
PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MX110F032DT-I/PT:
General purpose PIC32,
32-bit RISC MCU with M4K® core,
32 KB program memory, 44-pin,
Industrial temperature,
TQFP package.

Flash Memory Family

Architecture	MX = M4K® MCU core
Product Groups	1XX = General purpose microcontroller family 2XX = General purpose microcontroller family
Flash Memory Family	F = Flash program memory
Program Memory Size	016 = 16K 032 = 32K 064 = 64K 128 = 128K 256 = 256K
Pin Count	B = 28-pin C = 36-pin D = 44-pin
Software Targeting	B = Targeted for Bluetooth® Audio Break-in devices
Speed	() = 40 MHz – () indicates a blank field; package markings for 40 MHz devices do not include the Speed 50 = 50 MHz
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-temp)
Package	ML = 28-Lead (6x6 mm) QFN (Plastic Quad Flatpack) ML = 44-Lead (8x8 mm) QFN (Plastic Quad Flatpack) PT = 44-Lead (10x10x1 mm) TQFP (Plastic Thin Quad Flatpack) SO = 28-Lead (7.50 mm) SOIC (Plastic Small Outline) SP = 28-Lead (300 mil) SPDIP (Skinny Plastic Dual In-line) SS = 28-Lead (5.30 mm) SSOP (Plastic Shrink Small Outline) TL = 36-Lead (5x5 mm) VTLA (Very Thin Leadless Array) TL = 44-Lead (6x6 mm) VTLA (Very Thin Leadless Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample