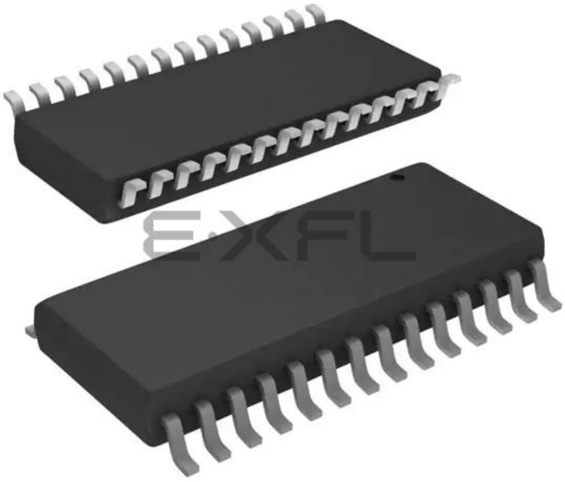
# Microchip Technology - PIC32MX120F032BT-V/SO Datasheet



**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 40MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SOIC (0.295", 7.50mm Width) |
| Supplier Device Package | 28-SOIC |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032bt-v-so |

## TABLE 8: PIN NAMES FOR 36-PIN USB DEVICES

### 36-PIN VTLA (TOP VIEW)(1,2,3,5)

**PIC32MX210F016C**
**PIC32MX220F032C**
**PIC32MX230F064C**
**PIC32MX250F128C**

36

1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 19 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 | 20 | RPC9/CTED7/RC9 |
| 3 | PGED4(4)/AN6/RPC0/RC0 | 21 | VSS |
| 4 | PGEC4(4)/AN7/RPC1/RC1 | 22 | VCAP |
| 5 | VDD | 23 | VDD |
| 6 | VSS | 24 | PGED2/RPB10/D+/CTED11/RB10 |
| 7 | OSC1/CLKI/RPA2/RA2 | 25 | PGEC2/RPB11/D-/RB11 |
| 8 | OSC2/CLKO/RPA3/PMA0/RA3 | 26 | VUSB3V3 |
| 9 | SOSCI/RPB4/RB4 | 27 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 10 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 28 | CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14 |
| 11 | AN12/RPC3/RC3 | 29 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 12 | VSS | 30 | AVSS |
| 13 | VDD | 31 | AVDD |
| 14 | VDD | 32 | $\overline{\text{MCLR}}$ |
| 15 | TMS/RPB5/USBID/RB5 | 33 | PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 |
| 16 | VBUS | 34 | PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 |
| 17 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 35 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 |
| 18 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 36 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 “I/O Ports”** for more information.
**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
**4:** This pin function is not available on PIC32MX210F016C and PIC32MX120F032C devices.
**5:** Shaded pins are 5V tolerant.

## Table of Contents

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| USBID | 11(3) | 14(3) | 15(3) | 41(3) | I | ST | USB OTG ID detect |
| CTED1 | 27 | 2 | 33 | 19 | I | ST | CTMU External Edge Input |
| CTED2 | 28 | 3 | 34 | 20 | I | ST | |
| CTED3 | 13 | 16 | 17 | 43 | I | ST | |
| CTED4 | 15 | 18 | 19 | 1 | I | ST | |
| CTED5 | 22 | 25 | 28 | 14 | I | ST | |
| CTED6 | 23 | 26 | 29 | 15 | I | ST | |
| CTED7 | — | — | 20 | 5 | I | ST | |
| CTED8 | — | — | — | 13 | I | ST | |
| CTED9 | 9 | 12 | 10 | 34 | I | ST | |
| CTED10 | 14 | 17 | 18 | 44 | I | ST | |
| CTED11 | 18 | 21 | 24 | 8 | I | ST | |
| CTED12 | 2 | 5 | 36 | 22 | I | ST | |
| CTED13 | 3 | 6 | 1 | 23 | I | ST | |
| CTPLS | 21 | 24 | 27 | 11 | O | — | CTMU Pulse Output |
| PGED1 | 1 | 4 | 35 | 21 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 1 |
| PGEC1 | 2 | 5 | 36 | 22 | I | ST | Clock input pin for Programming/Debugging Communication Channel 1 |
| PGED2 | 18 | 21 | 24 | 8 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 2 |
| PGEC2 | 19 | 22 | 25 | 9 | I | ST | Clock input pin for Programming/Debugging Communication Channel 2 |
| PGED3 | 11(2)<br>27(3) | 14(2)<br>2(3) | 15(2)<br>33(3) | 41(2)<br>19(3) | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 3 |
| PGEC3 | 12(2)<br>28(3) | 15(2)<br>3(3) | 16(2)<br>34(3) | 42(2)<br>20(3) | I | ST | Clock input pin for Programming/ Debugging Communication Channel 3 |
| PGED4 | — | — | 3 | 12 | I/O | ST | Data I/O pin for Programming/Debugging Communication Channel 4 |
| PGEC4 | — | — | 4 | 13 | I | ST | Clock input pin for Programming/ Debugging Communication Channel 4 |

**Legend:** CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
TTL = TTL input buffer
Analog = Analog input
O = Output
PPS = Peripheral Pin Select
P = Power
I = Input
— = N/A

**Note 1:** Pin numbers are provided for reference only. See the **“Pin Diagrams”** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

## 6.1 Reset Control Registers

### TABLE 6-1: RESET CONTROL REGISTER MAP

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| F600 | RCON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | CMR | VREGS | EXTR | SWR | — | WDTO | SLEEP | IDLE | BOR | POR | xxxx(2) |
| F610 | RSWRST | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SWRST | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 “CLR, SET and INV Registers”** for more information.

**2:** Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

**REGISTER 10-4: U1OTGCON: USB OTG CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | DPPULUP | DMPULUP | DPPULDWN | DMPULDWN | VBUSON | OTGEN | VBUSCHG | VBUSDIS |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as ‘`0`’

bit 7 **DPPULUP:** D+ Pull-Up Enable bit
`1` = D+ data line pull-up resistor is enabled
`0` = D+ data line pull-up resistor is disabled

bit 6 **DMPULUP:** D- Pull-Up Enable bit
`1` = D- data line pull-up resistor is enabled
`0` = D- data line pull-up resistor is disabled

bit 5 **DPPULDWN:** D+ Pull-Down Enable bit
`1` = D+ data line pull-down resistor is enabled
`0` = D+ data line pull-down resistor is disabled

bit 4 **DMPULDWN:** D- Pull-Down Enable bit
`1` = D- data line pull-down resistor is enabled
`0` = D- data line pull-down resistor is disabled

bit 3 **VBUSON:** VBUS Power-on bit
`1` = VBUS line is powered
`0` = VBUS line is not powered

bit 2 **OTGEN:** OTG Functionality Enable bit
`1` = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
`0` = DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

bit 1 **VBUSCHG:** VBUS Charge Enable bit
`1` = VBUS line is charged through a pull-up resistor
`0` = VBUS line is not charged through a resistor

bit 0 **VBUSDIS:** VBUS Discharge Enable bit
`1` = VBUS line is discharged through a pull-down resistor
`0` = VBUS line is not discharged through a resistor

**TABLE 11-2: OUTPUT PIN SELECTION**

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|---|---|---|---|
| RPA0 | RPA0R | RPA0R<3:0> | `0000` = No Connect<br>`0001` = U1TX<br>`0010` = $\overline{\text{U2RTS}}$<br>`0011` = SS1<br>`0100` = Reserved<br>`0101` = OC1<br>`0110` = Reserved<br>`0111` = C2OUT<br>`1000` = Reserved<br>•<br>•<br>•<br>`1111` = Reserved |
| RPB3 | RPB3R | RPB3R<3:0> | |
| RPB4 | RPB4R | RPB4R<3:0> | |
| RPB15 | RPB15R | RPB15R<3:0> | |
| RPB7 | RPB7R | RPB7R<3:0> | |
| RPC7 | RPC7R | RPC7R<3:0> | |
| RPC0 | RPC0R | RPC0R<3:0> | |
| RPC5 | RPC5R | RPC5R<3:0> | |
| RPA1 | RPA1R | RPA1R<3:0> | `0000` = No Connect<br>`0001` = Reserved<br>`0010` = Reserved<br>`0011` = SDO1<br>`0100` = SDO2<br>`0101` = OC2<br>`0110` = Reserved<br>`0111` = C3OUT<br>•<br>•<br>•<br>`1111` = Reserved |
| RPB5 | RPB5R | RPB5R<3:0> | |
| RPB1 | RPB1R | RPB1R<3:0> | |
| RPB11 | RPB11R | RPB11R<3:0> | |
| RPB8 | RPB8R | RPB8R<3:0> | |
| RPA8 | RPA8R | RPA8R<3:0> | |
| RPC8 | RPC8R | RPC8R<3:0> | |
| RPA9 | RPA9R | RPA9R<3:0> | |
| RPA2 | RPA2R | RPA2R<3:0> | `0000` = No Connect<br>`0001` = Reserved<br>`0010` = Reserved<br>`0011` = SDO1<br>`0100` = SDO2<br>`0101` = OC4<br>`0110` = OC5<br>`0111` = REFCLKO<br>`1000` = Reserved<br>•<br>•<br>•<br>`1111` = Reserved |
| RPB6 | RPB6R | RPB6R<3:0> | |
| RPA4 | RPA4R | RPA4R<3:0> | |
| RPB13 | RPB13R | RPB13R<3:0> | |
| RPB2 | RPB2R | RPB2R<3:0> | |
| RPC6 | RPC6R | RPC6R<3:0> | |
| RPC1 | RPC1R | RPC1R<3:0> | |
| RPC3 | RPC3R | RPC3R<3:0> | |
| RPA3 | RPA3R | RPA3R<3:0> | `0000` = No Connect<br>`0001` = $\overline{\text{U1RTS}}$<br>`0010` = U2TX<br>`0011` = Reserved<br>`0100` = $\overline{\text{SS2}}$<br>`0101` = OC3<br>`0110` = Reserved<br>`0111` = C1OUT<br>`1000` = Reserved<br>•<br>•<br>•<br>`1111` = Reserved |
| RPB14 | RPB14R | RPB14R<3:0> | |
| RPB0 | RPB0R | RPB0R<3:0> | |
| RPB10 | RPB10R | RPB10R<3:0> | |
| RPB9 | RPB9R | RPB9R<3:0> | |
| RPC9 | RPC9R | RPC9R<3:0> | |
| RPC2 | RPC2R | RPC2R<3:0> | |
| RPC4 | RPC4R | RPC4R<3:0> | |

**REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | SPISGNEXT | — | — | FRMERREN | SPIROVEN | SPITUREN | IGNROV | IGNTUR |
| 7:0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| | AUDEN(1) | — | — | — | AUDMONO(1,2) | — | AUDMOD<1:0>(1,2) | |

**Legend:**
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
1 = Data from RX FIFO is sign extended
0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as ‘0’

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
1 = Frame Error overflow generates error events
0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
1 = Receive overflow generates error events
0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
1 = Transmit underrun generates error events
0 = Transmit underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
0 = A ROV is a critical error that stops SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
0 = A TUR is a critical error that stops SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
1 = Audio protocol enabled
0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as ‘0’

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
1 = Audio data is mono (Each data word is transmitted on both left and right channels)
0 = Audio data is stereo

bit 2 **Unimplemented:** Read as ‘0’

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
11 = PCM/DSP mode
10 = Right-Justified mode
01 = Left-Justified mode
00 = I$^2$S mode

**Note 1:** This bit can only be written when the ON bit = 0.
**2:** This bit is only valid for AUDEN = 1.

### REGISTER 18-1: I2CxCON: I$^2$C CONTROL REGISTER

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | R/W-0 | R/W-1, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | ON(1) | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC | R/W-0, HC |
| | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |

| **Legend:** | HC = Cleared in Hardware | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as ‘0’

bit 15 **ON:** I$^2$C Enable bit(1)
1 = Enables the I$^2$C module and configures the SDA and SCL pins as serial port pins
0 = Disables the I$^2$C module; all I$^2$C pins are controlled by PORT functions

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **SIDL:** Stop in Idle Mode bit
1 = Discontinue module operation when the device enters Idle mode
0 = Continue module operation when the device enters Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I$^2$C slave)
1 = Release SCLx clock
0 = Hold SCLx clock low (clock stretch)

If STREN = 1:
Bit is R/W (i.e., software can write ‘0’ to initiate stretch and write ‘1’ to release clock). Hardware clear at beginning of slave transmission. Hardware clear at end of slave reception.

If STREN = 0:
Bit is R/S (i.e., software can only write ‘1’ to release clock). Hardware clear at beginning of slave transmission.

bit 11 **STRICT:** Strict I$^2$C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced. Device does not respond to reserved address space or generate addresses in reserved address space.
0 = Strict I$^2$C Reserved Address Rule not enabled

bit 10 **A10M:** 10-bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control disabled
0 = Slew rate control enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enable I/O pin thresholds compliant with SMBus specification
0 = Disable SMBus input thresholds

**Note 1:** When using 1:1 PBCLK divisor, the user’s software should not read/write the peripheral’s SFRs in the SYSCLK cycle immediately following the instruction that clears the module’s ON bit.

**NOTES:**

**NOTES:**

### REGISTER 27-1: DEVCFG0: DEVICE CONFIGURATION WORD 0

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-0 | r-1 | r-1 | R/P | r-1 | r-1 | r-1 | R/P |
| | — | — | — | CP | — | — | — | BWP |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | — | — | — | — | — | PWP<8:6>(3) | | |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | r-1 | r-1 |
| | PWP<5:0> | | | | | | — | — |
| 7:0 | r-1 | r-1 | r-1 | R/P | R/P | R/P | R/P | R/P |
| | — | — | — | ICESEL<1:0>(2) | | JTAGEN(1) | DEBUG<1:0> | |

| | | | |
|---|---|---|---|
| **Legend:** | r = Reserved bit | P = Programmable bit | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

| | |
|---|---|
| bit 31 | **Reserved:** Write ‘`0`’ |
| bit 30-29 | **Reserved:** Write ‘`1`’ |
| bit 28 | **CP:** Code-Protect bit<br>Prevents boot and program Flash memory from being read or modified by an external programming device.<br>`1` = Protection is disabled<br>`0` = Protection is enabled |
| bit 27-25 | **Reserved:** Write ‘`1`’ |
| bit 24 | **BWP:** Boot Flash Write-Protect bit<br>Prevents boot Flash memory from being modified during code execution.<br>`1` = Boot Flash is writable<br>`0` = Boot Flash is not writable |
| bit 23-19 | **Reserved:** Write ‘`1`’ |

**Note 1:** This bit sets the value for the JTAGEN bit in the CFGCON register.

**2:** The PGEC4/PGED4 pin pair is not available on all devices. Refer to the **“Pin Diagrams”** section for availability.

**3:** The PWP<8:7> bits are only available on devices with 256 KB Flash.

**TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage (Note 2)** | 2.3 | — | 3.6 | V | — |
| DC12 | VDR | **RAM Data Retention Voltage (Note 1)** | 1.75 | — | — | V | — |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | 1.75 | — | 2.1 | V | — |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.00005 | — | 0.115 | V/µs | — |

**Note 1:** This is the limit to which VDD can be lowered without losing RAM data.

**2:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

### TABLE 30-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ $T_A$ ≤ +85°C for Industrial<br>-40°C ≤ $T_A$ ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DO10 | $V_{OL}$ | **Output Low Voltage**<br>I/O Pins | — | — | 0.4 | V | $I_{OL}$ ≤ 10 mA, $V_{DD}$ = 3.3V |
| DO20 | $V_{OH}$ | **Output High Voltage**<br>I/O Pins | 1.5(1) | — | — | V | $I_{OH}$ ≥ -14 mA, $V_{DD}$ = 3.3V |
| | | | 2.0(1) | — | — | | $I_{OH}$ ≥ -12 mA, $V_{DD}$ = 3.3V |
| | | | 2.4 | — | — | | $I_{OH}$ ≥ -10 mA, $V_{DD}$ = 3.3V |
| | | | 3.0(1) | — | — | | $I_{OH}$ ≥ -7 mA, $V_{DD}$ = 3.3V |

**Note 1:** Parameters are characterized, but not tested.

### TABLE 30-11: ELECTRICAL CHARACTERISTICS: BOR

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ $T_A$ ≤ +85°C for Industrial<br>-40°C ≤ $T_A$ ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.(1)** | **Typical** | **Max.** | **Units** | **Conditions** |
| BO10 | $V_{BOR}$ | BOR Event on $V_{DD}$ transition high-to-low(2) | 2.0 | — | 2.3 | V | — |

**Note 1:** Parameters are for design guidance only and are not tested in manufacturing.

**2:** Overall functional device operation at $V_{BORMIN}$ < $V_{DD}$ < $V_{DDMIN}$ is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below $V_{DDMIN}$.

**FIGURE 30-5: EXTERNAL RESET TIMING CHARACTERISTICS**

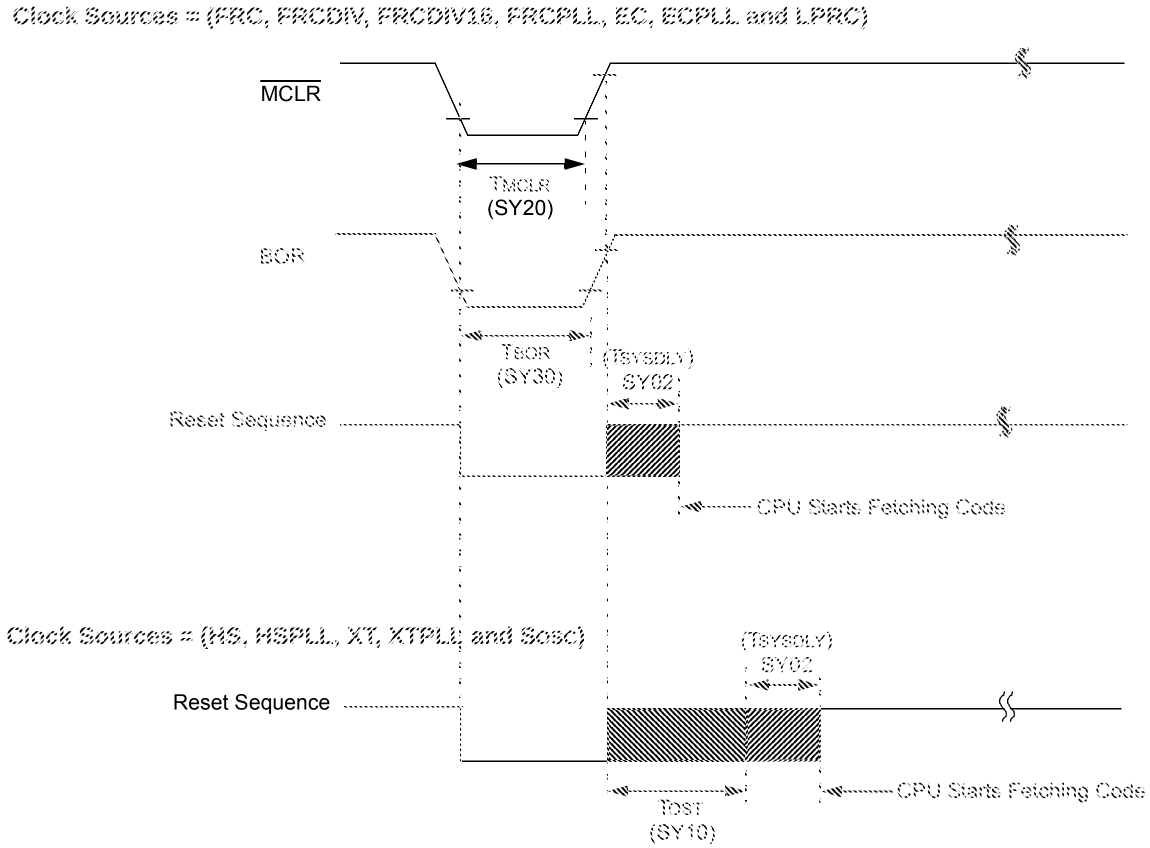


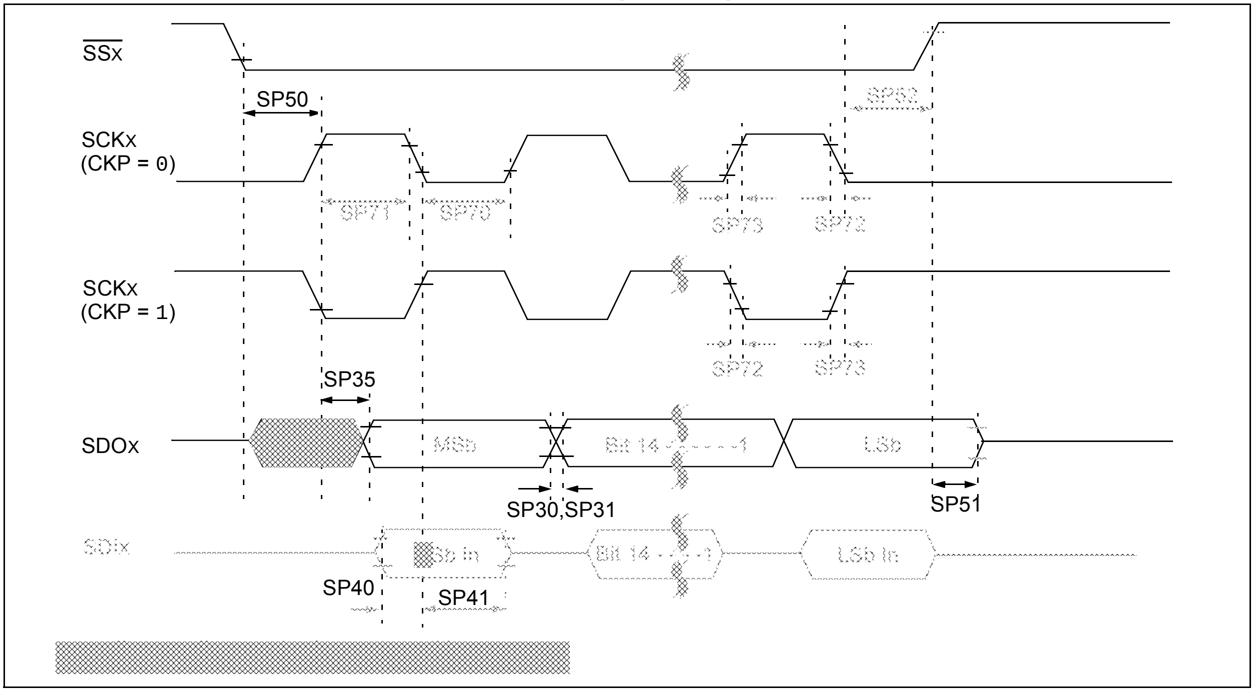
**TABLE 30-22: RESETS TIMING**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics[1]** | **Min.** | **Typical[2]** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period<br>Internal Voltage Regulator Enabled | — | 400 | 600 | µs | — |
| SY02 | TSYSDLY | System Delay Period:<br>Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched. | — | 1 µs +<br>8 SYSCLK cycles | — | — | — |
| SY20 | TMCLR | $\overline{\text{MCLR}}$ Pulse Width (low) | 2 | — | — | µs | — |
| SY30 | TBOR | BOR Pulse Width (low) | — | 1 | — | µs | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

### FIGURE 30-12: SPIx MODULE SLAVE MODE (CKE = `0`) TIMING CHARACTERISTICS



### TABLE 30-30: SPIx MODULE SLAVE MODE (CKE = `0`) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics[1]** | **Min.** | **Typ.[2]** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | — | — | ns | See parameter DO32 |
| SP73 | TscR | SCKx Input Rise Time | — | — | — | ns | See parameter DO31 |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV,<br>TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 15 | ns | Vdd > 2.7V |
| | | | — | — | 20 | ns | Vdd < 2.7V |
| SP40 | TdiV2scH,<br>TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL,<br>TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH,<br>TssL2scL | $\overline{\text{SSx}}$ ↓ to SCKx ↑ or SCKx Input | 175 | — | — | ns | — |
| SP51 | TssH2doZ | $\overline{\text{SSx}}$ ↑ to SDOx Output High-Impedance **(Note 3)** | 5 | — | 25 | ns | — |
| SP52 | TscH2ssH<br>TscL2ssH | $\overline{\text{SSx}}$ after SCKx Edge | Tsck + 20 | — | — | ns | — |

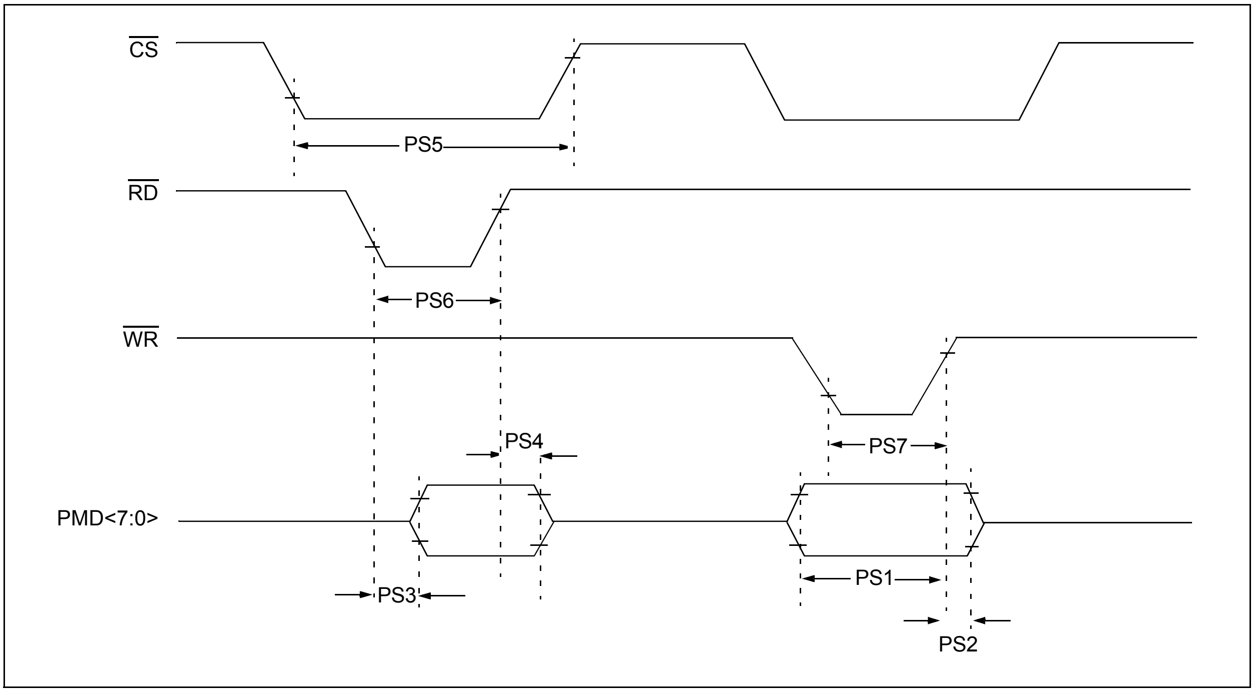
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 30-20: PARALLEL SLAVE PORT TIMING**



### TABLE 31-3: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | |
|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| **Idle Current (IIDLE): Core Off, Clock on Base Current (Note 1)** | | | | |
| MDC34a | 8 | 13 | mA | 50 MHz |

**Note 1:** The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = `1`
- No peripheral modules are operating, (ON bit = `0`), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

### TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | | |
|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | |
| **Power-Down Current (IPD) (Note 1)** | | | | | |
| MDC40k | 10 | 25 | μA | -40°C | Base Power-Down Current |
| MDC40n | 250 | 500 | μA | +85°C | |
| **Module Differential Current** | | | | | |
| MDC41e | 10 | 55 | μA | 3.6V | Watchdog Timer Current: ΔIWDT **(Note 3)** |
| MDC42e | 23 | 55 | μA | 3.6V | RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC **(Note 3)** |
| MDC43d | 1100 | 1300 | μA | 3.6V | ADC: ΔIADC **(Notes 3,4)** |

**Note 1:** The test conditions for IPD current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = `1`
- No peripheral modules are operating, (ON bit = `0`), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

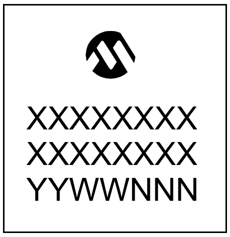
**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**NOTES:**

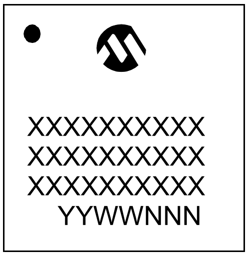
### 33.1 Package Marking Information (Continued)

36-Lead VTLA

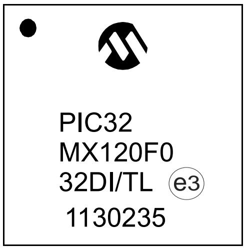


Example

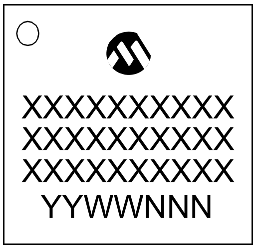
44-Lead VTLA



Example

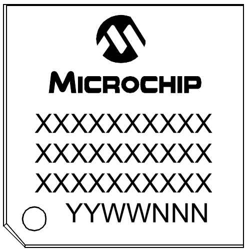


44-Lead QFN

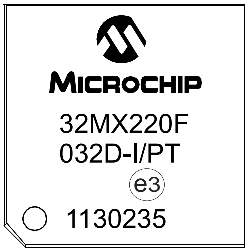


Example

44-Lead TQFP



Example

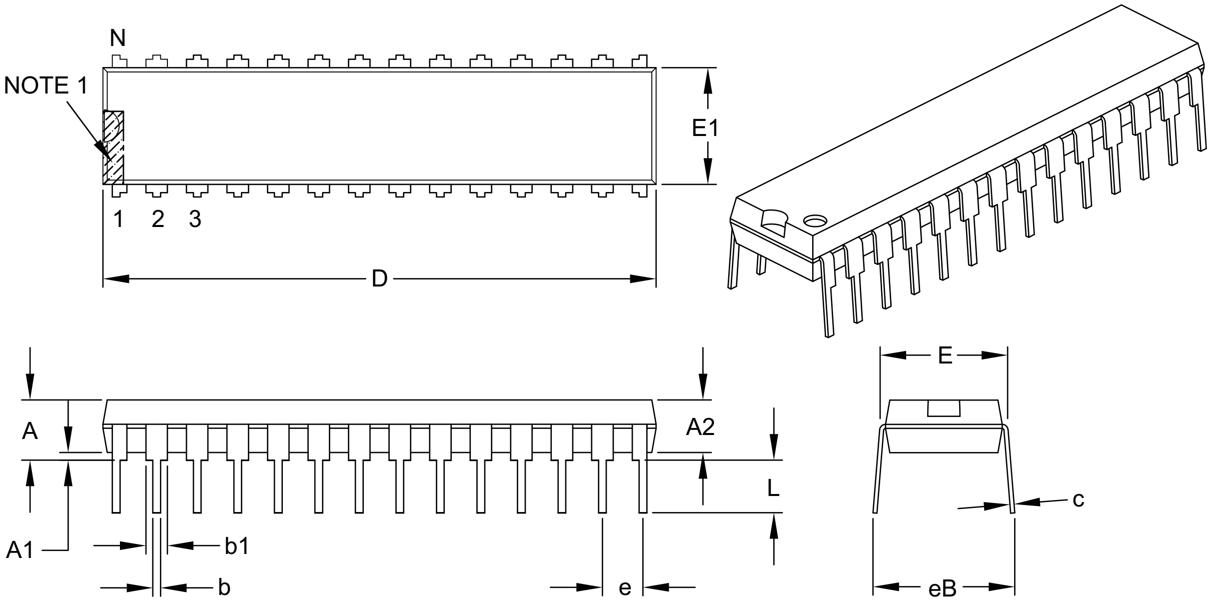


| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

**Note:** If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 28 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B