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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032c-50i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e[®] Support
- · Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- · 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1:MIPS32[®] M4K[®] PROCESSOR CORE HIGH-PERFORMANCE INTEGERMULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul rt) (div rs)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU,	16 bits	1	1
MSUB/MSUBU	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

-								
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	_	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	_	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
15:8	BMXDUDBA<15:8>							
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				BMXDU	DBA<7:0>			

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Legend:

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUDBA<15:10>: DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 BMXDUDBA<9:0>: Read-Only bits This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 5. "Flash Program Memory" (DS60001121), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family devices contain an internal Flash program memory for executing user code. There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming[™] (ICSP[™])

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is available in **Section 5. "Flash Program Memory"** (DS60001121) in the *"PIC32 Family Reference Manual"*.

EJTAG is performed using the EJTAG port of the device and an EJTAG capable programmer.

ICSP is performed using a serial data connection to the device and allows much faster programming times than RTSP.

The EJTAG and ICSP methods are described in the "*PIC32 Flash Programming Specification*" (DS60001145), which can be downloaded from the Microchip web site.

Note: The Flash page size on PIC32MX-1XX/2XX 28/36/44-pin Family devices is 1 KB and the row size is 128 bytes (256 IW and 32 IW, respectively).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0						
31:24	—	—	—	—	—	—	—	—
22.40	U-0	U-0						
23:10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0, HS	R/W-0
10.0	—	—	—	—	—	—	CMR	VREGS
	R/W-0, HS	R/W-0, HS	U-0	R/W-0, HS	R/W-0, HS	R/W-0, HS	R/W-1, HS	R/W-1, HS
7:0	EXTR	SWR	_	WDTO	SLEEP	IDLE	BOR ⁽¹⁾	POR ⁽¹⁾

REGISTER 6-1: RCON: RESET CONTROL REGISTER

Legend:	HS = Set by hardware			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-10 Unimplemented: Read as '0'

bit 9	CMR: Configuration Mismatch Reset Flag bit
	1 = Configuration mismatch Reset has occurred
	0 = Configuration mismatch Reset has not occurred
bit 8	VREGS: Voltage Regulator Standby Enable bit
	1 = Regulator is enabled and is on during Sleep mode
	0 = Regulator is disabled and is off during Sleep mode
bit 7	EXTR: External Reset (MCLR) Pin Flag bit
	1 = Master Clear (pin) Reset has occurred
	0 = Master Clear (pin) Reset has not occurred
bit 6	SWR: Software Reset Flag bit
	1 = Software Reset was executed
	0 = Software Reset as not executed
bit 5	Unimplemented: Read as '0'
bit 4	WDTO: Watchdog Timer Time-out Flag bit
	1 = WDT Time-out has occurred
	0 = WDT Time-out has not occurred
bit 3	SLEEP: Wake From Sleep Flag bit
	1 = Device was in Sleep mode
	0 = Device was not in Sleep mode
bit 2	IDLE: Wake From Idle Flag bit
	1 = Device was in Idle mode
	0 = Device was not in Idle mode
bit 1	BOR: Brown-out Reset Flag bit ⁽¹⁾
	1 = Brown-out Reset has occurred
	0 = Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit ⁽¹⁾
	1 = Power-on Reset has occurred
	0 = Power-on Reset has not occurred

Note 1: User software must clear this bit to view next detection.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	—	—	—	—	—	—	—	—	
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:10	_	—	_	—	—	_	_	_	
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
15:8	_	_	_	—	—	—	_	—	
7.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC	
7:0	_	_	_	_	_	_	_	SWRST ⁽¹⁾	

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Legend:	HC = Cleared by hardware				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 31-1 Unimplemented: Read as '0'

bit 0 SWRST: Software Reset Trigger bit⁽¹⁾ 1 = Enable Software Reset event

0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	_	—	_		_	—	_	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	_	—	_		_	—	_	—
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	STALLIE				TRNIE	SOFIE		URSTIE ⁽²⁾
	OTALLIL			IDELIE		OOLIE	OLIVIL	DETACHIE ⁽³⁾

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	STALLIE: STALL	Handshake	Interrupt Enable	bit

- 1 = STALL interrupt is enabled
- 0 = STALL interrupt is disabled
- bit 6 ATTACHIE: ATTACH Interrupt Enable bit
 - 1 = ATTACH interrupt is enabled 0 = ATTACH interrupt is disabled
- bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
 - 1 = RESUME interrupt is enabled
 - 0 = RESUME interrupt is disabled
- bit 4 IDLEIE: Idle Detect Interrupt Enable bit
 - 1 = Idle interrupt is enabled
 - 0 = Idle interrupt is disabled
- bit 3 TRNIE: Token Processing Complete Interrupt Enable bit
 - 1 = TRNIF interrupt is enabled
 - 0 = TRNIF interrupt is disabled
- bit 2 SOFIE: SOF Token Interrupt Enable bit
 - 1 = SOFIF interrupt is enabled
 - 0 = SOFIF interrupt is disabled
- bit 1 UERRIE: USB Error Interrupt Enable bit⁽¹⁾
 - 1 = USB Error interrupt is enabled
 - 0 = USB Error interrupt is disabled
- bit 0 URSTIE: USB Reset Interrupt Enable bit⁽²⁾
 - 1 = URSTIF interrupt is enabled
 - 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit⁽³⁾

- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE (U1IE<1>) bit must be set.

- 2: Device mode.
- 3: Host mode.

TABLE 11-2: OUTPUT PIN SELECTION

RPn Port Pin	RPnR SFR	RPnR bits	RPnR Value to Peripheral Selection				
RPA0	RPA0R	RPA0R<3:0>	0000 = No Connect				
RPB3	RPB3R	RPB3R<3:0>	0001 = 011X 0010 = 02RTS				
RPB4	RPB4R	RPB4R<3:0>	0011 = SS1				
RPB15	RPB15R	RPB15R<3:0>	0100 = Reserved 0101 = OC1				
RPB7	RPB7R	RPB7R<3:0>	0110 = Reserved				
RPC7	RPC7R	RPC7R<3:0>	1000 = Reserved				
RPC0	RPC0R	RPC0R<3:0>].				
RPC5	RPC5R	RPC5R<3:0>	• 1111 = Reserved				
RPA1	RPA1R	RPA1R<3:0>	0000 = No Connect				
RPB5	RPB5R	RPB5R<3:0>	0001 = Reserved 0010 = Reserved				
RPB1	RPB1R	RPB1R<3:0>	0011 = SDO1				
RPB11	RPB11R	RPB11R<3:0>	0100 = SDO2 0101 = OC2				
RPB8	RPB8R	RPB8R<3:0>	0110 = Reserved				
RPA8	RPA8R	RPA8R<3:0>	0111 = C3OOT				
RPC8	RPC8R	RPC8R<3:0>]• •				
RPA9	RPA9R	RPA9R<3:0>	1111 = Reserved				
RPA2	RPA2R	RPA2R<3:0>	0000 = No Connect				
RPB6	RPB6R	RPB6R<3:0>	01 = Reserved 10 = Reserved				
RPA4	RPA4R	RPA4R<3:0>	0011 = SDO1				
RPB13	RPB13R	RPB13R<3:0>	0101 = OC4				
RPB2	RPB2R	RPB2R<3:0>	0110 = OC5 0111 = REFCLKO				
RPC6	RPC6R	RPC6R<3:0>	1000 = Reserved				
RPC1	RPC1R	RPC1R<3:0>	- - -				
RPC3	RPC3R	RPC3R<3:0>	1111 = Reserved				
RPA3	RPA3R	RPA3R<3:0>	0000 = No Connect				
RPB14	RPB14R	RPB14R<3:0>	0010 = U2TX				
RPB0	RPB0R	RPB0R<3:0>	0011 = <u>Res</u> erved 0100 = <u>SS2</u>				
RPB10	RPB10R	RPB10R<3:0>	0101 = OC3				
RPB9	RPB9R	RPB9R<3:0>	0111 = C1OUT				
RPC9	RPC9R	RPC9R<3:0>	1000 = Reserved				
RPC2	RPC2R	RPC2R<3:0>]• •				
RPC4	RPC4R	RPC4R<3:0>	1111 = Reserved				



FIGURE 13-2: TIMER2/3, TIMER4/5 BLOCK DIAGRAM (32-BIT)

Input Capture Control Registers 15.1

AB	LE 15-1:	IN	PUT CA	PTURE	E 1-INPU		URE 5	REGIST	ER MA	2							
ess		â								Bi	ts						
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1
2000		31:16	_		_	_	_	-	—	_	_	-	_	_	_	_	
2000		15:0	ON	_	SIDL	_	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>
2010	IC1BUF	JF 31:16 15:0 IC1BUF<31:0>															
200		31:16	—	—	—	—	_	_	—	—	_	_	—	—	—	—	_
2200 2210	1020011	15:0	ON	—	SIDL	—	_		FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>
	IC2BUF	31:16 15:0								IC2BUF	<31:0>						
2400		31:16	—	_	—	_	—	—	—	—	—	—	_	_	—	_	
2400	IC3CON /	15:0	ON	_	SIDL	-	_	-	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>						
2600		31:16	-	—	_	-	_		—	—	_		_	_		—	
2000	104001	15:0	ON	_	SIDL		—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>
2610	IC4BUF	31:16 15:0								IC4BUF	<31:0>						
2000		31:16	_	_	—	_	_		—	_	_	_	_	—	_	—	_
2000	1000010	15:0	ON	—	SIDL	—	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0>
2810	IC5BUF	31:16 15:0								IC5BUF	<31:0>						

Legend:

x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

All Resets

0000

0000

xxxx xxxx 0000 0000

xxxx xxxx 0000

0000 xxxx xxxx 0000 0000

xxxx xxxx 0000 0000

xxxx xxxx

16/0

—

17.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 23. "Serial Peripheral Interface (SPI)" (DS60001106), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The SPI module is a synchronous serial interface that is useful for communicating with external peripherals and other microcontrollers. These peripheral devices may be Serial EEPROMs, Shift registers, display drivers, Analog-to-Digital Converters (ADC), etc. The PIC32 SPI module is compatible with Motorola[®] SPI and SIOP interfaces. Some of the key features of the SPI module are:

- Master mode and Slave mode support
- Four clock formats
- Enhanced Framed SPI protocol support
- User-configurable 8-bit, 16-bit and 32-bit data width
- Separate SPI FIFO buffers for receive and transmit
 FIFO buffers act as 4/8/16-level deep FIFOs based on 32/16/8-bit data width
- Programmable interrupt event on every 8-bit, 16-bit and 32-bit data transfer
- · Operation during Sleep and Idle modes
- Audio Codec Support:
 - I²S protocol
 - Left-justified
 - Right-justified
 - PCM

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

bit 3 SPITBE: SPI Transmit Buffer Empty Status bit 1 = Transmit buffer, SPIxTXB is empty 0 = Transmit buffer, SPIxTXB is not empty Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB. bit 2 Unimplemented: Read as '0' bit 1 SPITBF: SPI Transmit Buffer Full Status bit 1 = Transmit not yet started, SPITXB is full 0 = Transmit buffer is not full Standard Buffer Mode: Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB. Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR. Enhanced Buffer Mode: Set when CWPTR + 1 = SRPTR; cleared otherwise bit 0 SPIRBF: SPI Receive Buffer Full Status bit 1 = Receive buffer, SPIxRXB is full

0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise

19.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 21. "Universal Asynchronous Receiver Transmitter (UART)" (DS60001107), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The UART module is one of the serial I/O modules available in PIC32MX1XX/2XX 28/36/44-pin Family devices. The UART is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols, such as RS-232, RS-485, LIN, and IrDA[®]. The UART module also supports the hardware flow control option, with UXCTS and UXRTS pins, and also includes an IrDA encoder and decoder.

Key features of the UART module include:

- Full-duplex, 8-bit or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- · One or two Stop bits
- Hardware auto-baud feature
- · Hardware flow control option
- Fully integrated Baud Rate Generator (BRG) with 16-bit prescaler
- Baud rates ranging from 38 bps to 12.5 Mbps at 50 MHz
- 8-level deep First In First Out (FIFO) transmit data buffer
- 8-level deep FIFO receive data buffer
- Parity, framing and buffer overrun error detection
- Support for interrupt-only on address detect (9th bit = 1)
- · Separate transmit and receive interrupts
- Loopback mode for diagnostic support
- · LIN protocol support
- IrDA encoder and decoder with 16x baud clock output for external IrDA encoder/decoder support

Figure 19-1 illustrates a simplified block diagram of the UART module.

FIGURE 19-1: UART SIMPLIFIED BLOCK DIAGRAM

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED) bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit 11 = Reserved; do not use 10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters) 01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters) 00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character) bit 5 ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect. 0 = Address Detect mode is disabled bit 4 **RIDLE:** Receiver Idle bit (read-only) 1 =Receiver is Idle 0 = Data is being received PERR: Parity Error Status bit (read-only) bit 3 1 = Parity error has been detected for the current character 0 = Parity error has not been detected bit 2 FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character 0 = Framing error has not been detected **OERR:** Receive Buffer Overrun Error Status bit. bit 1 This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state. 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)

- 1 = Receive buffer has data, at least one more character can be read
- 0 = Receive buffer is empty

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	ADRML	JX<1:0>	PMPTTL	PTWREN	PTRDEN
7.0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7:0	CSF<	CSF<1:0> ⁽²⁾		_	CS1P ⁽²⁾	_	WRSP	RDSP

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Parallel Master Port Enable bit⁽¹⁾
 - 1 = PMP enabled
 - 0 = PMP disabled, no off-chip access performed
- bit 14 Unimplemented: Read as '0'
- bit 13 **SIDL:** Stop in Idle Mode bit
 - 1 = Discontinue module operation when the device enters Idle mode
 - 0 = Continue module operation when the device enters Idle mode
- bit 12-11 ADRMUX<1:0>: Address/Data Multiplexing Selection bits
 - 11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
 - 10 = All 16 bits of address are multiplexed on PMD<7:0> pins
 - 01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
 - 00 = Address and data appear on separate pins
- bit 10 **PMPTTL:** PMP Module TTL Input Buffer Select bit
 - 1 = PMP module uses TTL input buffers
 - 0 = PMP module uses Schmitt Trigger input buffer
- bit 9 **PTWREN:** Write Enable Strobe Port Enable bit
 - 1 = PMWR/PMENB port enabled
 - 0 = PMWR/PMENB port disabled
- bit 8 PTRDEN: Read/Write Strobe Port Enable bit
 - 1 = PMRD/PMWR port enabled
 - 0 = PMRD/PMWR port disabled
- bit 7-6 CSF<1:0>: Chip Select Function bits⁽²⁾
 - 11 = Reserved
 - 10 = PMCS1 functions as Chip Select
 - 01 = PMCS1 functions as PMA<14>
 - 00 = PMCS1 functions as PMA<14>
- bit 5 ALP: Address Latch Polarity bit⁽²⁾
 - 1 = Active-high (PMALL and PMALH)
 - $0 = \text{Active-low} (\overline{\text{PMALL}} \text{ and } \overline{\text{PMALH}})$
 - **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.
 - 2: These bits have no effect when their corresponding pins are used as address lines.

24.1 Comparator Voltage Reference Control Register

TABLE 24-1:	COMPARATOR VOLTAGE REFERENCE REGISTER MAP
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ess	Register Name ⁽¹⁾ Bit Range	Bits																	
Virtual Addr (BF80_#)		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
0000		31:16	—	—	_	_		_	_	_	_	—	—	_	_	_	—	_	0000
9600	CVRCON	15:0	ON	-	-	_	_	_	—	_	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0000

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

26.0 POWER-SAVING FEATURES

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 10. "Power-
	Saving Features" (DS60001130), which
	is available from the Documentation >
	Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- Sosc Run mode: the CPU is clocked from the Sosc clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- Posc Idle mode: the system clock is derived from the Posc. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- Sosc Idle mode: the system clock is derived from the Sosc. Peripherals continue to operate, but can optionally be individually disabled.

- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See Section 26.3.3 "Peripheral Bus Scaling Method" for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)								
	ARACIER		Operating tempe	erature -4	40°C dTa 40°C dTa	d+85°C d+105°	C for Industrial C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical ⁽¹⁾	Max.	Units	Conditions				
	VIL	Input Low Voltage									
DI10		I/O Pins with PMP	Vss	—	0.15 VDD	V					
		I/O Pins	Vss	—	0.2 Vdd	V					
DI18		SDAx, SCLx	Vss	—	0.3 Vdd	V	SMBus disabled (Note 4)				
DI19		SDAx, SCLx	Vss	_	0.8	V	SMBus enabled (Note 4)				
	VIH	Input High Voltage									
DI20		I/O Pins not 5V-tolerant ⁽⁵⁾	0.65 VDD	—	Vdd	V	(Note 4,6)				
		I/O Pins 5V-tolerant with PMP ⁽⁵⁾	0.25 VDD + 0.8V	_	5.5	V	(Note 4,6)				
		I/O Pins 5V-tolerant ⁽⁵⁾	0.65 VDD	—	5.5	V					
DI28		SDAx, SCLx	0.65 VDD	_	5.5	V	SMBus disabled (Note 4,6)				
DI29		SDAx, SCLx	2.1	_	5.5	V	SMBus enabled, 2.3V dVPIN d5.5 (Note 4,6)				
DI30	ICNPU	Change Notification Pull-up Current	_	—	-50	FA	VDD = 3.3V, VPIN = VSS (Note 3,6)				
DI31	ICNPD	Change Notification Pull-down Current ⁽⁴⁾	_	—	-50	μA	VDD = 3.3V, VPIN = VDD				
	lı∟	Input Leakage Current (Note 3)									
DI50		I/O Ports	_	—	<u>+</u> 1	FA	Vss dVPIN dVDD, Pin at high-impedance				
DI51		Analog Input Pins	_	_	<u>+</u> 1	FA	Vss dVPIN dVDD, Pin at high-impedance				
DI55		MCLR(2)	_	_	<u>+</u> 1	FA	Vss d/pin d/dd				
DI56		OSC1	_	_	<u>+</u> 1	FA	Vss d/PIN dVDD, XT and HS modes				

TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as current sourced by the pin.
- 4: This parameter is characterized, but not tested in manufacturing.
- 5: See the "Pin Diagrams" section for the 5V-tolerant pins.
- 6: The VIH specifications are only in relation to externally applied inputs, and not with respect to the userselectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

TABLE 31-5: EXTERNAL CLOCK TIMING REQUIREMENTS

АС СНА	RACTERI	STICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C dTA d+85°C for Industrial						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions		
MOS10	Fosc	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC 4		50 50	MHz MHz	EC (Note 2) ECPLL (Note 1)		

Note 1: PLL input requirements: 4 MHz dFPLLIN d5 MHz (use PLL prescaler to reduce Fosc). This parameter is characterized, but tested at 10 MHz only at manufacturing.

2: This parameter is characterized, but not tested in manufacturing.

TABLE 31-6: SPIX MASTER MODE (CKE = 0) TIMING REQUIREMENTS

АС СНА	ARACTERIS	rics	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C dTA d+85°C for Industrial							
Param. No.	Symbol	Characteristics	Min. Typical Max. Units Condition							
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	—	ns	_			
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	_	_	ns	_			

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

TABLE 31-7: SPIX MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

АС СНА	ARACTERIS	TICS	Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C dTA d+85°C for Industrial						
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions		
MSP10	TscL	SCKx Output Low Time (Note 1,2)	Тѕск/2	—	_	ns	_		
MSP11	TscH	SCKx Output High Time (Note 1,2)	Тѕск/2	—	—	ns	—		

Note 1: These parameters are characterized, but not tested in manufacturing.

2: The minimum clock period for SCKx is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

DETAIL A

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	N		44		
Number of Pins per Side	ND		12		
Number of Pins per Side	NE		10		
Pitch	е		0.50 BSC		
Overall Height	A	0.80	0.90	1.00	
Standoff	A1	0.025	-	0.075	
Overall Width	E	6.00 BSC			
Exposed Pad Width	E2	4.40	4.55	4.70	
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2	4.40	4.55	4.70	
Contact Width	b	0.20	0.25	0.30	
Contact Length	L	0.20	0.25	0.30	
Contact-to-Exposed Pad	K	0.20	_	_	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2