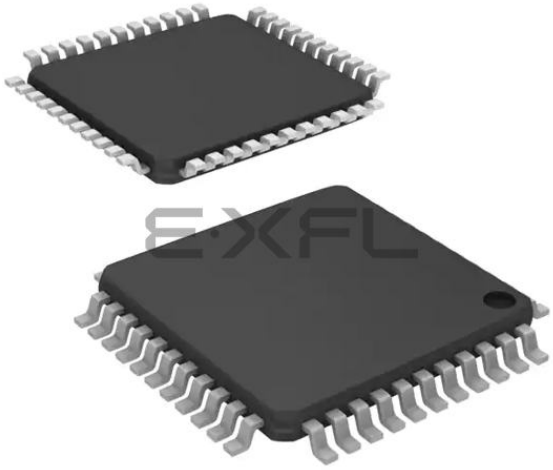

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Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx120f032d-i-pt

1.0 DEVICE OVERVIEW

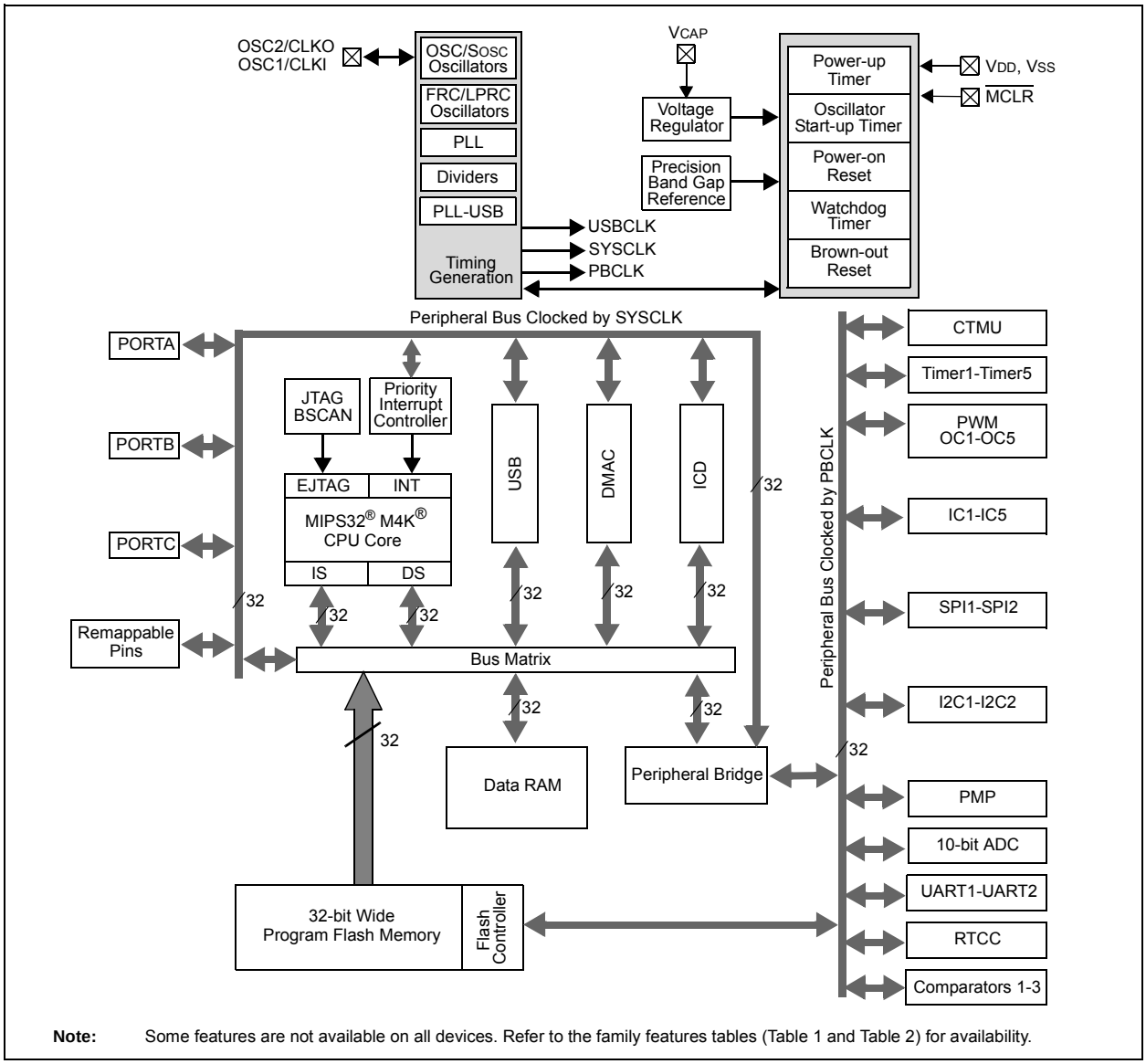
Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: BLOCK DIAGRAM



Note: Some features are not available on all devices. Refer to the family features tables (Table 1 and Table 2) for availability.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
SDA1	15	18	19	1	I/O	ST	Synchronous serial data input/output for I2C1
SCL2	4	7	2	24	I/O	ST	Synchronous serial clock input/output for I2C2
SDA2	3	6	1	23	I/O	ST	Synchronous serial data input/output for I2C2
TMS	19[2] 11[3]	22[2] 14[3]	25[2] 15[3]	12	I	ST	JTAG Test mode select pin
TCK	14	17	18	13	I	ST	JTAG test clock input pin
TDI	13	16	17	35	O	—	JTAG test data input pin
TDO	15	18	19	32	O	—	JTAG test data output pin
RTCC	4	7	2	24	O	ST	Real-Time Clock alarm output
CVREF-	28	3	34	20	I	Analog	Comparator Voltage Reference (low)
CVREF+	27	2	33	19	I	Analog	Comparator Voltage Reference (high)
CVREFOUT	22	25	28	14	O	Analog	Comparator Voltage Reference output
C1INA	4	7	2	24	I	Analog	Comparator Inputs
C1INB	3	6	1	23	I	Analog	
C1INC	2	5	36	22	I	Analog	
C1IND	1	4	35	21	I	Analog	
C2INA	2	5	36	22	I	Analog	
C2INB	1	4	35	21	I	Analog	
C2INC	4	7	2	24	I	Analog	
C2IND	3	6	1	23	I	Analog	
C3INA	23	26	29	15	I	Analog	
C3INB	22	25	28	14	I	Analog	
C3INC	27	2	33	19	I	Analog	
C3IND	1	4	35	21	I	Analog	
C1OUT	PPS	PPS	PPS	PPS	O	—	Comparator Outputs
C2OUT	PPS	PPS	PPS	PPS	O	—	
C3OUT	PPS	PPS	PPS	PPS	O	—	

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
USBID	11[3]	14[3]	15[3]	41[3]	I	ST	USB OTG ID detect
CTED1	27	2	33	19	I	ST	CTMU External Edge Input
CTED2	28	3	34	20	I	ST	
CTED3	13	16	17	43	I	ST	
CTED4	15	18	19	1	I	ST	
CTED5	22	25	28	14	I	ST	
CTED6	23	26	29	15	I	ST	
CTED7	—	—	20	5	I	ST	
CTED8	—	—	—	13	I	ST	
CTED9	9	12	10	34	I	ST	
CTED10	14	17	18	44	I	ST	
CTED11	18	21	24	8	I	ST	
CTED12	2	5	36	22	I	ST	
CTED13	3	6	1	23	I	ST	
CTPLS	21	24	27	11	O	—	CTMU Pulse Output
PGED1	1	4	35	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1
PGEC1	2	5	36	22	I	ST	Clock input pin for Programming/Debugging Communication Channel 1
PGED2	18	21	24	8	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2
PGEC2	19	22	25	9	I	ST	Clock input pin for Programming/Debugging Communication Channel 2
PGED3	11[2]	14[2]	15[2]	41[2]	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3
	27[3]	2[3]	33[3]	19[3]			
PGEC3	12[2]	15[2]	16[2]	42[2]	I	ST	Clock input pin for Programming/ Debugging Communication Channel 3
	28[3]	3[3]	34[3]	20[3]			
PGED4	—	—	3	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4
PGEC4	—	—	4	13	I	ST	Clock input pin for Programming/ Debugging Communication Channel 4

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

Note 1: Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3. "Memory Organization"** (DS60001115), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

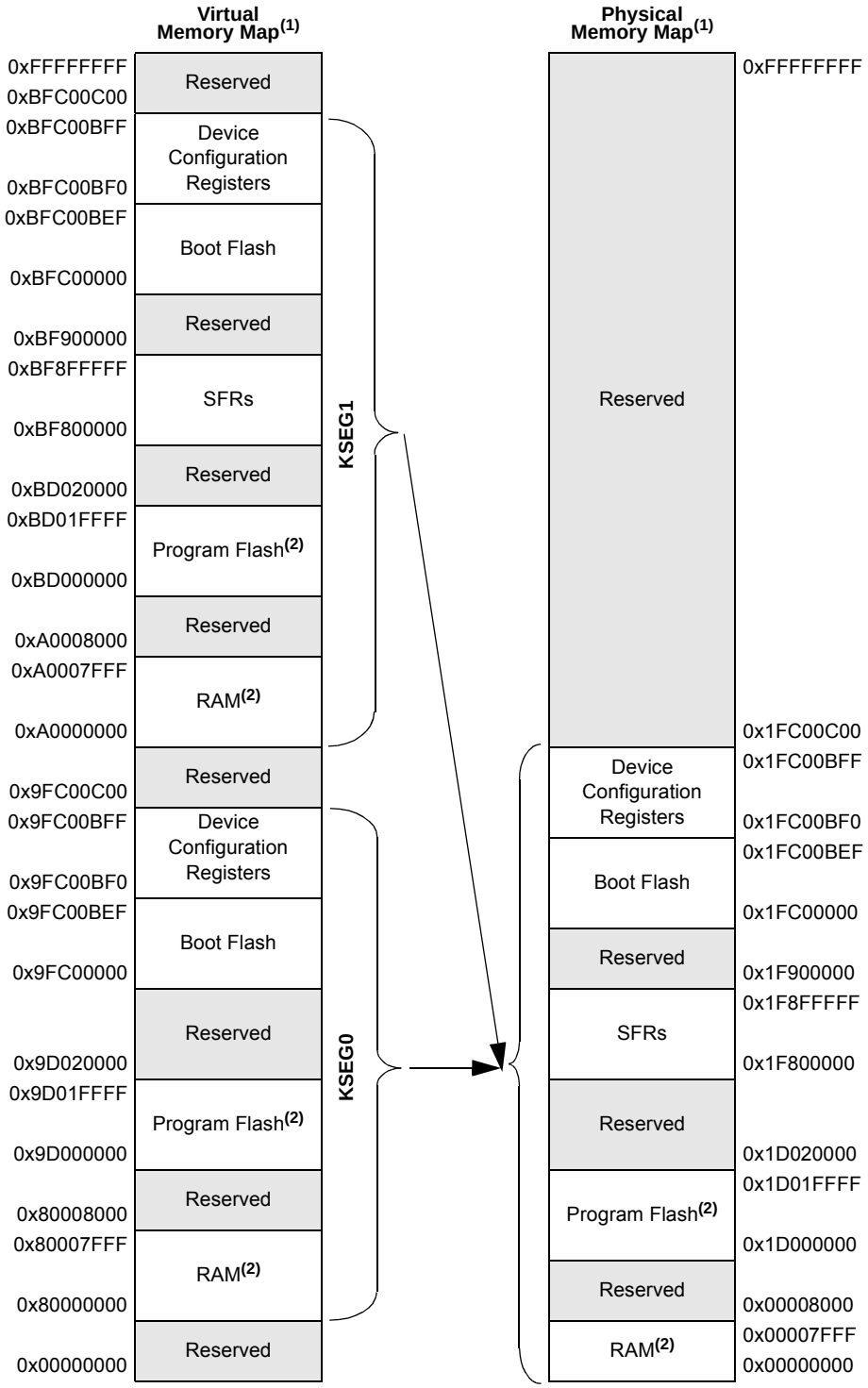
4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX150/250 DEVICES (32 KB RAM, 128 KB FLASH)



Note 1: Memory areas are not shown to scale.

2: The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

REGISTER 6-2: RSWRST: SOFTWARE RESET REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	W-0, HC
	—	—	—	—	—	—	—	SWRST(1)

Legend:	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **SWRST:** Software Reset Trigger bit(1)
- 1 = Enable Software Reset event
- 0 = No effect

Note 1: The system unlock sequence must be performed before the SWRST bit is written. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

TABLE 7-1: INTERRUPT IRQ, VECTOR AND BIT LOCATION (CONTINUED)

Interrupt Source(1)	IRQ #	Vector #	Interrupt Bit Location				Persistent Interrupt
			Flag	Enable	Priority	Sub-priority	
U1E – UART1 Fault	39	32	IFS1<7>	IEC1<7>	IPC8<4:2>	IPC8<1:0>	Yes
U1RX – UART1 Receive Done	40	32	IFS1<8>	IEC1<8>	IPC8<4:2>	IPC8<1:0>	Yes
U1TX – UART1 Transfer Done	41	32	IFS1<9>	IEC1<9>	IPC8<4:2>	IPC8<1:0>	Yes
I2C1B – I2C1 Bus Collision Event	42	33	IFS1<10>	IEC1<10>	IPC8<12:10>	IPC8<9:8>	Yes
I2C1S – I2C1 Slave Event	43	33	IFS1<11>	IEC1<11>	IPC8<12:10>	IPC8<9:8>	Yes
I2C1M – I2C1 Master Event	44	33	IFS1<12>	IEC1<12>	IPC8<12:10>	IPC8<9:8>	Yes
CNA – PORTA Input Change Interrupt	45	34	IFS1<13>	IEC1<13>	IPC8<20:18>	IPC8<17:16>	Yes
CNB – PORTB Input Change Interrupt	46	34	IFS1<14>	IEC1<14>	IPC8<20:18>	IPC8<17:16>	Yes
CNC – PORTC Input Change Interrupt	47	34	IFS1<15>	IEC1<15>	IPC8<20:18>	IPC8<17:16>	Yes
PMP – Parallel Master Port	48	35	IFS1<16>	IEC1<16>	IPC8<28:26>	IPC8<25:24>	Yes
PMPE – Parallel Master Port Error	49	35	IFS1<17>	IEC1<17>	IPC8<28:26>	IPC8<25:24>	Yes
SPI2E – SPI2 Fault	50	36	IFS1<18>	IEC1<18>	IPC9<4:2>	IPC9<1:0>	Yes
SPI2RX – SPI2 Receive Done	51	36	IFS1<19>	IEC1<19>	IPC9<4:2>	IPC9<1:0>	Yes
SPI2TX – SPI2 Transfer Done	52	36	IFS1<20>	IEC1<20>	IPC9<4:2>	IPC9<1:0>	Yes
U2E – UART2 Error	53	37	IFS1<21>	IEC1<21>	IPC9<12:10>	IPC9<9:8>	Yes
U2RX – UART2 Receiver	54	37	IFS1<22>	IEC1<22>	IPC9<12:10>	IPC9<9:8>	Yes
U2TX – UART2 Transmitter	55	37	IFS1<23>	IEC1<23>	IPC9<12:10>	IPC9<9:8>	Yes
I2C2B – I2C2 Bus Collision Event	56	38	IFS1<24>	IEC1<24>	IPC9<20:18>	IPC9<17:16>	Yes
I2C2S – I2C2 Slave Event	57	38	IFS1<25>	IEC1<25>	IPC9<20:18>	IPC9<17:16>	Yes
I2C2M – I2C2 Master Event	58	38	IFS1<26>	IEC1<26>	IPC9<20:18>	IPC9<17:16>	Yes
CTMU – CTMU Event	59	39	IFS1<27>	IEC1<27>	IPC9<28:26>	IPC9<25:24>	Yes
DMA0 – DMA Channel 0	60	40	IFS1<28>	IEC1<28>	IPC10<4:2>	IPC10<1:0>	No
DMA1 – DMA Channel 1	61	41	IFS1<29>	IEC1<29>	IPC10<12:10>	IPC10<9:8>	No
DMA2 – DMA Channel 2	62	42	IFS1<30>	IEC1<30>	IPC10<20:18>	IPC10<17:16>	No
DMA3 – DMA Channel 3	63	43	IFS1<31>	IEC1<31>	IPC10<28:26>	IPC10<25:24>	No
Lowest Natural Order Priority							

Note 1: Not all interrupt sources are available on all devices. See **TABLE 1: "PIC32MX1XX 28/36/44-Pin General Purpose Family Features"** and **TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features"** for the lists of available peripherals.

TABLE 10-1: USB REGISTER MAP (CONTINUED)

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits															All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
5390	U1EP9	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53A0	U1EP10	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53B0	U1EP11	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53C0	U1EP12	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53D0	U1EP13	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53E0	U1EP14	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000
53F0	U1EP15	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: With the exception of those noted, all registers in this table (except as noted) have corresponding CLR, SET and INV registers at their virtual address, plus an offset of 0x4, 0x8, and 0xC respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

2: This register does not have associated SET and INV registers.

3: This register does not have associated CLR, SET and INV registers.

4: Reset value for this bit is undefined.

TABLE 11-1: INPUT PIN SELECTION

Peripheral Pin	[*pin name*]R SFR	[*pin name*]R bits	[*pin name*]R Value to RPn Pin Selection
INT4	INT4R	INT4R<3:0>	0000 = RPA0 0001 = RPB3 0010 = RPB4 0011 = RPB15 0100 = RPB7 0101 = RPC7(2) 0110 = RPC0(1) 0111 = RPC5(2) 1000 = Reserved • • • 1111 = Reserved
T2CK	T2CKR	T2CKR<3:0>	
IC4	IC4R	IC4R<3:0>	
$\overline{SS1}$	SS1R	SS1R<3:0>	
REFCLKI	REFCLKIR	REFCLKIR<3:0>	
INT3	INT3R	INT3R<3:0>	0000 = RPA1 0001 = RPB5 0010 = RPB1 0011 = RPB11 0100 = RPB8 0101 = RPA8(2) 0110 = RPC8(2) 0111 = RPA9(2) 1000 = Reserved • • • 1111 = Reserved
T3CK	T3CKR	T3CKR<3:0>	
IC3	IC3R	IC3R<3:0>	
$\overline{U1CTS}$	U1CTSR	U1CTSR<3:0>	
U2RX	U2RXR	U2RXR<3:0>	
SDI1	SDI1R	SDI1R<3:0>	
INT2	INT2R	INT2R<3:0>	0000 = RPA2 0001 = RPB6 0010 = RPA4 0011 = RPB13 0100 = RPB2 0101 = RPC6(2) 0110 = RPC1(1) 0111 = RPC3(1) 1000 = Reserved • • • 1111 = Reserved
T4CK	T4CKR	T4CKR<3:0>	
IC1	IC1R	IC1R<3:0>	
IC5	IC5R	IC5R<3:0>	
U1RX	U1RXR	U1RXR<3:0>	
$\overline{U2CTS}$	U2CTSR	U2CTSR<3:0>	
SDI2	SDI2R	SDI2R<3:0>	
OCFB	OCFBR	OCFBR<3:0>	
INT1	INT1R	INT1R<3:0>	0000 = RPA3 0001 = RPB14 0010 = RPB0 0011 = RPB10 0100 = RPB9 0101 = RPC9(1) 0110 = RPC2(2) 0111 = RPC4(2) 1000 = Reserved • • • 1111 = Reserved
T5CK	T5CKR	T5CKR<3:0>	
IC2	IC2R	IC2R<3:0>	
$\overline{SS2}$	SS2R	SS2R<3:0>	
OCFA	OCFAR	OCFAR<3:0>	

Note 1: This pin is not available on 28-pin devices.

2: This pin is only available on 44-pin devices.

11.4 Ports Control Registers

TABLE 11-3: PORTA REGISTER MAP

Virtual Address (BF88_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
6000	ANSELA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANSA1	ANSA0	0003
6010	TRISA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	TRISA10(2)	TRISA9(2)	TRISA8(2)	TRISA7(2)	—	—	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	079F
6020	PORTA	31:16	—	—	—	—	—	—	—	—	—	—	—						0000
		15:0	—	—	—	—	—	RA10(2)	RA9(2)	RA8(2)	RA7(2)	—	—	RA4	RA3	RA2	RA1	RA0	xxxx
6030	LATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	LATA10(2)	LATA9(2)	LATA8(2)	LATA7(2)	—	—	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx
6040	ODCA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	ODCA10(2)	ODCA9(2)	ODCA8(2)	ODCA7(2)	—	—	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0	0000
6050	CNPUA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNPUA10(2)	CNPUA9(2)	CNPUA8(2)	CNPUA7(2)	—	—	CNPUA4	CNPUA3	CNPUA2	CNPUA1	CNPUA0	0000
6060	CNPDA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNPDA10(2)	CNPDA9(2)	CNPDA8(2)	CNPDA7(2)	—	—	CNPDA4	CNPDA3	CNPDA2	CNPDA1	CNPDA0	0000
6070	CNCONA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6080	CNENA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNIEA10(2)	CNIEA9(2)	CNIEA8(2)	CNIEA7(2)	—	—	CNIEA4	CNIEA3	CNIEA2	CNIEA1	CNIEA0	0000
6090	CNSTATA	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	CNSTATA10(2)	CNSTATA9(2)	CNSTATA8(2)	CNSTATA7(2)	—	—	CNSTATA4	CNSTATA3	CNSTATA2	CNSTATA1	CNSTATA0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

2: This bit is only available on 44-pin devices.

REGISTER 16-1: OCxCON: OUTPUT COMPARE 'x' CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	ON(1)	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	OC32	OCFLT(2)	OCTSEL	OCM<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Output Compare Peripheral On bit(1)
- 1 = Output Compare peripheral is enabled
- 0 = Output Compare peripheral is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit
- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode

bit 12-6 **Unimplemented:** Read as '0'

bit 5 **OC32:** 32-bit Compare Mode bit
- 1 = OCxR<31:0> and/or OCxRS<31:0> are used for comparisons to the 32-bit timer source
- 0 = OCxR<15:0> and OCxRS<15:0> are used for comparisons to the 16-bit timer source

bit 4 **OCFLT:** PWM Fault Condition Status bit(2)
- 1 = PWM Fault condition has occurred (cleared in hardware only)
- 0 = No PWM Fault condition has occurred

bit 3 **OCTSEL:** Output Compare Timer Select bit
- 1 = Timer3 is the clock source for this Output Compare module
- 0 = Timer2 is the clock source for this Output Compare module

bit 2-0 **OCM<2:0>:** Output Compare Mode Select bits
- 111 = PWM mode on OCx; Fault pin enabled
- 110 = PWM mode on OCx; Fault pin disabled
- 101 = Initialize OCx pin low; generate continuous output pulses on OCx pin
- 100 = Initialize OCx pin low; generate single output pulse on OCx pin
- 011 = Compare event toggles OCx pin
- 010 = Initialize OCx pin high; compare event forces OCx pin low
- 001 = Initialize OCx pin low; compare event forces OCx pin high
- 000 = Output compare peripheral is disabled but continues to draw current

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

2: This bit is only used when OCM<2:0> = '111'. It is read as '0' in all other modes.

REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	AUDEN(1)	—	—	—	AUDMONO(1,2)	—	AUDMOD<1:0>(1,2)	

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **SPISGNEXT:** Sign Extend Read Data from the RX FIFO bit
- 1 = Data from RX FIFO is sign extended
- 0 = Data from RX FIFO is not sign extended

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
- 1 = Frame Error overflow generates error events
- 0 = Frame Error does not generate error events

bit 11 **SPIROVEN:** Enable Interrupt Events via SPIROV bit
- 1 = Receive overflow generates error events
- 0 = Receive overflow does not generate error events

bit 10 **SPITUREN:** Enable Interrupt Events via SPITUR bit
- 1 = Transmit underrun generates error events
- 0 = Transmit underrun does not generate error events

bit 9 **IGNROV:** Ignore Receive Overflow bit (for Audio Data Transmissions)
- 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
- 0 = A ROV is a critical error that stops SPI operation

bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
- 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
- 0 = A TUR is a critical error that stops SPI operation

bit 7 **AUDEN:** Enable Audio CODEC Support bit(1)
- 1 = Audio protocol enabled
- 0 = Audio protocol disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 3 **AUDMONO:** Transmit Audio Data Format bit(1,2)
- 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
- 0 = Audio data is stereo

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **AUDMOD<1:0>:** Audio Protocol Mode bit(1,2)
- 11 = PCM/DSP mode
- 10 = Right-Justified mode
- 01 = Left-Justified mode
- 00 = I^2S mode

Note 1: This bit can only be written when the ON bit = 0.

2: This bit is only valid for AUDEN = 1.

REGISTER 19-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 7-6 **URXISEL<1:0>:** Receive Interrupt Mode Selection bit
11 = Reserved; do not use
10 = Interrupt flag bit is asserted while receive buffer is 3/4 or more full (i.e., has 6 or more data characters)
01 = Interrupt flag bit is asserted while receive buffer is 1/2 or more full (i.e., has 4 or more data characters)
00 = Interrupt flag bit is asserted while receive buffer is not empty (i.e., has at least 1 data character)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled. If 9-bit mode is not selected, this control bit has no effect.
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Data is being received

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit.
This bit is set in hardware and can only be cleared (= 0) in software. Clearing a previously set OERR bit resets the receiver buffer and the RSR to an empty state.
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed

bit 0 **URXDA:** Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

20.1 PMP Control Registers

TABLE 20-1: PARALLEL MASTER PORT REGISTER MAP

Virtual Address (BF80_#)	Register Name(1)	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
7000	PMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN	CSF<1:0>		ALP	—	CS1P	—	WRSP	RDSP	0000
7010	PMMODE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	BUSY	IRQM<1:0>		INCM<1:0>		—	MODE<1:0>		WAITB<1:0>		WAITM<3:0>				WAITE<1:0>		0000
7020	PMADDR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	CS1 / ADDR14	—	—	—	ADDR<10:0>											0000
7030	PMDOUT	31:16	DATAOUT<31:0>																0000
		15:0																	0000
7040	PMDIN	31:16	DATAIN<31:0>																0000
		15:0																	0000
7050	PMAEN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	PTEN14	—	—	—	PTEN<10:0>											0000
7060	PMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 23-2: CMSTAT: COMPARATOR STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
	—	—	SIDL	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
	—	—	—	—	—	C3OUT	C2OUT	C1OUT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Control bit
- 1 = All Comparator modules are disabled when the device enters Idle mode
- 0 = All Comparator modules continue to operate when the device enters Idle mode

bit 12-3 **Unimplemented:** Read as '0'

bit 2 **C3OUT:** Comparator Output bit
- 1 = Output of Comparator 3 is a '1'
- 0 = Output of Comparator 3 is a '0'

bit 1 **C2OUT:** Comparator Output bit
- 1 = Output of Comparator 2 is a '1'
- 0 = Output of Comparator 2 is a '0'

bit 0 **C1OUT:** Comparator Output bit
- 1 = Output of Comparator 1 is a '1'
- 0 = Output of Comparator 1 is a '0'

NOTES:

26.0 POWER-SAVING FEATURES

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 10. "Power-Saving Features"** (DS60001130), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This section describes power-saving features for the PIC32MX1XX/2XX 28/36/44-pin Family. The PIC32 devices offer a total of nine methods and modes, organized into two categories, that allow the user to balance power consumption with device performance. In all of the methods and modes described in this section, power-saving is controlled by software.

26.1 Power Saving with CPU Running

When the CPU is running, power consumption can be controlled by reducing the CPU clock frequency, lowering the PBCLK and by individually disabling modules. These methods are grouped into the following categories:

- FRC Run mode: the CPU is clocked from the FRC clock source with or without postscalers
- LPRC Run mode: the CPU is clocked from the LPRC clock source
- SOSC Run mode: the CPU is clocked from the SOSC clock source

In addition, the Peripheral Bus Scaling mode is available where peripherals are clocked at the programmable fraction of the CPU clock (SYSCLK).

26.2 CPU Halted Methods

The device supports two power-saving modes, Sleep and Idle, both of which Halt the clock to the CPU. These modes operate with all clock sources, as follows:

- POSC Idle mode: the system clock is derived from the POSC. The system clock source continues to operate. Peripherals continue to operate, but can optionally be individually disabled.
- FRC Idle mode: the system clock is derived from the FRC with or without postscalers. Peripherals continue to operate, but can optionally be individually disabled.
- SOSC Idle mode: the system clock is derived from the SOSC. Peripherals continue to operate, but can optionally be individually disabled.
- LPRC Idle mode: the system clock is derived from the LPRC. Peripherals continue to operate, but can optionally be individually disabled. This is the lowest power mode for the device with a clock running.
- Sleep mode: the CPU, the system clock source and any peripherals that operate from the system clock source are Halted. Some peripherals can operate in Sleep using specific clock sources. This is the lowest power mode for the device.

26.3 Power-Saving Operation

Peripherals and the CPU can be Halted or disabled to further reduce power consumption.

26.3.1 SLEEP MODE

Sleep mode has the lowest power consumption of the device power-saving operating modes. The CPU and most peripherals are Halted. Select peripherals can continue to operate in Sleep mode and can be used to wake the device from Sleep. See the individual peripheral module sections for descriptions of behavior in Sleep.

Sleep mode includes the following characteristics:

- The CPU is halted
- The system clock source is typically shutdown. See **Section 26.3.3 "Peripheral Bus Scaling Method"** for specific information.
- There can be a wake-up delay based on the oscillator selection
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode
- The BOR circuit remains operative during Sleep mode
- The WDT, if enabled, is not automatically cleared prior to entering Sleep mode
- Some peripherals can continue to operate at limited functionality in Sleep mode. These peripherals include I/O pins that detect a change in the input signal, WDT, ADC, UART and peripherals that use an external clock input or the internal LPRC oscillator (e.g., RTCC, Timer1 and Input Capture).
- I/O pins continue to sink or source current in the same manner as they do when the device is not in Sleep
- The USB module can override the disabling of the Posc or FRC. Refer to the USB section for specific details.
- Modules can be individually disabled by software prior to entering Sleep in order to further reduce consumption

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

APPENDIX A: REVISION HISTORY

Revision A (May 2011)

This is the initial released version of this document.

Revision B (October 2011)

The following two global changes are included in this revision:

- All packaging references to VLAP have been changed to VTLA throughout the document
- All references to VCORE have been removed
- All occurrences of the ASCL1, ASCL2, ASDA1, and ASDA2 pins have been removed
- V-temp temperature range (-40ºC to +105ºC) was added to all electrical specification tables

This revision includes the addition of the following devices:

- PIC32MX130F064B
- PIC32MX130F064C
- PIC32MX130F064D
- PIC32MX150F128B
- PIC32MX150F128C
- PIC32MX150F128D
- PIC32MX230F064B
- PIC32MX230F064C
- PIC32MX230F064D
- PIC32MX250F128B
- PIC32MX250F128C
- PIC32MX250F128D

Text and formatting changes were incorporated throughout the document.

All other major changes are referenced by their respective section in Table A-1.

TABLE A-1: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**"**	Split the existing Features table into two: PIC32MX1XX General Purpose Family Features (Table 1) and PIC32MX2XX USB Family Features (Table 2). Added the SPDIP package reference (see Table 1, Table 2, and **"Pin Diagrams"**). Added the new devices to the applicable pin diagrams. Changed PGED2 to PGED1 on pin 35 of the 36-pin VTLA diagram for PIC32MX220F032C, PIC32MX220F016C, PIC32MX230F064C, and PIC32MX250F128C devices.
1.0 "Device Overview"	Added the SPDIP package reference and updated the pin number for AN12 for 44-pin QFN devices in the Pinout I/O Descriptions (see Table 1-1). Added the PGEC4/PGED4 pin pair and updated the C1INA-C1IND and C2INA-C2IND pin numbers for 28-pin SSOP/SPDIP/SOIC devices in the Pinout I/O Descriptions (see Table 1-1).
2.0 "Guidelines for Getting Started with 32-bit Microcontrollers"	Updated the Recommended Minimum Connection diagram (see Figure 2-1).

NOTES: