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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f064ct-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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#### TABLE 14: PIN NAMES FOR 44-PIN USB DEVICES

#### 44-PIN VTLA (TOP VIEW)<sup>(1,2,3,5)</sup>

PIC32MX210F016D PIC32MX220F032D PIC32MX230F064D PIC32MX230F256D PIC32MX250F128D PIC32MX270F256D

Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	VDD
7	VCAP	29	Vss
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 <sup>(4)</sup> /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 <sup>(4)</sup> /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVdd	39	Vss
18	MCLR	40	Vdd
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	VBUS
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX210F016D and PIC32MX220F032D devices.

5: Shaded pins are 5V tolerant.

		Pin Nu	mber <sup>(1)</sup>					
Pin Name	28-pin 28-pin QFN SPDIF SOIC		36-pin QFN/ VTLA TQFP/ VTLA		Pin Type	Buffer Type	Description	
USBID	11 <sup>(3)</sup>	14(3)	15 <sup>(3)</sup>	41 <sup>(3)</sup>	I	ST	USB OTG ID detect	
CTED1	27	2	33	19	I	ST	CTMU External Edge Input	
CTED2	28	3	34	20	I	ST		
CTED3	13	16	17	43	I	ST		
CTED4	15	18	19	1	I	ST		
CTED5	22	25	28	14	I	ST		
CTED6	23	26	29	15	I	ST		
CTED7			20	5	I	ST		
CTED8				13	I	ST	7	
CTED9	9	12	10	34	I	ST		
CTED10	14	17	18	44	I	ST		
CTED11	18	21	24	8	I	ST	7	
CTED12	2	5	36	22	I	ST		
CTED13	3	6	1	23	I	ST	7	
CTPLS	21	24	27	11	0	—	CTMU Pulse Output	
PGED1	1	4	35	21	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 1	
PGEC1	2	5	36	22	I	ST	Clock input pin for Programming/Debugging Communication Channel 1	
PGED2	18	21	24	8	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 2	
PGEC2	19	22	25	9	I	ST	Clock input pin for Programming/Debugging Communication Channel 2	
PGED3	11 <sup>(2)</sup> 27 <sup>(3)</sup>	14 <sup>(2)</sup> 2 <sup>(3)</sup>	15 <sup>(2)</sup> 33 <sup>(3)</sup>	41 <sup>(2)</sup> 19 <sup>(3)</sup>	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 3	
PGEC3	12 <sup>(2)</sup> 28 <sup>(3)</sup>	15 <sup>(2)</sup> 3 <sup>(3)</sup>	16 <sup>(2)</sup> 34 <sup>(3)</sup>	42 <sup>(2)</sup> 20 <sup>(3)</sup>	- 1	ST	Clock input pin for Programming/ Debugging Communication Channel 3	
PGED4	—	—	3	12	I/O	ST	Data I/O pin for Programming/Debugging Communication Channel 4	
PGEC4	—	—	4	13	I	ST	Clock input pin for Programming/ Debugging Communication Channel 4	
Legend:	CMOS = CM	MOS compa	atible input	or output	•	Analog =	Analog input P = Power	
:	ST = Schmi	tt Trigger in	put with CN	<b>NOS</b> levels		O = Outp	but I=Input	

# TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

TTL = TTL input buffer PPS = Peripheral Pin Select

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

— = N/A

#### 3.2 Architecture Overview

The MIPS32 M4K processor core contains several logic blocks working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Fixed Mapping Translation (FMT)
- Dual Internal Bus interfaces
- Power Management
- MIPS16e<sup>®</sup> Support
- · Enhanced JTAG (EJTAG) Controller

#### 3.2.1 EXECUTION UNIT

The MIPS32 M4K processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous multiply/divide unit. The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. The register file consists of two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- · 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- · Load aligner
- Bypass multiplexers used to avoid stalls when executing instruction streams where data producing instructions are followed closely by consumers of their results
- Leading Zero/One detect unit for implementing the CLZ and CLO instructions
- Arithmetic Logic Unit (ALU) for performing bitwise logical operations
- Shifter and store aligner

### 3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The MIPS32 M4K processor core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows MDU operations to be partially masked by system stalls and/or other integer unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, result/accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown ('32' of 32x16) represents the *rs* operand. The second number ('16' of 32x16) represents the *rt* operand. The PIC32 core only checks the value of the latter (*rt*) operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU.

Divide operations are implemented with a simple 1 bit per clock iterative algorithm. An early-in detection checks the sign extension of the dividend (*rs*) operand. If *rs* is 8 bits wide, 23 iterations are skipped. For a 16-bit wide *rs*, 15 iterations are skipped and for a 24-bit wide *rs*, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline stall until the divide operation is completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be reissued) and latency (number of cycles until a result is available) for the PIC32 core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

# TABLE 3-1:MIPS32<sup>®</sup> M4K<sup>®</sup> PROCESSOR CORE HIGH-PERFORMANCE INTEGERMULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul rt) (div rs)	Latency	Repeat Rate
MULT/MULTU, MADD/MADDU,	16 bits	1	1
MSUB/MSUBU	32 bits	2	2
MUL	16 bits	2	1
	32 bits	3	2
DIV/DIVU	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

The MIPS architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the General Purpose Register file.

In addition to the HI/LO targeted operations, the MIPS32<sup>®</sup> architecture also defines a multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then

adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

#### 3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. Configuration information, such as presence of options like MIPS16e, is also available by accessing the CP0 registers, listed in Table 3-2.

Register Number	Register Name	Function
0-6	Reserved	Reserved in the PIC32MX1XX/2XX family core.
7	HWREna	Enables access via the RDHWR instruction to selected hardware registers.
8	BadVAddr <sup>(1)</sup>	Reports the address for the most recent address-related exception.
9	Count <sup>(1)</sup>	Processor cycle count.
10	Reserved	Reserved in the PIC32MX1XX/2XX family core.
11	Compare <sup>(1)</sup>	Timer interrupt control.
12	Status <sup>(1)</sup>	Processor status and control.
12	IntCtl <sup>(1)</sup>	Interrupt system status and control.
12	SRSCtl <sup>(1)</sup>	Shadow register set status and control.
12	SRSMap <sup>(1)</sup>	Provides mapping from vectored interrupt to a shadow set.
13	Cause <sup>(1)</sup>	Cause of last general exception.
14	EPC <sup>(1)</sup>	Program counter at last exception.
15	PRId	Processor identification and revision.
15	EBASE	Exception vector base register.
16	Config	Configuration register.
16	Config1	Configuration Register 1.
16	Config2	Configuration Register 2.
16	Config3	Configuration Register 3.
17-22	Reserved	Reserved in the PIC32MX1XX/2XX family core.
23	Debug <sup>(2)</sup>	Debug control and exception status.
24	DEPC <sup>(2)</sup>	Program counter at last debug exception.
25-29	Reserved	Reserved in the PIC32MX1XX/2XX family core.
30	ErrorEPC <sup>(1)</sup>	Program counter at last error.
31	DESAVE <sup>(2)</sup>	Debug handler scratchpad register.

#### TABLE 3-2: COPROCESSOR 0 REGISTERS

**Note 1:** Registers used in exception processing.

**2:** Registers used during debug.

Coprocessor 0 also contains the logic for identifying and managing exceptions. Exceptions can be caused by a variety of sources, including alignment errors in data, external events or program errors. Table 3-3 lists the exception types in order of priority.

Exception	Description
Reset	Assertion MCLR or a Power-on Reset (POR).
DSS	EJTAG debug single step.
DINT	EJTAG debug interrupt. Caused by the assertion of the external <i>EJ_DINT</i> input or by setting the EjtagBrk bit in the ECR register.
NMI	Assertion of NMI signal.
Interrupt	Assertion of unmasked hardware or software interrupt signal.
DIB	EJTAG debug hardware instruction break matched.
AdEL	Fetch address alignment error. Fetch reference to protected address.
IBE	Instruction fetch bus error.
DBp	EJTAG breakpoint (execution of SDBBP instruction).
Sys	Execution of SYSCALL instruction.
Вр	Execution of BREAK instruction.
RI	Execution of a reserved instruction.
CpU	Execution of a coprocessor instruction for a coprocessor that is not enabled.
CEU	Execution of a CorExtend instruction when CorExtend is not enabled.
Ov	Execution of an arithmetic instruction that overflowed.
Tr	Execution of a trap (when trap condition is true).
DDBL/DDBS	EJTAG Data Address Break (address only) or EJTAG data value break on store (address + value).
AdEL	Load address alignment error. Load reference to protected address.
AdES	Store address alignment error. Store to protected address.
DBE	Load or store bus error.
DDBL	EJTAG data hardware breakpoint matched in load data compare.

# TABLE 3-3: MIPS32<sup>®</sup> M4K<sup>®</sup> PROCESSOR CORE EXCEPTION TYPES

## 3.3 Power Management

The MIPS M4K processor core offers many power management features, including low-power design, active power management and power-down modes of operation. The core is a static design that supports slowing or Halting the clocks, which reduces system power consumption during Idle periods.

#### 3.3.1 INSTRUCTION-CONTROLLED POWER MANAGEMENT

The mechanism for invoking Power-Down mode is through execution of the WAIT instruction. For more information on power management, see Section 26.0 "Power-Saving Features".

# 3.4 EJTAG Debug Support

The MIPS M4K processor core provides an Enhanced JTAG (EJTAG) interface for use in the software debug of application and kernel code. In addition to standard User mode and Kernel modes of operation, the M4K core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification define which registers are selected and how they are used.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
31.24		NVMKEY<31:24>									
00.40	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
23:10	NVMKEY<23:16>										
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
15:8	NVMKEY<15:8>										
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0			
7:0				NVMK	EY<7:0>						

#### REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

# Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

#### REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24	NVMADDR<31:24>									
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMADDR<23:16>									
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
10.0	NVMADDR<15:8>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0				NVMA	DR<7:0>					

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 NVMADDR<31:0>: Flash Address bits

Bulk/Chip/PFM Erase: Address is ignored. Page Erase: Address identifies the page to erase. Row Program: Address identifies the row to program. Word Program: Address identifies the word to program.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31:24	—	—	_	—	—	—	—	—			
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	—	—			
15:0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0			
10.0	—	—	—	—	—	5	6RIPL<2:0> <sup>(1)</sup>				
7:0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7:0	—	—		VEC<5:0> <sup>(1)</sup>							

#### REGISTER 7-2: INTSTAT: INTERRUPT STATUS REGISTER

#### Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-11 Unimplemented: Read as '0'

- bit 10-8 SRIPL<2:0>: Requested Priority Level bits<sup>(1)</sup>
  - 111-000 = The priority level of the latest interrupt presented to the CPU
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 VEC<5:0>: Interrupt Vector bits<sup>(1)</sup> 11111-00000 = The interrupt vector that is presented to the CPU
- Note 1: This value should only be used when the interrupt controller is configured for Single Vector mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24		IPTMR<31:24>								
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23.10	IPTMR<23:16>									
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	IPTMR<15:8>									
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
				IPTM	IR<7:0>					

#### REGISTER 7-3: IPTMR: INTERRUPT PROXIMITY TIMER REGISTER

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 **IPTMR<31:0>:** Interrupt Proximity Timer Reload bits Used by the Interrupt Proximity Timer as a reload value when the Interrupt Proximity timer is triggered by an interrupt event.

# 8.0 OSCILLATOR CONFIGURATION

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 6. "Oscillator
	Configuration" (DS60001112), which is
	available from the Documentation >
	Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

The PIC32MX1XX/2XX 28/36/44-pin Family oscillator system has the following modules and features:

- Four external and internal oscillator options as clock sources
- On-Chip PLL with user-selectable input divider, multiplier and output divider to boost operating frequency on select internal and external oscillator sources
- On-Chip user-selectable divisor postscaler on select oscillator sources
- Software-controllable switching between various clock sources
- A Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Dedicated On-Chip PLL for USB peripheral

A block diagram of the oscillator system is provided in Figure 8-1.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	_	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	_	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
15:8	CHBUSY	—	—	—	—	_	_	CHCHNS <sup>(1)</sup>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN <sup>(2)</sup>	CHAED	CHCHN	CHAEN	—	CHEDET	CHPF	RI<1:0>

#### REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, r	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 CHBUSY: Channel Busy bit
  - 1 = Channel is active or has been enabled
  - 0 = Channel is inactive or has been disabled
- bit 14-9 Unimplemented: Read as '0'
- bit 8 CHCHNS: Chain Channel Selection bit<sup>(1)</sup>
  - 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
  - 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

#### bit 7 CHEN: Channel Enable bit<sup>(2)</sup>

- 1 = Channel is enabled
- 0 = Channel is disabled

#### bit 6 CHAED: Channel Allow Events If Disabled bit

- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

#### bit CHCHN: Channel Chain Enable bit

- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained
- bit 4 CHAEN: Channel Automatic Enable bit
  - 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
    0 = Channel is disabled on block transfer complete

#### bit 3 Unimplemented: Read as '0'

- bit 2 CHEDET: Channel Event Detected bit
  - 1 = An event has been detected
  - 0 = No events have been detected
- bit 1-0 CHPRI<1:0>: Channel Priority bits
  - 11 = Channel has priority 3 (highest)
  - 10 = Channel has priority 2
  - 01 = Channel has priority 1
  - 00 = Channel has priority 0
- Note 1: The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).
  - 2: When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	_	_	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE	_	VBUSVDIE

#### REGISTER 10-2: U1OTGIE: USB OTG INTERRUPT ENABLE REGISTER

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-8 Unimplemented: Read as '0'

- bit 7 **IDIE:** ID Interrupt Enable bit
  - 1 = ID interrupt is enabled
  - 0 = ID interrupt is disabled

#### bit 6 T1MSECIE: 1 Millisecond Timer Interrupt Enable bit

- 1 = 1 millisecond timer interrupt is enabled
- 0 = 1 millisecond timer interrupt is disabled

#### bit 5 LSTATEIE: Line State Interrupt Enable bit

- 1 = Line state interrupt is enabled
- 0 = Line state interrupt is disabled
- bit 4 ACTVIE: Bus Activity Interrupt Enable bit
  - 1 = Activity interrupt is enabled
  - 0 = Activity interrupt is disabled
- bit 3 SESVDIE: Session Valid Interrupt Enable bit
  - 1 = Session valid interrupt is enabled
  - 0 = Session valid interrupt is disabled
- bit 2 SESENDIE: B-Device Session End Interrupt Enable bit
  - 1 = B-Device session end interrupt is enabled
  - 0 = B-Device session end interrupt is disabled
- bit 1 Unimplemented: Read as '0'
- bit 0 VBUSVDIE: A-Device VBUS Valid Interrupt Enable bit
  - 1 = A-Device VBUS valid interrupt is enabled
  - 0 = A-Device VBUS valid interrupt is disabled

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0						
31.24	—	—	—	—	—	—	—	—
23:16	U-0	U-0						
	—	—	—	—	—	—	—	—
15.0	U-0	U-0						
15.0	—	—	—	—	—	—	—	—
7:0	R/WC-0, HS	R/WC-0, HS						
	BTSEF	EF BMXEF DMA				CRC16EF	CRC5EF <sup>(4)</sup>	PIDEF
					DINOLI		EOFEF <sup>(3,5)</sup>	

#### REGISTER 10-8: U1EIR: USB ERROR INTERRUPT STATUS REGISTER

Legend:	WC = Write '1' to clear HS = Hardware Settable bit		oit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31-8 Unimplemented: Read as '0'
- bit 7 BTSEF: Bit Stuff Error Flag bit
  - 1 = Packet rejected due to bit stuff error
  - 0 = Packet accepted
- bit 6 BMXEF: Bus Matrix Error Flag bit
  - 1 = The base address, of the Buffer Descriptor Table, or the address of an individual buffer pointed to by a Buffer Descriptor Table entry, is invalid.
  - 0 = No address error
- bit 5 DMAEF: DMA Error Flag bit<sup>(1)</sup>
  - 1 = USB DMA error condition detected
  - 0 = No DMA error
- bit 4 BTOEF: Bus Turnaround Time-Out Error Flag bit<sup>(2)</sup>
  - 1 = Bus turnaround time-out has occurred
  - 0 = No bus turnaround time-out
- bit 3 **DFN8EF:** Data Field Size Error Flag bit
  - 1 = Data field received is not an integral number of bytes
  - 0 = Data field received is an integral number of bytes
- bit 2 CRC16EF: CRC16 Failure Flag bit
  - 1 = Data packet rejected due to CRC16 error
  - 0 = Data packet accepted
- **Note 1:** This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
  - **2:** This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
  - **3:** This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.
  - 4: Device mode.
  - 5: Host mode.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—			—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	_	—	_	_	_			_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—			—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
						FRMH<2:0>		

#### REGISTER 10-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Legend	:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits The register bits are updated with the current frame number whenever a SOF TOKEN is received.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
31.24	—	—	—	—	—	—		—			
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
23.10	—	—	—	—	—	—	-	—			
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0			
15.0	—	—	—	—	—	—		—			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
7.0		PID<	3:0>(1)			EP<	3:0>				

#### REGISTER 10-15: U1TOK: USB TOKEN REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits<sup>(1)</sup>

1101 = SETUP (TX) token type transaction

- 1001 = IN (RX) token type transaction
- 0001 = OUT (TX) token type transaction

Note: All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits The four bit value must specify a valid endpoint.

Note 1: All other values are reserved and must not be used.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
1.0				CNT	<7:0>			

#### REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-8 Unimplemented: Read as '0'

- bit 7-0 CNT<7:0>: SOF Threshold Value bits Typical values of the threshold are:

  - 01001010 = 64-byte packet 00101010 = **32-byte packet**
  - 00011010 = **16-byte packet**
  - 00010010 = 8-byte packet

#### REGISTER 10-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	-	-	-	-	_
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—					_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—				-	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
7.0			B	DTPTRL<15:9	)>			_

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-8 Unimplemented: Read as '0'

bit 7-1 BDTPTRL<15:9>: Buffer Descriptor Table Base Address bits This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 Unimplemented: Read as '0'

#### 22.0 **10-BIT ANALOG-TO-DIGITAL** CONVERTER (ADC)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- · Up to 1 Msps conversion speed

**FIGURE 22-1:** 

- Up to 13 analog input pins
- External voltage reference input pins
- · One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- · 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- · Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.



#### 5: This selection is only used with CTMU capacitive and time measurement.

ADC1 MODULE BLOCK DIAGRAM

NOTES:

						0					
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.04	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1			
31:24	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—		—	_			
22.16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1			
23.10	—	—	—	—	—	—	—	-			
15.0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P			
15.0	USERID<15:8>										
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P			
7.0				USERID<	7:0>						

#### REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3

Legend:	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 FVBUSONIO: USB VBUSON Selection bit

- 1 = VBUSON pin is controlled by the USB module 0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit 1 = USBID pin is controlled by the USB module 0 = USBID pin is controlled by the port function
- bit 29 IOL1WAY: Peripheral Pin Select Configuration bit
  - 1 = Allow only one reconfiguration
  - 0 = Allow multiple reconfigurations
- bit 28 PMDI1WAY: Peripheral Module Disable Configuration bit
  - 1 = Allow only one reconfiguration
  - 0 = Allow multiple reconfigurations
- bit 27-16 Reserved: Write '1'
- bit 15-0 USERID<15:0>: User ID bits

This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

NOTES:

# **30.0 ELECTRICAL CHARACTERISTICS**

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices that operate at 40 MHz. Refer to **Section 31.0** "**50 MHz Electrical Characteristics**" for additional specifications for operations at higher frequency. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

## **Absolute Maximum Ratings**

#### (See Note 1)

Ambient temperature under bias	40°C to +105°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when VDD $\ge$ 2.3V (Note 3)	0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	0.3V to +5.5V
Maximum current out of Vss pin(s)	
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports (Note 2)	200 mA

**Note 1:** Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the "Pin Diagrams" section for the 5V tolerant pins.

#### TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard (unless of Operating	<b>Operati</b> herwise tempera	n <b>g Condition e stated)</b> ture -40°C -40°C	ns: 2.3V ≤ Ta ≤ + ≤ Ta ≤ +	′ <b>to 3.6V</b> -85°C fo -105°C f	r Industrial or V-temp
Param. No.	Symbol	Characteristi	Min.	Typical	Max.	Units	Conditions	
OS50	Fplli	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range		3.92	_	5	MHz	ECPLL, HSPLL, XTPLL, FRCPLL modes
OS51	Fsys	On-Chip VCO System Frequency		60	_	120	MHz	_
OS52	TLOCK	PLL Start-up Time (Lock Time)		_	—	2	ms	—
OS53	DCLK	CLKO Stability <sup>(2)</sup> (Period Jitter or Cumulative)		-0.25		+0.25	%	Measured over 100 ms period

Note 1: These parameters are characterized, but not tested in manufacturing.

2: This jitter specification is based on clock-cycle by clock-cycle measurements. To get the effective jitter for individual time-bases on communication clocks, use the following formula:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{SYSCLK}{CommunicationClock}}}$$

For example, if SYSCLK = 40 MHz and SPI bit rate = 20 MHz, the effective jitter is as follows:

$$EffectiveJitter = \frac{D_{CLK}}{\sqrt{\frac{40}{20}}} = \frac{D_{CLK}}{1.41}$$

#### TABLE 30-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		<b>Standar</b> (unless Operatir	Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp						
Param. No.	Characteristics	Min. Typical Max. Units Conditions				Conditions			
Internal FRC Accuracy @ 8.00 MHz <sup>(1)</sup>									
F20b	FRC	-0.9 — +0.9 % —							

Note 1: Frequency calibrated at 25°C and 3.3V. The TUN bits can be used to compensate for temperature drift.

#### TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standar (unless Operatir	$\begin{array}{ll} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$							
Param. No.	Characteristics	Min.	Typical	Max.	Units	Conditions				
	LPRC @ 31.25 kHz <sup>(1)</sup>									
F21	LPRC	-15 — +15 % —								

**Note 1:** Change of LPRC frequency as VDD changes.

# 31.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 30.0** "Electrical Characteristics", with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter "M", which denotes 50 MHz operation. For example, parameter DC29a in **Section 30.0** "**Electrical Characteristics**", is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

## Absolute Maximum Ratings

#### (See Note 1)

Ambient temperature under bias	40°C to +85°C
Storage temperature	65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to Vss (Note 3)	0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to Vss when $VDD \ge 2.3V$ (Note 3)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 2.3V (Note 3)	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3	0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS	-0.3V to +5.5V
Maximum current out of Vss pin(s)	
Maximum current into VDD pin(s) (Note 2)	
Maximum output current sunk by any I/O pin	15 mA
Maximum output current sourced by any I/O pin	15 mA
Maximum current sunk by all ports	
Maximum current sourced by all ports (Note 2)	200 mA

**Note 1:** Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).
- 3: See the "Pin Diagrams" section for the 5V tolerant pins.