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Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f064ct-v-tl

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1: PIC32MX1XX 28/36/44-PIN GENERAL PURPOSE FAMILY FEATURES

Device	Pins	Program Memory (KB) ⁽¹⁾	Data Memory (KB)	Remappable Peripherals					Analog Comparators	USB On-The-Go (OTG)	I ² C	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	Packages
				Remappable Pins	Timers ⁽²⁾ /Capture/Compare	UART	SPI/I ² S	External Interrupts ⁽³⁾											
PIC32MX110F016B	28	16+3	4	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX110F016C	36	16+3	4	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX110F016D	44	16+3	4	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX120F032B	28	32+3	8	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX120F032C	36	32+3	8	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX120F032D	44	32+3	8	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX130F064B	28	64+3	16	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX130F064C	36	64+3	16	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX130F064D	44	64+3	16	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX150F128B	28	128+3	32	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX150F128C	36	128+3	32	24	5/5/5	2	2	5	3	N	2	Y	4/0	Y	12	Y	25	Y	VTLA
PIC32MX150F128D	44	128+3	32	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX130F256B	28	256+3	16	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX130F256D	44	256+3	16	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN
PIC32MX170F256B	28	256+3	64	20	5/5/5	2	2	5	3	N	2	Y	4/0	Y	10	Y	21	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX170F256D	44	256+3	64	32	5/5/5	2	2	5	3	N	2	Y	4/0	Y	13	Y	35	Y	VTLA, TQFP, QFN

- Note 1:** This device features 3 KB of boot Flash memory.
2: Four out of five timers are remappable.
3: Four out of five external interrupts are remappable.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 10: PIN NAMES FOR 44-PIN USB DEVICES

44-PIN QFN (TOP VIEW) ^(1,2,3,5)			
PIC32MX210F016D PIC32MX220F032D PIC32MX230F064D PIC32MX230F256D PIC32MX250F128D PIC32MX270F256D			
		44	1
Pin #	Full Pin Name	Pin #	Full Pin Name
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	VSS	28	VDD
7	VCAP	29	VSS
8	PGED2/RPB10/D+/CTED11/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/D-/RB11	31	OSC2/CLKO/RPA3/RA3
10	VUSB3V3	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4/TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4/TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/VBUSEN/SCK1/CTED5/RB14	36	AN12/RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVSS	38	RPC5/PMA3/RC5
17	AVDD	39	VSS
18	MCLR	40	VDD
19	PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	41	RPB5/USBID/RB5
20	PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	42	VBUS
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
 - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
 - 4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.
 - 5: Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Table of Contents

1.0	Device Overview	19
2.0	Guidelines for Getting Started with 32-bit MCUs.....	27
3.0	CPU	33
4.0	Memory Organization	37
5.0	Flash Program Memory	53
6.0	Resets	59
7.0	Interrupt Controller	63
8.0	Oscillator Configuration	73
9.0	Direct Memory Access (DMA) Controller	83
10.0	USB On-The-Go (OTG).....	103
11.0	I/O Ports	127
12.0	Timer1	143
13.0	Timer2/3, Timer4/5	147
14.0	Watchdog Timer (WDT)	153
15.0	Input Capture	157
16.0	Output Compare	161
17.0	Serial Peripheral Interface (SPI).....	165
18.0	Inter-Integrated Circuit (I ² C).....	173
19.0	Universal Asynchronous Receiver Transmitter (UART)	181
20.0	Parallel Master Port (PMP).....	189
21.0	Real-Time Clock and Calendar (RTCC).....	199
22.0	10-bit Analog-to-Digital Converter (ADC)	209
23.0	Comparator	219
24.0	Comparator Voltage Reference (CVREF).....	223
25.0	Charge Time Measurement Unit (CTMU)	227
26.0	Power-Saving Features	233
27.0	Special Features	239
28.0	Instruction Set	251
29.0	Development Support.....	253
30.0	Electrical Characteristics	257
31.0	50 MHz Electrical Characteristics.....	301
32.0	DC and AC Device Characteristics Graphs.....	307
33.0	Packaging Information.....	311
	The Microchip Web Site	341
	Customer Change Notification Service	341
	Customer Support	341
	Product Identification System.....	342

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

Referenced Sources

This device data sheet is based on the following individual chapters of the “PIC32 Family Reference Manual”. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the following documents, refer to the <i>Documentation > Reference Manuals</i> section of the Microchip PIC32 website: http://www.microchip.com/pic32

- **Section 1. “Introduction”** (DS60001127)
- **Section 2. “CPU”** (DS60001113)
- **Section 3. “Memory Organization”** (DS60001115)
- **Section 5. “Flash Program Memory”** (DS60001121)
- **Section 6. “Oscillator Configuration”** (DS60001112)
- **Section 7. “Resets”** (DS60001118)
- **Section 8. “Interrupt Controller”** (DS60001108)
- **Section 9. “Watchdog Timer and Power-up Timer”** (DS60001114)
- **Section 10. “Power-Saving Features”** (DS60001130)
- **Section 12. “I/O Ports”** (DS60001120)
- **Section 13. “Parallel Master Port (PMP)”** (DS60001128)
- **Section 14. “Timers”** (DS60001105)
- **Section 15. “Input Capture”** (DS60001122)
- **Section 16. “Output Compare”** (DS60001111)
- **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104)
- **Section 19. “Comparator”** (DS60001110)
- **Section 20. “Comparator Voltage Reference (CVREF)”** (DS60001109)
- **Section 21. “Universal Asynchronous Receiver Transmitter (UART)”** (DS60001107)
- **Section 23. “Serial Peripheral Interface (SPI)”** (DS60001106)
- **Section 24. “Inter-Integrated Circuit (I²C)”** (DS60001116)
- **Section 27. “USB On-The-Go (OTG)”** (DS60001126)
- **Section 29. “Real-Time Clock and Calendar (RTCC)”** (DS60001125)
- **Section 31. “Direct Memory Access (DMA) Controller”** (DS60001117)
- **Section 32. “Configuration”** (DS60001124)
- **Section 33. “Programming and Diagnostics”** (DS60001129)
- **Section 37. “Charge Time Measurement Unit (CTMU)”** (DS60001167)

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

2.8.1 CRYSTAL OSCILLATOR DESIGN CONSIDERATION

The following example assumptions are used to calculate the Primary Oscillator loading capacitor values:

- C_{IN} = PIC32_OSC2_Pin Capacitance = ~4-5 pF
- C_{OUT} = PIC32_OSC1_Pin Capacitance = ~4-5 pF
- C1 and C2 = XTAL manufacturing recommended loading capacitance
- Estimated PCB stray capacitance, (i.e., 12 mm length) = 2.5 pF

EXAMPLE 2-1: CRYSTAL LOAD CAPACITOR CALCULATION

Crystal manufacturer recommended: $C1 = C2 = 15 \text{ pF}$

Therefore:

$$\begin{aligned} C_{LOAD} &= \{ ([C_{IN} + C1] * [C_{OUT} + C2]) / [C_{IN} + C1 + C2 + C_{OUT}] \} \\ &\quad + \text{estimated oscillator PCB stray capacitance} \\ &= \{ ([5 + 15][5 + 15]) / [5 + 15 + 15 + 5] \} + 2.5 \text{ pF} \\ &= \{ ([20][20]) / [40] \} + 2.5 \\ &= 10 + 2.5 = 12.5 \text{ pF} \end{aligned}$$

Rounded to the nearest standard value or 12 pF in this example for Primary Oscillator crystals "C1" and "C2".

The following tips are used to increase oscillator gain, (i.e., to increase peak-to-peak oscillator signal):

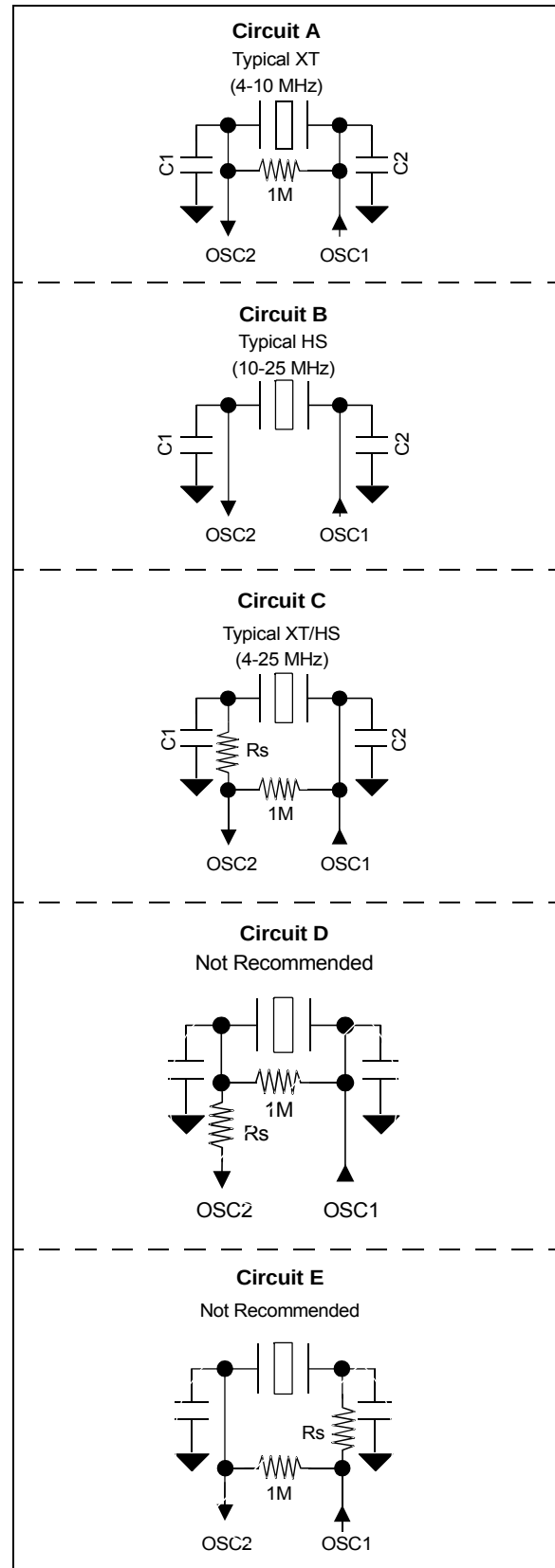
- Select a crystal with a lower "minimum" power drive rating
- Select an crystal oscillator with a lower XTAL manufacturing "ESR" rating.
- Add a parallel resistor across the crystal. The smaller the resistor value the greater the gain. It is recommended to stay in the range of 600k to 1M
- C1 and C2 values also affect the gain of the oscillator. The lower the values, the higher the gain.
- C2/C1 ratio also affects gain. To increase the gain, make C1 slightly smaller than C2, which will also help start-up performance.

Note: Do not add excessive gain such that the oscillator signal is clipped, flat on top of the sine wave. If so, you need to reduce the gain or add a series resistor, R_S , as shown in circuit "C" in Figure 2-4. Failure to do so will stress and age the crystal, which can result in an early failure. Adjust the gain to trim the max peak-to-peak to $\sim V_{DD} - 0.6V$. When measuring the oscillator signal you must use a FET scope probe or a probe with $\leq 1.5 \text{ pF}$ or the scope probe itself will unduly change the gain and peak-to-peak levels.

2.8.1.1 Additional Microchip References

- AN588 "PICmicro® Microcontroller Oscillator Design Guide"
- AN826 "Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices"
- AN849 "Basic PICmicro® Oscillator Design"

FIGURE 2-4: PRIMARY CRYSTAL OSCILLATOR CIRCUIT RECOMMENDATIONS



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

2.9 Typical Application Connection Examples

Examples of typical application connections are shown in Figure 2-5 and Figure 2-6.

FIGURE 2-5: CAPACITIVE TOUCH SENSING WITH GRAPHICS APPLICATION

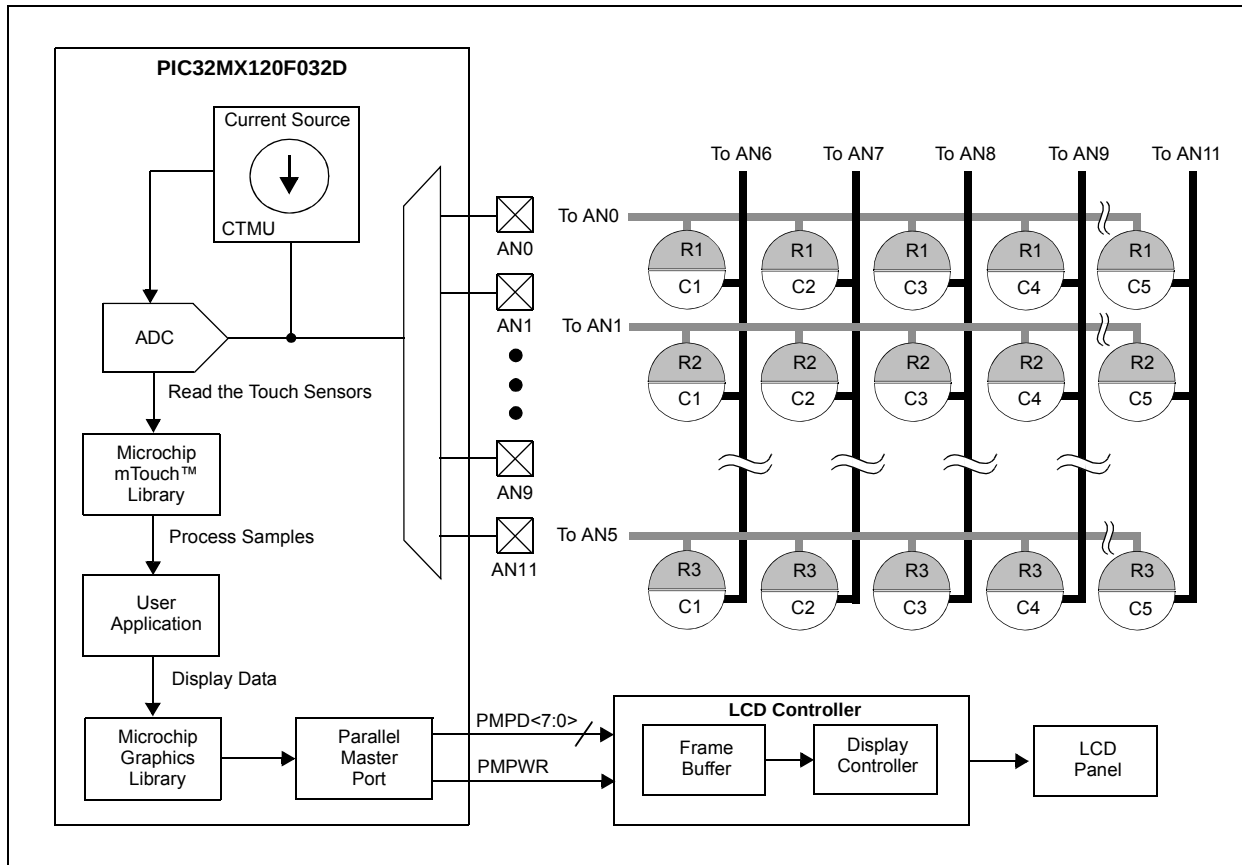
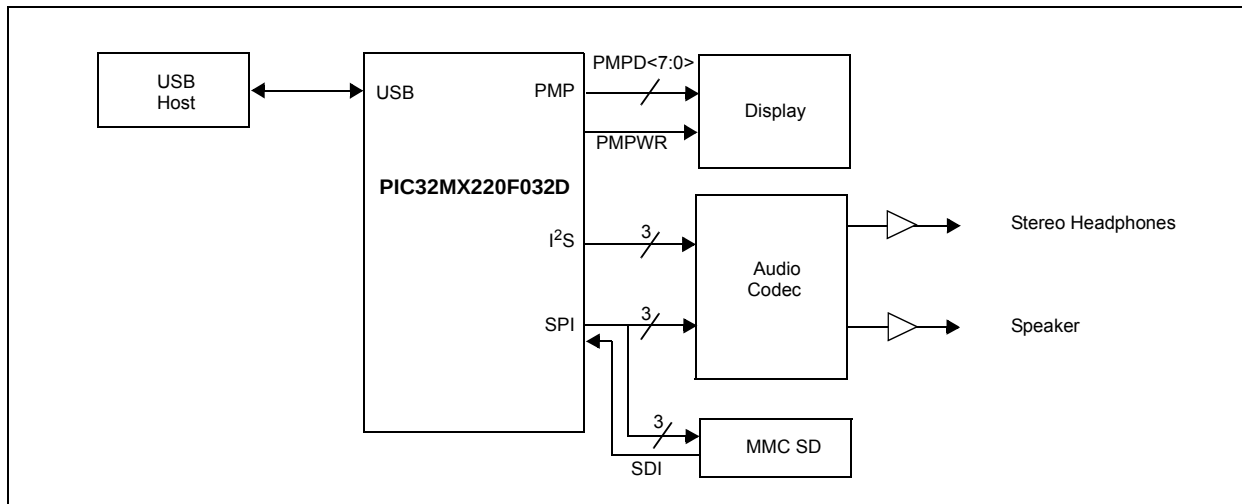


FIGURE 2-6: AUDIO PLAYBACK APPLICATION



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1
	—	—	PLLODIV<2:0>			FRCDIV<2:0>		
23:16	U-0	R-0	R-1	R/W-y	R/W-y	R/W-y	R/W-y	R/W-y
	—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>		
15:8	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
	—	COSC<2:0>			—	NOSC<2:0>		
7:0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0
	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRocen ⁽¹⁾	SOSCEN	OSWEN

Legend: y = Value set from Configuration bits on POR
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

111 = PLL output divided by 256
110 = PLL output divided by 64
101 = PLL output divided by 32
100 = PLL output divided by 16
011 = PLL output divided by 8
010 = PLL output divided by 4
001 = PLL output divided by 2
000 = PLL output divided by 1

bit 26-24 **FRCDIV<2:0>:** Internal Fast RC (FRC) Oscillator Clock Divider bits

111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2 (default setting)
000 = FRC divided by 1

bit 23 **Unimplemented:** Read as '0'

bit 22 **SOSCRDY:** Secondary Oscillator (Sosc) Ready Indicator bit

1 = The Secondary Oscillator is running and is stable
0 = The Secondary Oscillator is still warming up or is turned off

bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit

1 = PBDIV<1:0> bits can be written
0 = PBDIV<1:0> bits cannot be written

bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits

11 = PBCLK is SYSCLK divided by 8 (default)
10 = PBCLK is SYSCLK divided by 4
01 = PBCLK is SYSCLK divided by 2
00 = PBCLK is SYSCLK divided by 1

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the "PIC32 Family Reference Manual" for details.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 9-12: DCHxSSIZ: DMA CHANNEL 'x' SOURCE SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHSSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHSSIZ<15:0>:** Channel Source Size bits

1111111111111111 = 65,535 byte source size

.

.

.

0000000000000010 = 2 byte source size

0000000000000001 = 1 byte source size

0000000000000000 = 65,536 byte source size

REGISTER 9-13: DCHxDSIZ: DMA CHANNEL 'x' DESTINATION SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CHDSIZ<7:0>							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-0 **CHDSIZ<15:0>:** Channel Destination Size bits

1111111111111111 = 65,535 byte destination size

.

.

.

0000000000000010 = 2 byte destination size

0000000000000001 = 1 byte destination size

0000000000000000 = 65,536 byte destination size

TABLE 11-6: PERIPHERAL PIN SELECT INPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FA54	U1CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U1CTSR<3:0>				0000
FA58	U2RXR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2RXR<3:0>				0000
FA5C	U2CTSR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	U2CTSR<3:0>				0000
FA84	SDI1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI1R<3:0>				0000
FA88	SS1R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS1R<3:0>				0000
FA90	SDI2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SDI2R<3:0>				0000
FA94	SS2R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	SS2R<3:0>				0000
FAB8	REFCLKIR	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	REFCLKIR<3:0>				0000

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB8C	RPC8R ⁽¹⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC8<3:0>				0000
FB90	RPC9R ⁽³⁾	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC9<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

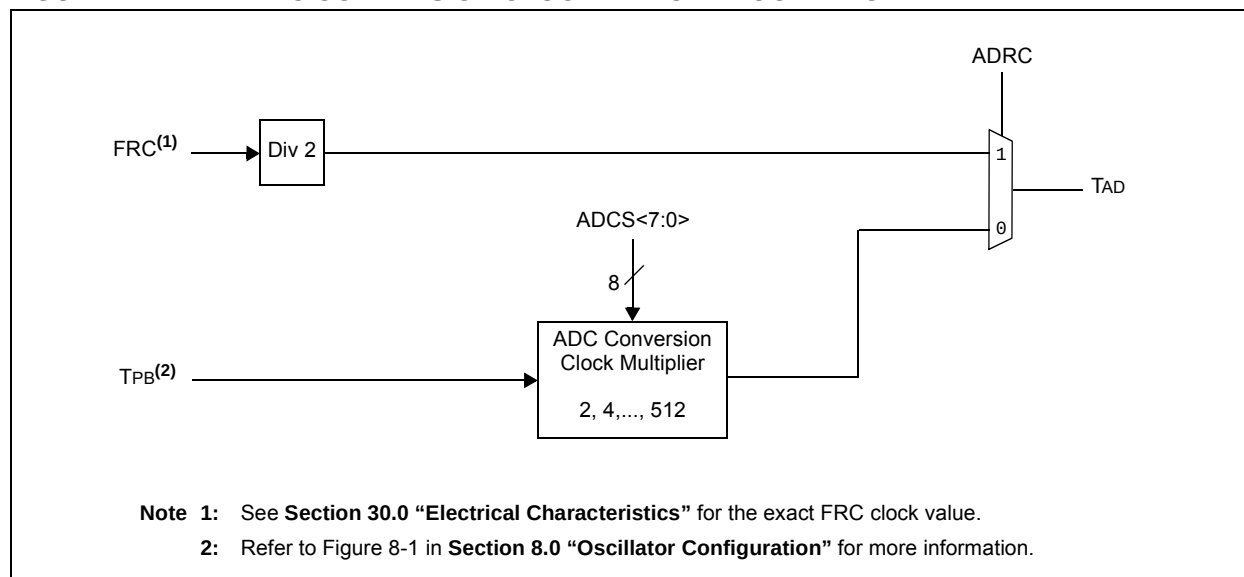
- Note**
- 1: This register is only available on 44-pin devices.
 - 2: This register is only available on PIC32MX1XX devices.
 - 3: This register is only available on 36-pin and 44-pin devices.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 22-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM



PIC32MX1XX/2XX 28/36/44-PIN FAMILY

26.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

To disable a peripheral, the associated PMDx bit must be set to '1'. To enable a peripheral, the associated PMDx bit must be cleared (default). See Table 26-1 for more information.

Note: Disabling a peripheral module while its ON bit is set, may result in undefined behavior. The ON bit for the associated peripheral module must be cleared prior to disable a module via the PMDx bits.

TABLE 26-1: PERIPHERAL MODULE DISABLE BITS AND LOCATIONS

Peripheral ⁽¹⁾	PMDx bit Name ⁽¹⁾	Register Name and Bit Location
ADC1	AD1MD	PMD1<0>
CTMU	CTMUMD	PMD1<8>
Comparator Voltage Reference	CVRMD	PMD1<12>
Comparator 1	CMP1MD	PMD2<0>
Comparator 2	CMP2MD	PMD2<1>
Comparator 3	CMP3MD	PMD2<2>
Input Capture 1	IC1MD	PMD3<0>
Input Capture 2	IC2MD	PMD3<1>
Input Capture 3	IC3MD	PMD3<2>
Input Capture 4	IC4MD	PMD3<3>
Input Capture 5	IC5MD	PMD3<4>
Output Compare 1	OC1MD	PMD3<16>
Output Compare 2	OC2MD	PMD3<17>
Output Compare 3	OC3MD	PMD3<18>
Output Compare 4	OC4MD	PMD3<19>
Output Compare 5	OC5MD	PMD3<20>
Timer1	T1MD	PMD4<0>
Timer2	T2MD	PMD4<1>
Timer3	T3MD	PMD4<2>
Timer4	T4MD	PMD4<3>
Timer5	T5MD	PMD4<4>
UART1	U1MD	PMD5<0>
UART2	U2MD	PMD5<1>
SPI1	SPI1MD	PMD5<8>
SPI2	SPI2MD	PMD5<9>
I2C1	I2C1MD	PMD5<16>
I2C2	I2C2MD	PMD5<17>
USB ⁽²⁾	USBMD	PMD5<24>
RTCC	RTCCMD	PMD6<0>
Reference Clock Output	REFOMD	PMD6<1>
PMP	PMPMD	PMD6<16>

Note 1: Not all modules and associated PMDx bits are available on all devices. See **TABLE 1: “PIC32MX1XX 28/36/44-Pin General Purpose Family Features”** and **TABLE 2: “PIC32MX2XX 28/36/44-pin USB Family Features”** for the lists of available peripherals.

2: The module must not be busy after clearing the associated ON bit and prior to setting the USBMD bit.

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-9: DC CHARACTERISTICS: I/O PIN INPUT INJECTION CURRENT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DI60a	I _{ICL}	Input Low Injection Current	0	—	-5 ^(2,5)	mA	This parameter applies to all pins, with the exception of the power pins.
DI60b	I _{ICH}	Input High Injection Current	0	—	+5 ^(3,4,5)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, and the SOSCI, SOSCO, OSC1, D+, and D- pins.
DI60c	ΣI _{ICT}	Total Input Injection Current (sum of all I/O and Control pins)	-20 ⁽⁶⁾	—	+20 ⁽⁶⁾	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (I _{ICL} + I _{ICH}) ≤ ΣI _{ICT})

- Note 1:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.
- 2:** V_{IL} source < (V_{SS} - 0.3). Characterized but not tested.
- 3:** V_{IH} source > (V_{DD} + 0.3) for non-5V tolerant pins only.
- 4:** Digital 5V tolerant pins do not have an internal high side diode to V_{DD}, and therefore, cannot tolerate any “positive” input injection current.
- 5:** Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., V_{IH} Source > (V_{DD} + 0.3) or V_{IL} source < (V_{SS} - 0.3)).
- 6:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. If **Note 2**, I_{ICL} = (((V_{SS} - 0.3) - V_{IL} source) / R_S). If **Note 3**, I_{ICH} = ((I_{ICH} source - (V_{DD} + 0.3)) / R_S). R_S = Resistance between input source voltage and device pin. If (V_{SS} - 0.3) ≤ V_{SOURCE} ≤ (V_{DD} + 0.3), injection current = 0.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ for V-temp			
Param. No.	Symbol	Characteristics		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM11	THI:SCL	Clock High Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	—
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode (Note 2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	$20 + 0.1 C_b$	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	—
			400 kHz mode	0	0.9	μs	
			1 MHz mode (Note 2)	0	0.3	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	$TPB * (BRG + 2)$	—	μs	—
			400 kHz mode	$TPB * (BRG + 2)$	—	μs	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	$TPB * (BRG + 2)$	—	ns	—
			400 kHz mode	$TPB * (BRG + 2)$	—	ns	
			1 MHz mode (Note 2)	$TPB * (BRG + 2)$	—	ns	

Note 1: BRG is the value of the I²C Baud Rate Generator.

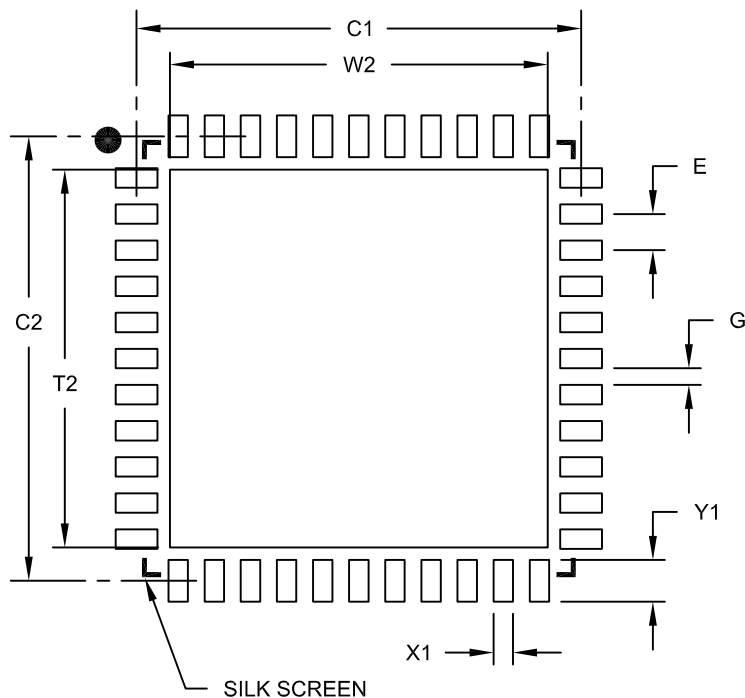
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: The typical value for this parameter is 104 ns.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.80
Optional Center Pad Length	T2			6.80
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.80
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

(64 KB RAM, 256 KB Flash)	42	DCHxSPTR (DMA Channel 'x' Source Pointer).....	99
Memory Organization	37	DCHxSSA (DMA Channel 'x' Source Start Address) ..	97
Microchip Internet Web Site	341	DCHxSSIZ (DMA Channel 'x' Source Size).....	98
MPLAB ASM30 Assembler, Linker, Librarian	254	DCRCCON (DMA CRC Control).....	90
MPLAB Integrated Development Environment Software ..	253	DCRCDATA (DMA CRC Data)	92
MPLAB PM3 Device Programmer.....	255	DCRCXOR (DMA CRCXOR Enable)	92
MPLAB REAL ICE In-Circuit Emulator System.....	255	DEVCFG0 (Device Configuration Word 0)	241
MPLINK Object Linker/MPLIB Object Librarian	254	DEVCFG1 (Device Configuration Word 1)	243
O		DEVCFG2 (Device Configuration Word 2)	245
Oscillator Configuration	73	DEVCFG3 (Device Configuration Word 3)	247
Output Compare.....	161	DEVID (Device and Revision ID).....	249
P		DMAADDR (DMA Address).....	89
Packaging	311	DMACON (DMA Controller Control)	88
Details	313	DMASTAT (DMA Status).....	89
Marking	311	I2CxCON (I2C Control).....	176
Parallel Master Port (PMP)	189	I2CxSTAT (I2C Status)	178
PIC32 Family USB Interface Diagram.....	104	ICxCON (Input Capture 'x' Control)	159
Pinout I/O Descriptions (table)	20	IECx (Interrupt Enable Control)	70
Power-on Reset (POR)		IFxSx (Interrupt Flag Status)	70
and On-Chip Voltage Regulator	250	INTCON (Interrupt Control).....	68
Power-Saving Features.....	233	INTSTAT (Interrupt Status).....	69
CPU Halted Methods	233	IPCx (Interrupt Priority Control)	71
Operation	233	IPTMR (Interrupt Proximity Timer).....	69
with CPU Running.....	233	NVMADDR (Flash Address)	56
R		NVMCON (Programming Control)	55
Real-Time Clock and Calendar (RTCC).....	199	NVMDATA (Flash Program Data).....	57
Register Maps	45--??	NVMKEY (Programming Unlock).....	56
Registers		NVMSRCADDR (Source Data Address)	57
[<i>pin name</i>]R (Peripheral Pin Select Input).....	141	OCxCON (Output Compare 'x' Control).....	163
AD1CHS (ADC Input Select)	217	OSCCON (Oscillator Control).....	76
AD1CON1 (ADC Control 1)	213	OSCTUN (FRC Tuning).....	79
AD1CON2 (ADC Control 2)	215	PMADDR (Parallel Port Address).....	195
AD1CON3 (ADC Control 3)	216	PMAEN (Parallel Port Pin Enable).....	196
AD1CSSL (ADC Input Scan Select)	218	PMCON (Parallel Port Control).....	191
ALRMDATE (Alarm Date Value)	208	PMODE (Parallel Port Mode).....	193
ALRMTIME (Alarm Time Value)	207	PMSTAT (Parallel Port Status (Slave Modes Only)) ..	197
BMXBOOTSZ (Boot Flash (IFM) Size)	51	REFOCON (Reference Oscillator Control)	80
BMXCON (Bus Matrix Configuration)	46	REFOTRIM (Reference Oscillator Trim).....	82
BMXDKPBA (Data RAM Kernel Program		RPnR (Peripheral Pin Select Output)	141
Base Address)	47	RSWRST (Software Reset)	62
BMXDRMSZ (Data RAM Size Register)	50	RTCALRM (RTC Alarm Control).....	203
BMXDUDBA (Data RAM User Data Base Address) ...	48	RTCCON (RTC Control).....	201
BMXDUPBA (Data RAM User Program		RTCDATE (RTC Date Value)	206
Base Address)	49	RTCTIME (RTC Time Value).....	205
BMXPFMSZ (Program Flash (PFM) Size)	51	SPIxCON (SPI Control)	167
BMXPUPBA (Program Flash (PFM) User Program		SPIxCON2 (SPI Control 2)	170
Base Address)	50	SPIxSTAT (SPI Status).....	171
CFGCON (Configuration Control)	248	T1CON (Type A Timer Control).....	145
CM1CON (Comparator 1 Control)	221	TxCON (Type B Timer Control).....	150
CMSTAT (Comparator Status Register)	222	U1ADDR (USB Address).....	121
CNCONx (Change Notice Control for PORTx)	142	U1BDTP1 (USB BDT Page 1)	123
CTMUCON (CTMU Control)	229	U1BDTP2 (USB BDT Page 2)	124
CVRCON (Comparator Voltage Reference Control) ..	225	U1BDTP3 (USB BDT Page 3)	124
DCHxCON (DMA Channel 'x' Control).....	93	U1CNFG1 (USB Configuration 1).....	125
DCHxCPTR (DMA Channel 'x' Cell Pointer).....	100	U1CON (USB Control).....	119
DCHxCSIZ (DMA Channel 'x' Cell-Size).....	100	U1EIE (USB Error Interrupt Enable).....	117
DCHxDAT (DMA Channel 'x' Pattern Data).....	101	U1EIR (USB Error Interrupt Status).....	115
DCHxDPTR (Channel 'x' Destination Pointer)	99	U1EP0-U1EP15 (USB Endpoint Control)	126
DCHxDSA (DMA Channel 'x' Destination		U1FRMH (USB Frame Number High)	122
Start Address)	97	U1FRML (USB Frame Number Low).....	121
DCHxDSIZ (DMA Channel 'x' Destination Size)	98	U1IE (USB Interrupt Enable)	114
DCHxECON (DMA Channel 'x' Event Control)	94	U1IR (USB Interrupt)	113
DCHxINT (DMA Channel 'x' Interrupt Control).....	95	U1OTGCON (USB OTG Control)	111
		U1OTGIE (USB OTG Interrupt Enable).....	109
		U1OTGIR (USB OTG Interrupt Status).....	108