What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f064d-i-ml

TABLE 6:   PIN NAMES FOR 28-PIN USB DEVICES

28-PIN QFN (TOP VIEW)[1,2,3,4]

PIC32MX210F016B
PIC32MX220F032B
PIC32MX230F064B
PIC32MX230F256B
PIC32MX250F128B
PIC32MX270F256B

28   1

Pin #	Full Pin Name	Pin #	Full Pin Name
1	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	15	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	16	V_{SS}
3	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	17	V_{CAP}
4	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	18	PGED2/RPB10/D+/CTED11/RB10
5	V_{SS}	19	PGEC2/RPB11/D-/RB11
6	OSC1/CLKI/RPA2/RA2	20	V_{USB3V3}
7	OSC2/CLKO/RPA3/PMA0/RA3	21	AN11/RPB13/CTPLS/PMRD/RB13
8	SOSCI/RPB4/RB4	22	CV_{REFOUT}/AN10/C3INB/RPB14/V_{BUSON}/SCK1/CTED5/RB14
9	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	23	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
10	V_{DD}	24	AV_{SS}
11	TMS/RPB5/USBID/RB5	25	AV_{DD}
12	V_{BUS}	26	$\overline{MCLR}$
13	TDI/RPB7/CTED3/PMD5/INT0/RB7	27	PGED3/V_{REF}+/CV_{REF}+/AN0/C3INC/RPA0/CTED1/PMD7/RA0
14	TCK/RPB8/SCL1/CTED10/PMD4/RB8	28	PGEC3/V_{REF}-/CV_{REF}-/AN1/RPA1/CTED2/PMD6/RA1

Note   1:   The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

2:   Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

3:   The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V_{SS} externally.

4:   Shaded pins are 5V tolerant.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number[1]				Pin Type	Buffer Type	Description
	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA			
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		—	—	27	O	—	Parallel Master Port address (Demultiplexed Master modes)
PMA3		—	—	38	O	—	
PMA4		—	—	37	O	—	
PMA5		—	—	4	O	—	
PMA6		—	—	5	O	—	
PMA7		—	—	13	O	—	
PMA8		—	—	32	O	—	
PMA9		—	—	35	O	—	
PMA10		—	—	12	O	—	
PMCS1	23	26	29	15	O	—	Parallel Master Port Chip Select 1 strobe
PMD0	20[2] 1[3]	23[2] 4[3]	26[2] 35[3]	10[2] 21[3]	I/O	TTL/ST	Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes)
PMD1	19[2] 2[3]	22[2] 5[3]	25[2] 36[3]	9[2] 22[3]	I/O	TTL/ST	
PMD2	18[2] 3[3]	21[2] 6[3]	24[2] 1[3]	8[2] 23[3]	I/O	TTL/ST	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12[2] 28[3]	15[2] 3[3]	16[2] 34[3]	42[2] 20[3]	I/O	TTL/ST	
PMD7	11[2] 27[3]	14[2] 2[3]	15[2] 33[3]	41[2] 19[3]	I/O	TTL/ST	
PMRD	21	24	27	11	O	—	Parallel Master Port read strobe
PMWR	22[2] 4[3]	25[2] 7[3]	28[2] 2[3]	14[2] 24[3]	O	—	Parallel Master Port write strobe
VBUS	12[3]	15[3]	16[3]	42[3]	I	Analog	USB bus power monitor
VUSB3V3	20[3]	23[3]	26[3]	10[3]	P	—	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22[3]	25[3]	28[3]	14[3]	O	—	USB Host and OTG bus power control output
D+	18[3]	21[3]	24[3]	8[3]	I/O	Analog	USB D+
D-	19[3]	22[3]	25[3]	9[3]	I/O	Analog	USB D-

Legend: CMOS = CMOS compatible input or output   Analog = Analog input   P = Power
        ST = Schmitt Trigger input with CMOS levels   O = Output   I = Input
        TTL = TTL input buffer   PPS = Peripheral Pin Select   — = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.
    2: Pin number for PIC32MX1XX devices only.
    3: Pin number for PIC32MX2XX devices only.

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

> **Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/36/44-pin Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VCAP pin (see **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- MCLR pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

> **Note:** The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.

- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.

- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.

- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

NOTES:

6.1   Reset Control Registers

TABLE 6-1:   RESET CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
F600	RCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CMR	VREGS	EXTR	SWR	—	WDTO	SLEEP	IDLE	BOR	POR	xxxx[2]
F610	RSWRST	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note   1:   All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

2:   Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	MVEC	—	TPC<2:0>		
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	INT4EP	INT3EP	INT2EP	INT1EP	INT0EP

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MVEC:** Multi Vector Configuration bit

1 = Interrupt controller configured for Multi-vectored mode
0 = Interrupt controller configured for Single-vectored mode

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits

111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
001 = Interrupts of group priority 1 start the Interrupt Proximity timer
000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit

1 = Rising edge
0 = Falling edge

8.1 Oscillator Control Regiters

TABLE 8-1: OSCILLATOR CONTROL REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>			x1xx[2]
		15:0	—	COSC<2:0>			—	NOSC<2:0>			CLKLOCK	ULOCK[3]	SLOCK	SLPEN	CF	UFRCEN[3]	SOSCEN	OSWEN	xxxx[2]
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000
F020	REFOCON	31:16	—	RODIV<14:0>															0000
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>				0000
F030	REFOTRIM	31:16	ROTRIM<8:0>									—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.

3: This bit is only available on PIC32MX2XX devices.

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REGISTER 9-1: **DMACON: DMA CONTROLLER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
23:16	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —
15:8	R/W-0 ON[1]	U-0 —	U-0 —	R/W-0 SUSPEND	R/W-0 DMABUSY	U-0 —	U-0 —	U-0 —
7:0	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —	U-0 —

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** DMA On bit[1]
1 = DMA module is enabled
0 = DMA module is disabled

bit 14-13 **Unimplemented:** Read as '0'

bit 12 **SUSPEND:** DMA Suspend bit
1 = DMA transfers are suspended to allow CPU uninterrupted access to data bus
0 = DMA operates normally

bit 11 **DMABUSY:** DMA Module Busy bit
1 = DMA module is active
0 = DMA module is disabled and not actively transferring data

bit 10-0 **Unimplemented:** Read as '0'

Note 1: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 10-11: U1CON: USB CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-x	R-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	JSTATE	SE0	PKTDIS[4] TOKBUSY[1,5]	USBRST	HOSTEN[2]	RESUME[3]	PPBRST	USBEN[4] SOFEN[5]

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-8   **Unimplemented:** Read as '0'

bit 7   **JSTATE:** Live Differential Receiver JSTATE flag bit
1 = JSTATE was detected on the USB
0 = No JSTATE was detected

bit 6   **SE0:** Live Single-Ended Zero flag bit
1 = Single-Ended Zero was detected on the USB
0 = No Single-Ended Zero was detected

bit 5   **PKTDIS:** Packet Transfer Disable bit[4]
1 = Token and packet processing is disabled (set upon SETUP token received)
0 = Token and packet processing is enabled
TOKBUSY: Token Busy Indicator bit[1,5]
1 = Token is being executed by the USB module
0 = No token is being executed

bit 4   **USBRST:** Module Reset bit[5]
1 = USB reset generated
0 = USB reset terminated

bit 3   **HOSTEN:** Host Mode Enable bit[2]
1 = USB host capability is enabled
0 = USB host capability is disabled

bit 2   **RESUME:** RESUME Signaling Enable bit[3]
1 = RESUME signaling is activated
0 = RESUME signaling is disabled

Note 1: Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).
    2: All host control logic is reset any time that the value of this bit is toggled.
    3: Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.
    4: Device mode.
    5: Host mode.

TABLE 11-5: PORTC REGISTER MAP

Virtual Address (BF88_#)	Register Name[1,2]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
6200	ANSELC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	ANSC3[4]	ANSC2[3]	ANSC1	ANSC0	000F
6210	TRISC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	TRISC9	TRISC8[3]	TRISC7[3]	TRISC6[3]	TRISC5[3]	TRISC4[3]	TRISC3	TRISC2[3]	TRISC1	TRISC0	03FF
6220	PORTC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	RC9	RC8[3]	RC7[3]	RC6[3]	RC5[3]	RC4[3]	RC3	RC2[3]	RC1	RC0	xxxx
6230	LATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	LATC9	LATC8[3]	LATC7[3]	LATC6[3]	LATC5[3]	LATC4[3]	LATC3	LATC2[3]	LATC1	LATC0	xxxx
6240	ODCC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	ODCC9	ODCC8[3]	ODCC7[3]	ODCC6[3]	ODCC5[3]	ODCC4[3]	ODCC3	ODCC2[3]	ODCC1	ODCC0	0000
6250	CNPUC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPUC9	CNPUC8[3]	CNPUC7[3]	CNPUC6[3]	CNPUC5[3]	CNPUC4[3]	CNPUC3	CNPUC2[3]	CNPUC1	CNPUC0	0000
6260	CNPDC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNPDC9	CNPDC8[3]	CNPDC7[3]	CNPDC6[3]	CNPDC5[3]	CNPDC4[3]	CNPDC3	CNPDC2[3]	CNPDC1	CNPDC0	0000
6270	CNCONC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
6280	CNENC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNIEC9	CNIEC8[3]	CNIEC7[3]	CNIEC6[3]	CNIEC5[3]	CNIEC4[3]	CNIEC3	CNIEC2[3]	CNIEC1	CNIEC0	0000
6290	CNSTATC	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	CNSTATC9	CNSTATC8[3]	CNSTATC7[3]	CNSTATC6[3]	CNSTATC5[3]	CNSTATC4[3]	CNSTATC3	CNSTATC2[3]	CNSTATC1	CNSTATC0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note   1:   All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

2:   PORTC is not available on 28-pin devices.

3:   This bit is only available on 44-pin devices.

4:   This bit is only available on USB-enabled devices with 36 or 44 pins.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB4C	RPB8R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB8<3:0>				0000
FB50	RPB9R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB9<3:0>				0000
FB54	RPB10R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB10<3:0>				0000
FB58	RPB11R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB11<3:0>				0000
FB60	RPB13R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB13<3:0>				0000
FB64	RPB14R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB14<3:0>				0000
FB68	RPB15R	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPB15<3:0>				0000
FB6C	RPC0R[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC0<3:0>				0000
FB70	RPC1R[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC1<3:0>				0000
FB74	RPC2R[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC2<3:0>				0000
FB78	RPC3R[3]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC3<3:0>				0000
FB7C	RPC4R[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC4<3:0>				0000
FB80	RPC5R[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC5<3:0>				0000
FB84	RPC6R[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC6<3:0>				0000
FB88	RPC7R[1]	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC7<3:0>				0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This register is only available on 44-pin devices.
2: This register is only available on PIC32MX1XX devices.
3: This register is only available on 36-pin and 44-pin devices.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

12.2 Timer1 Control Registers

TABLE 12-1: TIMER1 REGISTER MAP

Virtual Address (BF80_#)	Register Name[1]	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Resets
0600	T1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	—	SIDL	TWDIS	TWIP	—	—	—	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—	0000
0610	TMR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	TMR1<15:0>																0000
0620	PR1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	PR1<15:0>																FFFF

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

REGISTER 20-1: PMCON: PARALLEL PORT CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ON[1]	—	SIDL	ADRMUX<1:0>		PMPTTL	PTWREN	PTRDEN
7:0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0
	CSF<1:0>[2]		ALP[2]	—	CS1P[2]	—	WRSP	RDSP

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-16　**Unimplemented:** Read as '0'

bit 15　**ON:** Parallel Master Port Enable bit[1]

　　1 = PMP enabled
　　0 = PMP disabled, no off-chip access performed

bit 14　**Unimplemented:** Read as '0'

bit 13　**SIDL:** Stop in Idle Mode bit

　　1 = Discontinue module operation when the device enters Idle mode
　　0 = Continue module operation when the device enters Idle mode

bit 12-11　**ADRMUX<1:0>:** Address/Data Multiplexing Selection bits

　　11 = Lower 8 bits of address are multiplexed on PMD<7:0> pins; upper 8 bits are not used
　　10 = All 16 bits of address are multiplexed on PMD<7:0> pins
　　01 = Lower 8 bits of address are multiplexed on PMD<7:0> pins, upper bits are on PMA<10:8> and PMA<14>
　　00 = Address and data appear on separate pins

bit 10　**PMPTTL:** PMP Module TTL Input Buffer Select bit

　　1 = PMP module uses TTL input buffers
　　0 = PMP module uses Schmitt Trigger input buffer

bit 9　**PTWREN:** Write Enable Strobe Port Enable bit

　　1 = PMWR/PMENB port enabled
　　0 = PMWR/PMENB port disabled

bit 8　**PTRDEN:** Read/Write Strobe Port Enable bit

　　1 = PMRD/PMWR port enabled
　　0 = PMRD/PMWR port disabled

bit 7-6　**CSF<1:0>:** Chip Select Function bits[2]

　　11 = Reserved
　　10 = PMCS1 functions as Chip Select
　　01 = PMCS1 functions as PMA<14>
　　00 = PMCS1 functions as PMA<14>

bit 5　**ALP:** Address Latch Polarity bit[2]

　　1 = Active-high (PMALL and PMALH)
　　0 = Active-low (PMALL and PMALH)

Note 1:　When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON control bit.

　　2:　These bits have no effect when their corresponding pins are used as address lines.

REGISTER 21-5: ALRMTIME: ALARM TIME VALUE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	—	HR10<1:0>		HR01<3:0>			
23:16	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	MIN10<2:0>			MIN01<3:0>			
15:8	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
	—	SEC10<2:0>			SEC01<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31-30 **Unimplemented:** Read as '0'

bit 29-28 **HR10<1:0>:** Binary Coded Decimal value of hours bits, 10s place digit; contains a value from 0 to 2

bit 27-24 **HR01<3:0>:** Binary Coded Decimal value of hours bits, 1s place digit; contains a value from 0 to 9

bit 23 **Unimplemented:** Read as '0'

bit 22-20 **MIN10<2:0>:** Binary Coded Decimal value of minutes bits, 10s place digit; contains a value from 0 to 5

bit 19-16 **MIN01<3:0>:** Binary Coded Decimal value of minutes bits, 1s place digit; contains a value from 0 to 9

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **SEC10<2:0>:** Binary Coded Decimal value of seconds bits, 10s place digit; contains a value from 0 to 5

bit 11-8 **SEC01<3:0>:** Binary Coded Decimal value of seconds bits, 1s place digit; contains a value from 0 to 9

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 27-2: **DEVCFG1: DEVICE CONFIGURATION WORD 1 (CONTINUED)**

bit 15-14 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits

`1x` = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
`01` = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
`00` = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 13-12 **FPBDIV<1:0>:** Peripheral Bus Clock Divisor Default Value bits

`11` = PBCLK is SYSCLK divided by 8
`10` = PBCLK is SYSCLK divided by 4
`01` = PBCLK is SYSCLK divided by 2
`00` = PBCLK is SYSCLK divided by 1

bit 11 **Reserved:** Write '`1`'

bit 10 **OSCIOFNC:** CLKO Enable Configuration bit

`1` = CLKO output disabled
`0` = CLKO output signal active on the OSCO pin; Primary Oscillator must be disabled or configured for the External Clock mode (EC) for the CLKO to be active (POSCMOD<1:0> = `11` or `00`)

bit 9-8 **POSCMOD<1:0>:** Primary Oscillator Configuration bits

`11` = Primary Oscillator is disabled
`10` = HS Oscillator mode is selected
`01` = XT Oscillator mode is selected
`00` = External Clock mode is selected

bit 7 **IESO:** Internal External Switchover bit

`1` = Internal External Switchover mode is enabled (Two-Speed Start-up is enabled)
`0` = Internal External Switchover mode is disabled (Two-Speed Start-up is disabled)

bit 6 **Reserved:** Write '`1`'

bit 5 **FSOSCEN:** Secondary Oscillator Enable bit

`1` = Enable Secondary Oscillator
`0` = Disable Secondary Oscillator

bit 4-3 **Reserved:** Write '`1`'

bit 2-0 **FNOSC<2:0>:** Oscillator Selection bits

`111` = Fast RC Oscillator with divide-by-N (FRCDIV)
`110` = FRCDIV16 Fast RC Oscillator with fixed divide-by-16 postscaler
`101` = Low-Power RC Oscillator (LPRC)
`100` = Secondary Oscillator (Sosc)
`011` = Primary Oscillator (Posc) with PLL module (XT+PLL, HS+PLL, EC+PLL)
`010` = Primary Oscillator (XT, HS, EC)[1]
`001` = Fast RC Oscillator with divide-by-N with PLL module (FRCDIV+PLL)
`000` = Fast RC Oscillator (FRC)

Note 1: Do not disable the Posc (POSCMOD = `11`) when using this oscillator source.

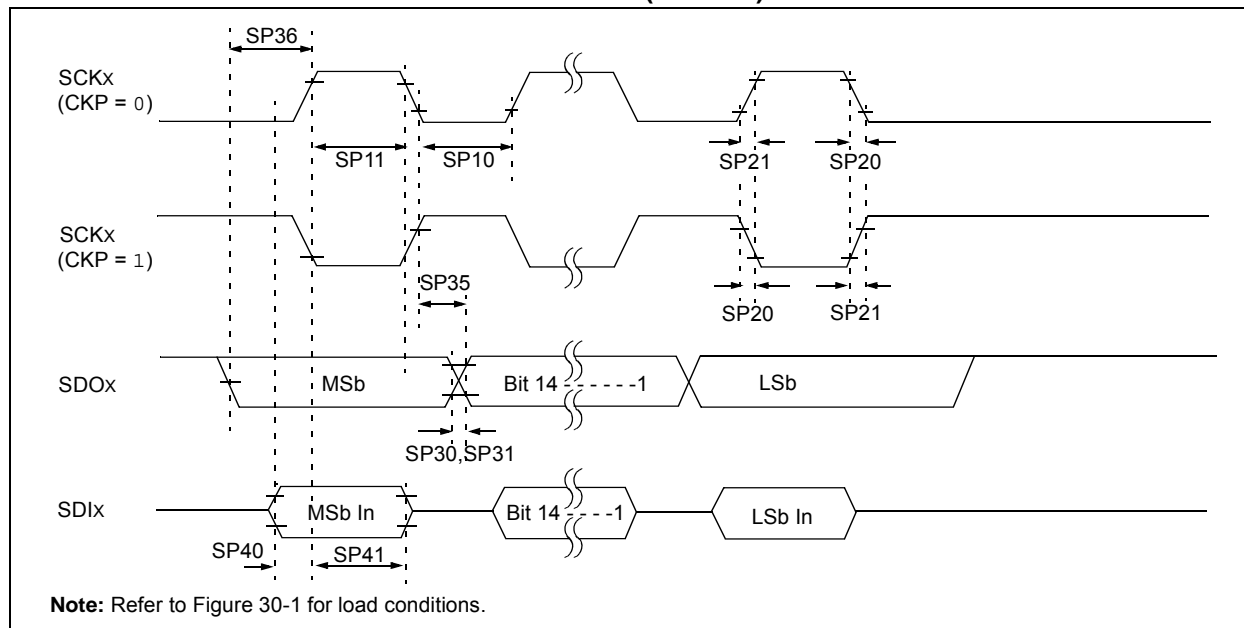**TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature $-40°C \leq T_A \leq +85°C$ for Industrial $-40°C \leq T_A \leq +105°C$ for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical[1]	Max.	Units	Conditions
	V_{IL}	**Input Low Voltage**					
DI10		I/O Pins with PMP	V_{SS}	—	0.15 V_{DD}	V	
		I/O Pins	V_{SS}	—	0.2 V_{DD}	V	
DI18		SDAx, SCLx	V_{SS}	—	0.3 V_{DD}	V	SMBus disabled **(Note 4)**
DI19		SDAx, SCLx	V_{SS}	—	0.8	V	SMBus enabled **(Note 4)**
	V_{IH}	**Input High Voltage**					
DI20		I/O Pins not 5V-tolerant[5]	0.65 V_{DD}	—	V_{DD}	V	**(Note 4,6)**
		I/O Pins 5V-tolerant with PMP[5]	0.25 V_{DD} + 0.8V	—	5.5	V	**(Note 4,6)**
		I/O Pins 5V-tolerant[5]	0.65 V_{DD}	—	5.5	V	
DI28		SDAx, SCLx	0.65 V_{DD}	—	5.5	V	SMBus disabled **(Note 4,6)**
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, $2.3V \leq V_{PIN} \leq 5.5$ **(Note 4,6)**
DI30	I_{CNPU}	**Change Notification Pull-up Current**	—	—	-50	µA	V_{DD} = 3.3V, V_{PIN} = V_{SS} **(Note 3,6)**
DI31	I_{CNPD}	**Change Notification Pull-down Current[4]**	—	—	-50	µA	V_{DD} = 3.3V, V_{PIN} = V_{DD}
	I_{IL}	**Input Leakage Current (Note 3)**					
DI50		I/O Ports	—	—	±1	µA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance
DI51		Analog Input Pins	—	—	±1	µA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at high-impedance
DI55		$\overline{MCLR}$[2]	—	—	±1	µA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
DI56		OSC1	—	—	±1	µA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT and HS modes

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the **"Pin Diagrams"** section for the 5V-tolerant pins.

6: The V_{IH} specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of I_{CNPU}. For External "input" logic inputs that require a pull-up source, to guarantee the minimum V_{IH} of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

FIGURE 30-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS

Note: Refer to Figure 30-1 for load conditions.

TABLE 30-29: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP10	T_{ScL}	SCKx Output Low Time **(Note 3)**	$T_{SCK}/2$	—	—	ns	—
SP11	T_{ScH}	SCKx Output High Time **(Note 3)**	$T_{SCK}/2$	—	—	ns	—
SP20	T_{ScF}	SCKx Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP21	T_{ScR}	SCKx Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP30	T_{DOF}	SDOx Data Output Fall Time **(Note 4)**	—	—	—	ns	See parameter DO32
SP31	T_{DOR}	SDOx Data Output Rise Time **(Note 4)**	—	—	—	ns	See parameter DO31
SP35	$T_{ScH2DOV}$, $T_{ScL2DOV}$	SDOx Data Output Valid after SCKx Edge	—	—	15	ns	$V_{DD} > 2.7V$
			—	—	20	ns	$V_{DD} < 2.7V$
SP36	T_{DOV2SC}, $T_{DOV2ScL}$	SDOx Data Output Setup to First SCKx Edge	15	—	—	ns	—
SP40	$T_{DIV2ScH}$, $T_{DIV2ScL}$	Setup Time of SDIx Data Input to SCKx Edge	15	—	—	ns	$V_{DD} > 2.7V$
			20	—	—	ns	$V_{DD} < 2.7V$
SP41	$T_{ScH2DIL}$, $T_{ScL2DIL}$	Hold Time of SDIx Data Input to SCKx Edge	15	—	—	ns	$V_{DD} > 2.7V$
			20	—	—	ns	$V_{DD} < 2.7V$

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 50 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Characteristics		Min.[1]	Max.	Units	Conditions
IM10	$T_{LO:SCL}$	Clock Low Time	100 kHz mode	T_{PB} * (BRG + 2)	—	µs	—
			400 kHz mode	T_{PB} * (BRG + 2)	—	µs	—
			1 MHz mode (Note 2)	T_{PB} * (BRG + 2)	—	µs	—
IM11	$T_{HI:SCL}$	Clock High Time	100 kHz mode	T_{PB} * (BRG + 2)	—	µs	—
			400 kHz mode	T_{PB} * (BRG + 2)	—	µs	—
			1 MHz mode (Note 2)	T_{PB} * (BRG + 2)	—	µs	—
IM20	$T_{F:SCL}$	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	C_B is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 C_B	300	ns	
			1 MHz mode (Note 2)	—	100	ns	
IM21	$T_{R:SCL}$	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	C_B is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 C_B	300	ns	
			1 MHz mode (Note 2)	—	300	ns	
IM25	$T_{SU:DAT}$	Data Input Setup Time	100 kHz mode	250	—	ns	—
			400 kHz mode	100	—	ns	
			1 MHz mode (Note 2)	100	—	ns	
IM26	$T_{HD:DAT}$	Data Input Hold Time	100 kHz mode	0	—	µs	—
			400 kHz mode	0	0.9	µs	
			1 MHz mode (Note 2)	0	0.3	µs	
IM30	$T_{SU:STA}$	Start Condition Setup Time	100 kHz mode	T_{PB} * (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	T_{PB} * (BRG + 2)	—	µs	
			1 MHz mode (Note 2)	T_{PB} * (BRG + 2)	—	µs	
IM31	$T_{HD:STA}$	Start Condition Hold Time	100 kHz mode	T_{PB} * (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	T_{PB} * (BRG + 2)	—	µs	
			1 MHz mode (Note 2)	T_{PB} * (BRG + 2)	—	µs	
IM33	$T_{SU:STO}$	Stop Condition Setup Time	100 kHz mode	T_{PB} * (BRG + 2)	—	µs	—
			400 kHz mode	T_{PB} * (BRG + 2)	—	µs	
			1 MHz mode (Note 2)	T_{PB} * (BRG + 2)	—	µs	
IM34	$T_{HD:STO}$	Stop Condition Hold Time	100 kHz mode	T_{PB} * (BRG + 2)	—	ns	—
			400 kHz mode	T_{PB} * (BRG + 2)	—	ns	
			1 MHz mode (Note 2)	T_{PB} * (BRG + 2)	—	ns	

Note 1: BRG is the value of the I^{2}C Baud Rate Generator.
2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).
3: The typical value for this parameter is 104 ns.

**FIGURE 30-23:** **EJTAG TIMING CHARACTERISTICS**


TABLE 30-42: EJTAG TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp			
Param. No.	Symbol	Description[1]	Min.	Max.	Units	Conditions
EJ1	TTCKCYC	TCK Cycle Time	25	—	ns	—
EJ2	TTCKHIGH	TCK High Time	10	—	ns	—
EJ3	TTCKLOW	TCK Low Time	10	—	ns	—
EJ4	TTSETUP	TAP Signals Setup Time Before Rising TCK	5	—	ns	—
EJ5	TTHOLD	TAP Signals Hold Time After Rising TCK	3	—	ns	—
EJ6	TTDOOUT	TDO Output Delay Time from Falling TCK	—	5	ns	—
EJ7	TTDOZSTATE	TDO 3-State Delay Time from Falling TCK	—	5	ns	—
EJ8	TTRSTLOW	TRST Low Time	25	—	ns	—
EJ9	TRF	TAP Signals Rise/Fall Time, All Input and Output	—	—	ns	—

Note 1: These parameters are characterized, but not tested in manufacturing.

FIGURE 32-6: **TYPICAL FRC FREQUENCY @ V$_{DD}$ = 3.3V**
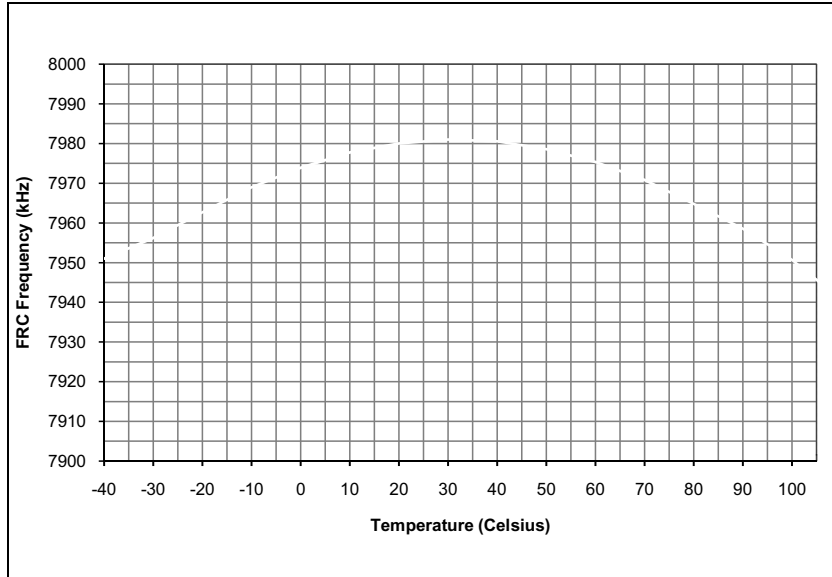
FIGURE 32-7: **TYPICAL LPRC FREQUENCY @ V$_{DD}$ = 3.3V**
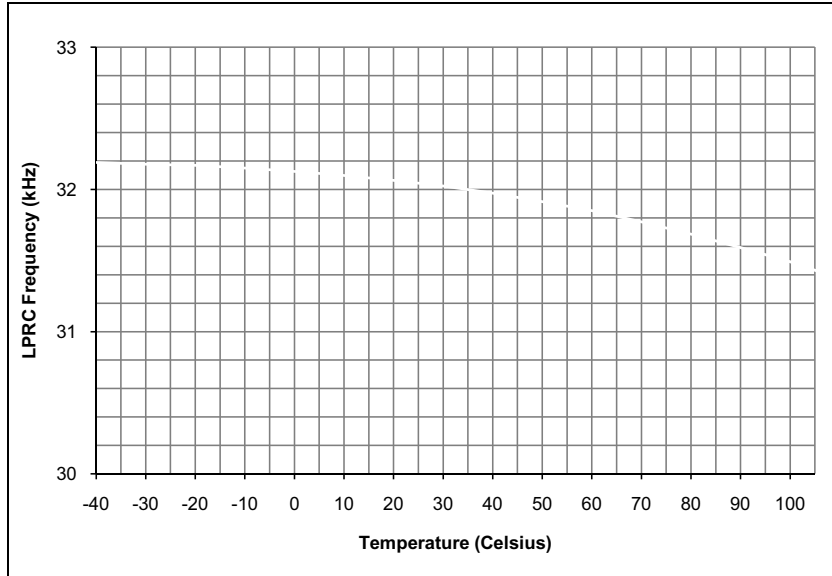
FIGURE 32-8: **TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE**