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Details

Product Status	Obsolete
Core Processor	MIPS32 ® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFTLA Exposed Pad
Supplier Device Package	44-VTLA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f064d-i-tl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

NOTES:

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3.** "Memory Organization" (DS60001115), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- · Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.



FIGURE 4-1: MEMORY MAP ON RESET FOR PIC32MX110/210 DEVICES (4 KB RAM, 16 KB FLASH)

6.0 RESETS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7.** "**Resets**" (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- Power-on Reset (POR)
- Master Clear Reset pin (MCLR)
- · Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM



	-								
Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	R/W-y	R/W-y	R/W-y	R/W-0	R/W-0	R/W-1	
31:24	—	—	P	LLODIV<2:0	>	FRCDIV<2:0>			
00.40	U-0	R-0	R-1	R-1 R/W-y		R/W-y	R/W-y	R/W-y	
23:10	—	SOSCRDY	PBDIVRDY	PBDIVRDY PBDIV<1:0>			LLMULT<2:0>	>	
45.0	U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y	
15:8	—		COSC<2:0>		—		NOSC<2:0>		
7.0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-y	R/W-0	
7:0	CLKLOCK	ULOCK ⁽¹⁾	SLOCK	SLPEN	CF	UFRCEN ⁽¹⁾	SOSCEN	OSWEN	

REGISTER 8-1: OSCCON: OSCILLATOR CONTROL REGISTER

Legend:	y = Value set from Configuration bits on POR							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'						
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown					

bit 31-30 **Unimplemented:** Read as '0'

bit 29-27 **PLLODIV<2:0>:** Output Divider for PLL

- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 26-24 FRCDIV<2:0>: Internal Fast RC (FRC) Oscillator Clock Divider bits

- 111 = FRC divided by 256
- 110 = FRC divided by 64
- 101 = FRC divided by 32
- 100 = FRC divided by 16
- 011 = FRC divided by 8
- 010 = FRC divided by 4
- 001 = FRC divided by 2 (default setting)
- 000 = FRC divided by 1
- bit 23 Unimplemented: Read as '0'
- bit 22 SOSCRDY: Secondary Oscillator (Sosc) Ready Indicator bit
 - 1 = The Secondary Oscillator is running and is stable
 - 0 = The Secondary Oscillator is still warming up or is turned off
- bit 21 **PBDIVRDY:** Peripheral Bus Clock (PBCLK) Divisor Ready bit
 - 1 = PBDIV<1:0> bits can be written
 - 0 = PBDIV<1:0> bits cannot be written
- bit 20-19 **PBDIV<1:0>:** Peripheral Bus Clock (PBCLK) Divisor bits
 - 11 = PBCLK is SYSCLK divided by 8 (default)
 - 10 = PBCLK is SYSCLK divided by 4
 - 01 = PBCLK is SYSCLK divided by 2
 - 00 = PBCLK is SYSCLK divided by 1

Note 1: This bit is only available on PIC32MX2XX devices.

Note: Writes to this register require an unlock sequence. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

REGISTE	R 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)
bit 4	CHDHIF: Channel Destination Half Full Interrupt Flag bit
	 1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2) 0 = No interrupt is pending
bit 3	CHBCIF: Channel Block Transfer Complete Interrupt Flag bit
	 1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs 0 = No interrupt is pending
bit 2	CHCCIF: Channel Cell Transfer Complete Interrupt Flag bit
	1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)0 = No interrupt is pending
bit 1	CHTAIF: Channel Transfer Abort Interrupt Flag bit
	 1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted 0 = No interrupt is pending
bit 0	CHERIF: Channel Address Error Interrupt Flag bit
	 1 = A channel address error has been detected (either the source or the destination address is invalid) 0 = No interrupt is pending

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PIC32MX1XX/2XX 28/36/44-PIN FAMILY



FIGURE 13-2: TIMER2/3, TIMER4/5 BLOCK DIAGRAM (32-BIT)

Bit Range	Bit Bit 31/23/15/7 30/22/14/6		Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0 U-0		U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
15:8	ON ⁽¹⁾	—	SIDL	IREN	RTSMD	—	UEN	<1:0>
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	WAKE	LPBACK	ABAUD	RXINV	BRGH	PDSEL	<1:0>	STSEL

REGISTER 19-1: UXMODE: UARTX MODE REGISTER

Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 ON: UARTx Enable bit⁽¹⁾
 - 1 = UARTx is enabled. UARTx pins are controlled by UARTx as defined by the UEN<1:0> and UTXEN control bits.
 - 0 = UARTx is disabled. All UARTx pins are controlled by corresponding bits in the PORTx, TRISx and LATx registers; UARTx power consumption is minimal.
- bit 14 Unimplemented: Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

- 1 = Discontinue module operation when the device enters Idle mode
- 0 = Continue module operation when the device enters Idle mode
- bit 12 IREN: IrDA Encoder and Decoder Enable bit
 - 1 = IrDA is enabled
 - 0 = IrDA is disabled
- bit 11 **RTSMD:** Mode Selection for UxRTS Pin bit
 - 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
 - $0 = \overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 Unimplemented: Read as '0'
- bit 9-8 UEN<1:0>: UARTx Enable bits
 - 11 = UxTX, UxRX and UxBCLK pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 10 = UxTX, UxRX, UxCTS and UxRTS pins are enabled and used
 - 01 = UxTX, UxRX and UxRTS pins are enabled and used; UxCTS pin is controlled by corresponding bits in the PORTx register
 - 00 = UxTX and UxRX pins are enabled and used; UxCTS and UxRTS/UxBCLK pins are controlled by corresponding bits in the PORTx register
- bit 7 WAKE: Enable Wake-up on Start bit Detect During Sleep Mode bit
 - 1 = Wake-up enabled
 - 0 = Wake-up disabled
- bit 6 LPBACK: UARTx Loopback Mode Select bit
 - 1 = Loopback mode is enabled
 - 0 = Loopback mode is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0				
24.24	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0				
31:24	—	—	—	—	—	—	CAL<9):8>				
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
23.10	CAL<7:0>											
45.0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0				
15:8	ON ^(1,2)	—	SIDL	_	—	—	—	—				
7.0	R/W-0	R-0	U-0	U-0	R/W-0	R-0	R-0	R/W-0				
7:0	RTSECSEL ⁽³⁾	RTCCLKON	—	—	RTCWREN ⁽⁴⁾	RTCSYNC	HALFSEC ⁽⁵⁾	RTCOE				

REGISTER 21-1: RTCCON: RTC CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-26 Unimplemented: Read as '0'

bit 25-16 CAL<9:0>: RTC Drift Calibration bits, which contain a signed 10-bit integer value 0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute 000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute 000000000 = No adjustment 1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute 100000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute ON: RTCC On bit^(1,2) bit 15 1 = RTCC module is enabled 0 = RTCC module is disabled bit 14 Unimplemented: Read as '0' bit 13 SIDL: Stop in Idle Mode bit 1 = Disables the PBCLK to the RTCC when the device enters Idle mode 0 = Continue normal operation when the device enters Idle mode bit 12-8 Unimplemented: Read as '0' bit 7 RTSECSEL: RTCC Seconds Clock Output Select bit⁽³⁾ 1 = RTCC Seconds Clock is selected for the RTCC pin 0 = RTCC Alarm Pulse is selected for the RTCC pin bit 6 RTCCLKON: RTCC Clock Enable Status bit 1 = RTCC Clock is actively running 0 = RTCC Clock is not running **Note 1:** The ON bit is only writable when RTCWREN = 1. 2: When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit. 3: Requires RTCOE = 1 (RTCCON<0>) for the output to be active. 4: The RTCWREN bit can be set only when the write sequence is enabled. 5: This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

Note: This register is reset only on a Power-on Reset (POR).

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22.0 **10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)**

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 17. "10-bit Analog-to-Digital Converter (ADC)" (DS60001104), which is available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32).

The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- · Up to 1 Msps conversion speed

FIGURE 22-1:

- Up to 13 analog input pins
- External voltage reference input pins
- · One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- · 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- · Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.



5: This selection is only used with CTMU capacitive and time measurement.

ADC1 MODULE BLOCK DIAGRAM

Bit Range	Bit Bit ge 31/23/15/7 30/22/14/6		Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0 U-0		U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R-0
15:8	ON ⁽¹⁾	COE	CPOL ⁽²⁾	—	—	—	—	COUT
7.0	R/W-1	R/W-1	U-0	R/W-0	U-0	U-0	R/W-1	R/W-1
7:0	EVPOL	_<1:0>	_	CREF	_	_	CCH	<1:0>

REGISTER 23-1: CMXCON: COMPARATOR CONTROL REGISTER

Legend:

5							
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'					
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown				

bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Comparator ON bit⁽¹⁾
 - 1 = Module is enabled. Setting this bit does not affect the other bits in this register
 - 0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in this register
- bit 14 **COE:** Comparator Output Enable bit
 - 1 = Comparator output is driven on the output CxOUT pin
 - 0 = Comparator output is not driven on the output CxOUT pin
- bit 13 **CPOL:** Comparator Output Inversion bit⁽²⁾
 - 1 = Output is inverted
 - 0 = Output is not inverted
- bit 12-9 Unimplemented: Read as '0'
- bit 8 **COUT:** Comparator Output bit
 - 1 = Output of the Comparator is a '1'
 - 0 = Output of the Comparator is a '0'
- bit 7-6 **EVPOL<1:0>:** Interrupt Event Polarity Select bits
 - 11 = Comparator interrupt is generated on a low-to-high or high-to-low transition of the comparator output
 - 10 = Comparator interrupt is generated on a high-to-low transition of the comparator output
 - 01 = Comparator interrupt is generated on a low-to-high transition of the comparator output
 - 00 = Comparator interrupt generation is disabled
- bit 5 Unimplemented: Read as '0'
- bit 4 CREF: Comparator Positive Input Configure bit
 - 1 = Comparator non-inverting input is connected to the internal CVREF
 - 0 = Comparator non-inverting input is connected to the CXINA pin
- bit 3-2 Unimplemented: Read as '0'
- bit 1-0 CCH<1:0>: Comparator Negative Input Select bits for Comparator
 - 11 = Comparator inverting input is connected to the IVREF
 - 10 = Comparator inverting input is connected to the CxIND pin
 - 01 = Comparator inverting input is connected to the CxINC pin
 - 00 = Comparator inverting input is connected to the CxINB pin
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
 - 2: Setting this bit will invert the signal to the comparator interrupt generator as well. This will result in an interrupt being generated on the opposite edge from the one selected by EVPOL<1:0>.

24.1 Comparator Voltage Reference Control Register

Virtual Address (BF80_#)	Register Name ⁽¹⁾ Bit Range	Bits																	
		Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
																	/		
0000	CVRCON	31:16	_	—	_	_	_	—	_	_	_	—	-	_	-	—	—	_	0000
9000	CVRCON	15:0	ON	_		_	_	_	_	_	_	CVROE	CVRR	CVRSS		CVR<	3:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

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The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- · On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

- Note 1: Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a Posc of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.
 - 2: Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from Posc to LPRC just prior to entering Sleep in order to save power. No oscillator startup delay would be applied when exiting Idle. However, when switching back to Posc, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a WAIT instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

REGISTER 27-1: DEVCFG0: DEVICE CONFIGURATION WORD 0 (CONTINUED)

bit 18-10 **PWP<8:0>:** Program Flash Write-Protect bits⁽³⁾

	Prevents selected program Flash memory pages from being modified during code execution.
	11111111 = Disabled 11111111 = Memory below 0x0400 address is write-protected 11111110 = Memory below 0x0800 address is write-protected 11111100 = Memory below 0x0C00 address is write-protected 111111011 = Memory below 0x1000 (4K) address is write-protected 111111010 = Memory below 0x1400 address is write-protected 111111001 = Memory below 0x1800 address is write-protected 111111000 = Memory below 0x1C00 address is write-protected 111111011 = Memory below 0x2000 (8K) address is write-protected
	111110110 = Memory below 0x2400 address is write-protected 111110101 = Memory below 0x2800 address is write-protected 111110100 = Memory below 0x2C00 address is write-protected 111110011 = Memory below 0x3000 address is write-protected
	111110010 = Memory below 0x3400 address is write-protected 111110001 = Memory below 0x3800 address is write-protected 11110000 = Memory below 0x3C00 address is write-protected 111101111 = Memory below 0x4000 (16K) address is write-protected
	110111111 = Memory below 0x10000 (64K) address is write-protected
	: 101111111 = Memory below 0x20000 (128K) address is write-protected
	• 011111111 = Memory below 0x40000 (256K) address is write-protected •
	• 000000000 = All possible memory is write-protected
bit 9-5	Reserved: Write '1'
bit 4-3	ICESEL<1:0>: In-Circuit Emulator/Debugger Communication Channel Select bits ⁽²⁾ 11 = PGEC1/PGED1 pair is used 10 = PGEC2/PGED2 pair is used 01 = PGEC3/PGED3 pair is used 00 = PGEC4/PGED4 pair is used ⁽²⁾
bit 2	JTAGEN: JTAG Enable bit ⁽¹⁾ 1 = JTAG is enabled 0 = JTAG is disabled
bit 1-0	DEBUG<1:0>: Background Debugger Enable bits (forced to '11' if code-protect is enabled) 1x = Debugger is disabled 0x = Debugger is enabled
Note 1: 2:	This bit sets the value for the JTAGEN bit in the CFGCON register. The PGEC4/PGED4 pin pair is not available on all devices. Refer to the " Pin Diagrams " section for availability.

3: The PWP<8:7> bits are only available on devices with 256 KB Flash.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	R	R	R	R	R	R	R	R	
31:24		VER<	3:0> (1)			Bit 19/11/3 Bit 26/18/10/2 25 R R DEVID<27:2	27:24> ⁽¹⁾		
00.40	R	R	R	R	R	R	R	R	
23:10	DEVID<23:16> ⁽¹⁾								
45.0	R	R	R	R	R	R	R	R	
15:8	DEVID<15:8> ⁽¹⁾								
7:0	R	R	R	R	R	R	R	R	
	DEVID<7:0>(1)								

REGISTER 27-6: DEVID: DEVICE AND REVISION ID REGISTER

Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 VER<3:0>: Revision Identifier bits⁽¹⁾

bit 27-0 DEVID<27:0>: Device ID bits⁽¹⁾

Note 1: See the "*PIC32 Flash Programming Specification*" (DS60001145) for a list of Revision and Device ID values.

27.3 On-Chip Voltage Regulator

All PIC32MX1XX/2XX 28/36/44-pin Family devices' core and digital logic are designed to operate at a nominal 1.8V. To simplify system designs, most devices in the PIC32MX1XX/2XX 28/36/44-pin Family family incorporate an on-chip regulator providing the required core logic voltage from VDD.

A low-ESR capacitor (such as tantalum) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in **Section 30.1 "DC Characteristics"**.

Note:	It is important that the low-ESR capacitor
	is placed as close as possible to the VCAP
	pin.

27.3.1 ON-CHIP REGULATOR AND POR

It takes a fixed delay for the on-chip regulator to generate an output. During this time, designated as TPU, code execution is disabled. TPU is applied every time the device resumes operation after any power-down, including Sleep mode.

27.3.2 ON-CHIP REGULATOR AND BOR

PIC32MX1XX/2XX 28/36/44-pin Family devices also have a simple brown-out capability. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<1>). The brown-out voltage levels are specific in **Section 30.1 "DC Characteristics"**.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP REGULATOR



27.4 **Programming and Diagnostics**

PIC32MX1XX/2XX 28/36/44-pin Family devices provide a complete range of programming and diagnostic features that can increase the flexibility of any application using them. These features allow system designers to include:

- Simplified field programmability using two-wire In-Circuit Serial Programming[™] (ICSP[™]) interfaces
- Debugging using ICSP
- Programming and debugging capabilities using the EJTAG extension of JTAG
- JTAG boundary scan testing for device and board diagnostics

PIC32 devices incorporate two programming and diagnostic modules, and a trace controller, that provide a range of functions to the application developer.

Figure 27-2 illustrates a block diagram of the programming, debugging, and trace ports.





29.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac OS[®] X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- · Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window
- Project-Based Workspaces:
- Multiple projects
- Multiple tools
- · Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

DC CHARACTERISTICS		Standard Operating Condition (unless otherwise stated) Operating temperature -40 -40			nditions ed) -40°C ≤ -40°C ≤	itions: 2.3V to 3.6V $0^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $0^{\circ}C \le TA \le +105^{\circ}C$ for V-temp	
Param.	am. Symbol Characteristic Min. Typ. Max.		Units	Conditions			
DO10	Vol	Output Low Voltage	_	_	0.4	V	$\text{Iol} \leq 10 \text{ mA}, \text{ Vdd} = 3.3 \text{V}$
DO20	Vон	Output High Voltage	1.5 ⁽¹⁾	_	_		IOH \ge -14 mA, VDD = 3.3V
		I/O Pins	2.0 ⁽¹⁾	—	—		IOH \ge -12 mA, VDD = 3.3V
			2.4	_	_	v	Ioh \geq -10 mA, Vdd = 3.3V
			3.0(1)	_	_		$IOH \ge -7 \text{ mA}, \text{ VDD} = 3.3 \text{V}$

TABLE 30-10: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

Note 1: Parameters are characterized, but not tested.

TABLE 30-11: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$				
Param. No.	Symbol	Characteristics	Min. ⁽¹⁾	Typical	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD transition high-to-low ⁽²⁾	2.0		2.3	V	_

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN.

PIC32MX1XX/2XX 28/36/44-PIN FAMILY

FIGURE 30-20: PARALLEL SLAVE PORT TIMING





TYPICAL FRC FREQUENCY @ VDD = 3.3V



FIGURE 32-6: