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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f256b-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f256b-i-ml</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 2: PIC32MX2XX 28/36/44-PIN USB FAMILY FEATURES**

Device	Pins	Program Memory (KB) <sup>(1)</sup>	Data Memory (KB)	Remappable Peripherals					Analog Comparators	USB On-The-Go (OTG)	I <sup>2</sup> C	PMP	DMA Channels (Programmable/Dedicated)	CTMU	10-bit 1 Msps ADC (Channels)	RTCC	I/O Pins	JTAG	Packages
				Remappable Pins	Timers <sup>(2)</sup> /Capture/Compare	UART	SPI <sup>(3)</sup> /S	External Interrupts <sup>(3)</sup>											
PIC32MX210F016B	28	16+3	4	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX210F016C	36	16+3	4	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	25	Y	VTLA
PIC32MX210F016D	44	16+3	4	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX220F032B	28	32+3	8	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX220F032C	36	32+3	8	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX220F032D	44	32+3	8	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX230F064B	28	64+3	16	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX230F064C	36	64+3	16	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX230F064D	44	64+3	16	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX250F128B	28	128+3	32	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX250F128C	36	128+3	32	23	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	12	Y	23	Y	VTLA
PIC32MX250F128D	44	128+3	32	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX230F256B	28	256+3	16	20	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX230F256D	44	256+3	16	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX270F256B	28	256+3	64	19	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	9	Y	19	Y	SOIC, SSOP, SPDIP, QFN
PIC32MX270F256D	44	256+3	64	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN
PIC32MX270F256DB <sup>(4)</sup>	44	256+3	64	31	5/5/5	2	2	5	3	Y	2	Y	4/2	Y	13	Y	33	Y	VTLA, TQFP, QFN

**Note 1:** This device features 3 KB of boot Flash memory.

**2:** Four out of five timers are remappable.

**3:** Four out of five external interrupts are remappable.

**4:** This PIC32 device is targeted to specific audio software packages that are tracked for licensing royalty purposes. All peripherals and electrical characteristics are identical to their corresponding base part numbers.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

## 8.1 Oscillator Control Registers

**TABLE 8-1: OSCILLATOR CONTROL REGISTER MAP**

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits															All Resets		
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1		16/0	
F000	OSCCON	31:16	—	—	PLLODIV<2:0>			FRCDIV<2:0>			—	SOSCRDY	PBDIVRDY	PBDIV<1:0>		PLLMULT<2:0>			x1xx <sup>(2)</sup>	
		15:0	COSC<2:0>				—	NOSC<2:0>			CLKLOCK	ULOCK <sup>(3)</sup>	SLOCK	SLPEN	CF	UFRGEN <sup>(3)</sup>	SOSCEN	OSWEN	xxxx <sup>(2)</sup>	
F010	OSCTUN	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
		15:0	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000	
F020	REFOCON	31:16	—	RODIV<14:0>															0000	
		15:0	ON	—	SIDL	OE	RSLP	—	DIVSWEN	ACTIVE	—	—	—	—	ROSEL<3:0>			0000		
F030	REFOTRIM	31:16	ROTRIM<8:0>										—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.
  - 2: Reset values are dependent on the DEVCFGx Configuration bits and the type of reset.
  - 3: This bit is only available on PIC32MX2XX devices.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	CHBUSY	—	—	—	—	—	—	CHCHNS <sup>(1)</sup>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R/W-0	R/W-0
	CHEN <sup>(2)</sup>	CHAED	CHCHN	CHAEN	—	CHEDET	CHPRI<1:0>	

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit

1 = Channel is active or has been enabled

0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit<sup>(1)</sup>

1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)

0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit<sup>(2)</sup>

1 = Channel is enabled

0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit

1 = Channel start/abort events will be registered, even if the channel is disabled

0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit

1 = Allow channel to be chained

0 = Do not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit

1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete

0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit

1 = An event has been detected

0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits

11 = Channel has priority 3 (highest)

10 = Channel has priority 2

01 = Channel has priority 1

00 = Channel has priority 0

**Note 1:** The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

**2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE <sup>(1)</sup>	URSTIE <sup>(2)</sup> DETACHIE <sup>(3)</sup>

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **STALLIE:** STALL Handshake Interrupt Enable bit

1 = STALL interrupt is enabled  
0 = STALL interrupt is disabled

bit 6 **ATTACHIE:** ATTACH Interrupt Enable bit

1 = ATTACH interrupt is enabled  
0 = ATTACH interrupt is disabled

bit 5 **RESUMEIE:** RESUME Interrupt Enable bit

1 = RESUME interrupt is enabled  
0 = RESUME interrupt is disabled

bit 4 **IDLEIE:** Idle Detect Interrupt Enable bit

1 = Idle interrupt is enabled  
0 = Idle interrupt is disabled

bit 3 **TRNIE:** Token Processing Complete Interrupt Enable bit

1 = TRNIF interrupt is enabled  
0 = TRNIF interrupt is disabled

bit 2 **SOFIE:** SOF Token Interrupt Enable bit

1 = SOFIF interrupt is enabled  
0 = SOFIF interrupt is disabled

bit 1 **UERRIE:** USB Error Interrupt Enable bit<sup>(1)</sup>

1 = USB Error interrupt is enabled  
0 = USB Error interrupt is disabled

bit 0 **URSTIE:** USB Reset Interrupt Enable bit<sup>(2)</sup>

1 = URSTIF interrupt is enabled  
0 = URSTIF interrupt is disabled

**DETACHIE:** USB Detach Interrupt Enable bit<sup>(3)</sup>

1 = DATTCHIF interrupt is enabled  
0 = DATTCHIF interrupt is disabled

**Note 1:** For an interrupt to propagate USBIF, the UERRIE (U1IE<1>) bit must be set.

**2:** Device mode.

**3:** Host mode.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 10-21: U1EP0-U1EP15: USB ENDPOINT CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPD	RETRYDIS	—	EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSK

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **LSPD:** Low-Speed Direct Connection Enable bit (Host mode and U1EP0 only)

1 = Direct connection to a Low-Speed device enabled

0 = Direct connection to a Low-Speed device disabled; hub required with PRE\_PID

bit 6 **RETRYDIS:** Retry Disable bit (Host mode and U1EP0 only)

1 = Retry NAKed transactions disabled

0 = Retry NAKed transactions enabled; retry done in hardware

bit 5 **Unimplemented:** Read as '0'

bit 4 **EPCONDIS:** Bidirectional Endpoint Control bit

If EPTXEN = 1 and EPRXEN = 1:

1 = Disable Endpoint n from Control transfers; only TX and RX transfers allowed

0 = Enable Endpoint n for Control (SETUP) transfers; TX and RX transfers also allowed

Otherwise, this bit is ignored.

bit 3 **EPRXEN:** Endpoint Receive Enable bit

1 = Endpoint n receive is enabled

0 = Endpoint n receive is disabled

bit 2 **EPTXEN:** Endpoint Transmit Enable bit

1 = Endpoint n transmit is enabled

0 = Endpoint n transmit is disabled

bit 1 **EPSTALL:** Endpoint Stall Status bit

1 = Endpoint n was stalled

0 = Endpoint n was not stalled

bit 0 **EPHSK:** Endpoint Handshake Enable bit

1 = Endpoint Handshake is enabled

0 = Endpoint Handshake is disabled (typically used for isochronous endpoints)

TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)

Virtual Address (BF80_#)	Register Name	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
FB8C	RPC8R <sup>(1)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC8<3:0>				0000
FB90	RPC9R <sup>(3)</sup>	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	—	—	—	—	—	—	—	—	—	—	RPC9<3:0>				0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

- Note**
- 1: This register is only available on 44-pin devices.
  - 2: This register is only available on PIC32MX1XX devices.
  - 3: This register is only available on 36-pin and 44-pin devices.



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## REGISTER 18-1: I2CxCON: I<sup>2</sup>C CONTROL REGISTER (CONTINUED)

- bit 7     **GCEN:** General Call Enable bit (when operating as I<sup>2</sup>C slave)  
1 = Enable interrupt when a general call address is received in the I2CxRSR (module is enabled for reception)  
0 = General call address is disabled
- bit 6     **STREN:** SCLx Clock Stretch Enable bit (when operating as I<sup>2</sup>C slave)  
Used in conjunction with SCLREL bit.  
1 = Enable software or receive clock stretching  
0 = Disable software or receive clock stretching
- bit 5     **ACKDT:** Acknowledge Data bit (when operating as I<sup>2</sup>C master, applicable during master receive)  
Value that is transmitted when the software initiates an Acknowledge sequence.  
1 = Send a NACK during an Acknowledge sequence  
0 = Send an ACK during an Acknowledge sequence
- bit 4     **ACKEN:** Acknowledge Sequence Enable bit (when operating as I<sup>2</sup>C master, applicable during master receive)  
1 = Initiate Acknowledge sequence on SDAx and SCLx pins and transmit ACKDT data bit.  
Hardware clear at end of master Acknowledge sequence.  
0 = Acknowledge sequence not in progress
- bit 3     **RCEN:** Receive Enable bit (when operating as I<sup>2</sup>C master)  
1 = Enables Receive mode for I<sup>2</sup>C. Hardware clear at end of eighth bit of master receive data byte.  
0 = Receive sequence not in progress
- bit 2     **PEN:** Stop Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Stop condition on SDAx and SCLx pins. Hardware clear at end of master Stop sequence.  
0 = Stop condition not in progress
- bit 1     **RSEN:** Repeated Start Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Repeated Start condition on SDAx and SCLx pins. Hardware clear at end of master Repeated Start sequence.  
0 = Repeated Start condition not in progress
- bit 0     **SEN:** Start Condition Enable bit (when operating as I<sup>2</sup>C master)  
1 = Initiate Start condition on SDAx and SCLx pins. Hardware clear at end of master Start sequence.  
0 = Start condition not in progress

**Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

## 21.1 RTCC Control Registers

TABLE 21-1: RTCC REGISTER MAP

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
0200	RTCCON	31:16	—	—	—	—	—	—	CAL<9:0>										0000
		15:0	ON	—	SIDL	—	—	—	—	—	RTSECSSEL	RTCCLKON	—	—	—	RTCWREN	RTCSYNC	HALFSEC	RTC0E
0210	RTCALRM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ALRMEN	CHIME	PIV	ALRMSYNC	AMASK<3:0>					ARPT<7:0>							0000
0220	RTCTIME	31:16	—	—	HR10<1:0>		HR01<3:0>				—	MIN10<2:0>			MIN01<3:0>				xxxx
		15:0	—	SEC10<2:0>				SEC01<3:0>				—	—	—	—	—	—	—	—
0230	RTCDATE	31:16	YEAR10<3:0>				YEAR01<3:0>				—	—	—	MONTH10	MONTH01<3:0>				xxxx
		15:0	—	—	DAY10<1:0>		DAY01<3:0>				—	—	—	—	—	WDAY01<2:0>			xx00
0240	ALRMTIME	31:16	—	—	HR10<1:0>		HR01<3:0>				—	MIN10<2:0>			MIN01<3:0>				xxxx
		15:0	—	SEC10<2:0>				SEC01<3:0>				—	—	—	—	—	—	—	—
0250	ALRMDATE	31:16	—	—	—	—	—	—	—	—	—	—	—	MONTH10	MONTH01<3:0>				00xx
		15:0	DAY10<3:0>				DAY01<3:0>				—	—	—	—	—	WDAY01<2:0>			xx0x

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 21-2: RTCALRM: RTC ALARM CONTROL REGISTER (CONTINUED)

bit 7-0 **ARPT<7:0>**: Alarm Repeat Counter Value bits<sup>(2)</sup>

11111111 = Alarm will trigger 256 times

•  
•  
•

00000000 = Alarm will trigger one time

The counter decrements on any alarm event. The counter only rolls over from 0x00 to 0xFF if CHIME = 1.

- Note 1:** Hardware clears the ALRMEN bit anytime the alarm event occurs, when ARPT<7:0> = 00 and CHIME = 0.
- 2:** This field should not be written when the RTCC ON bit = '1' (RTCCON<15>) and ALRMSYNC = 1.
- 3:** This assumes a CPU read will execute in less than 32 PBCLKs.

<b>Note:</b> This register is reset only on a Power-on Reset (POR).
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# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 22.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 17. “10-bit Analog-to-Digital Converter (ADC)”** (DS60001104), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

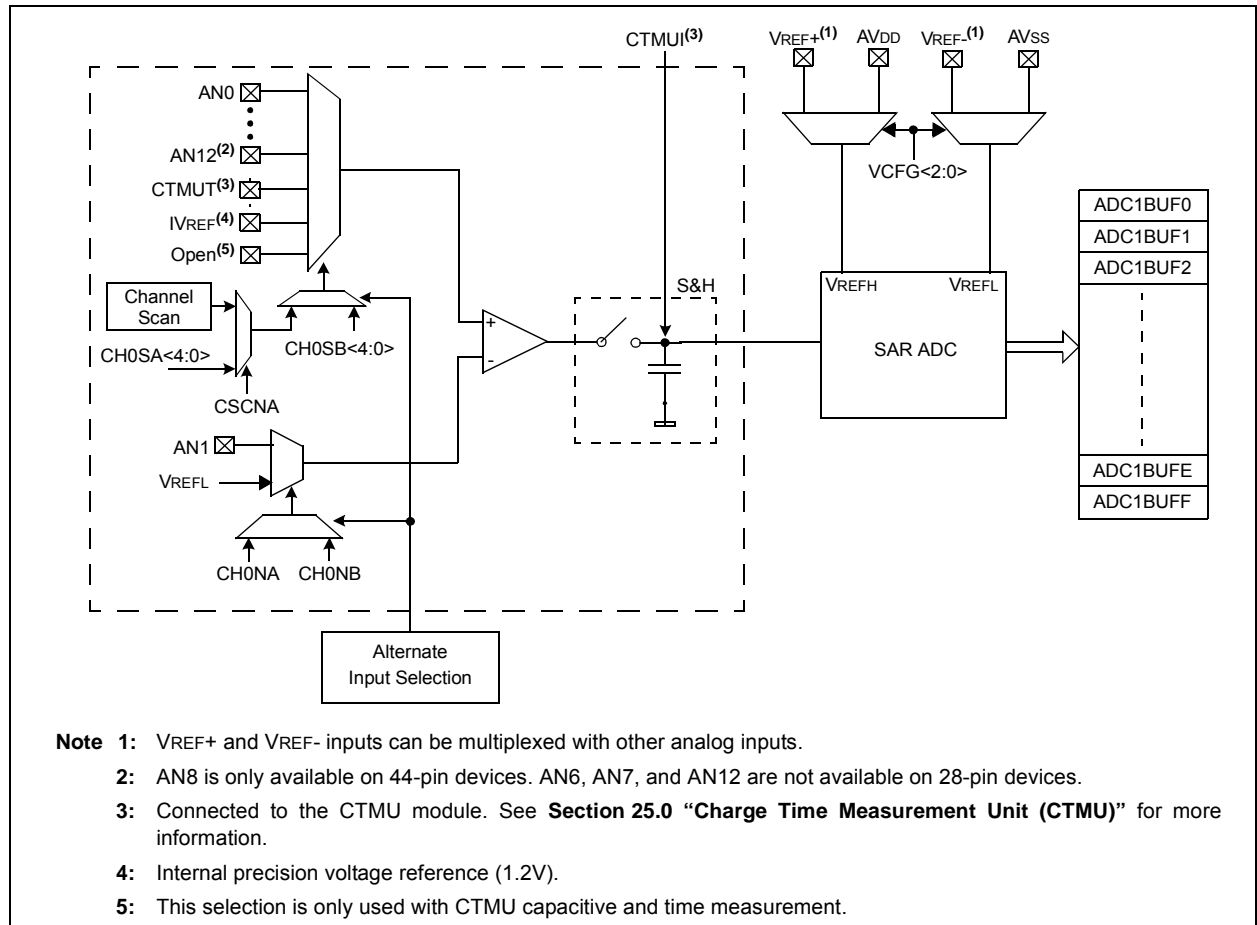
The 10-bit Analog-to-Digital Converter (ADC) includes the following features:

- Successive Approximation Register (SAR) conversion
- Up to 1 Msps conversion speed

- Up to 13 analog input pins
- External voltage reference input pins
- One unipolar, differential Sample and Hold Amplifier (SHA)
- Automatic Channel Scan mode
- Selectable conversion trigger source
- 16-word conversion result buffer
- Selectable buffer fill modes
- Eight conversion result format options
- Operation during Sleep and Idle modes

A block diagram of the 10-bit ADC is illustrated in Figure 22-1. Figure 22-2 illustrates a block diagram of the ADC conversion clock period. The 10-bit ADC has up to 13 analog input pins, designated AN0-AN12. In addition, there are two analog input pins for external voltage reference connections. These voltage reference inputs may be shared with other analog input pins and may be common to other analog module references.

**FIGURE 22-1: ADC1 MODULE BLOCK DIAGRAM**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/P	R/P	R/P	R/P	r-1	r-1	r-1	r-1
	FVBUSONIO	FUSBIDIO	IOL1WAY	PMDL1WAY	—	—	—	—
23:16	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
	—	—	—	—	—	—	—	—
15:8	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<15:8>							
7:0	R/P	R/P	R/P	R/P	R/P	R/P	R/P	R/P
	USERID<7:0>							

<b>Legend:</b>	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

- bit 31 **FVBUSONIO:** USB VBUSON Selection bit  
1 = VBUSON pin is controlled by the USB module  
0 = VBUSON pin is controlled by the port function
- bit 30 **FUSBIDIO:** USB USBID Selection bit  
1 = USBID pin is controlled by the USB module  
0 = USBID pin is controlled by the port function
- bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit  
1 = Allow only one reconfiguration  
0 = Allow multiple reconfigurations
- bit 28 **PMDL1WAY:** Peripheral Module Disable Configuration bit  
1 = Allow only one reconfiguration  
0 = Allow multiple reconfigurations
- bit 27-16 **Reserved:** Write '1'
- bit 15-0 **USERID<15:0>:** User ID bits  
This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**TABLE 30-12: DC CHARACTERISTICS: PROGRAM MEMORY**

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-temp				
Param. No.	Symbol	Characteristics	Min.	Typical <sup>(1)</sup>	Max.	Units	Conditions
<b>Program Flash Memory<sup>(3)</sup></b>							
D130	EP	Cell Endurance	20,000	—	—	E/W	—
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	2.3	—	3.6	V	—
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	—	411	—	FRC Cycles	See <b>Note 4</b>
D136	TRW	Row Write Cycle Time	—	6675	—		See <b>Note 2,4</b>
D137	TPE	Page Erase Cycle Time	—	20011	—		See <b>Note 4</b>
	TCE	Chip Erase Cycle Time	—	80180	—		See <b>Note 4</b>

**Note 1:** Data in “Typical” column is at 3.3V, 25°C unless otherwise stated.

**2:** The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

**3:** Refer to the “PIC32 Flash Programming Specification” (DS60001145) for operating conditions during programming and erase cycles.

**4:** This parameter depends on FRC accuracy (See Table 30-19) and FRC tuning values (See Register 8-2).

FIGURE 32-6: TYPICAL FRC FREQUENCY @ V<sub>DD</sub> = 3.3V

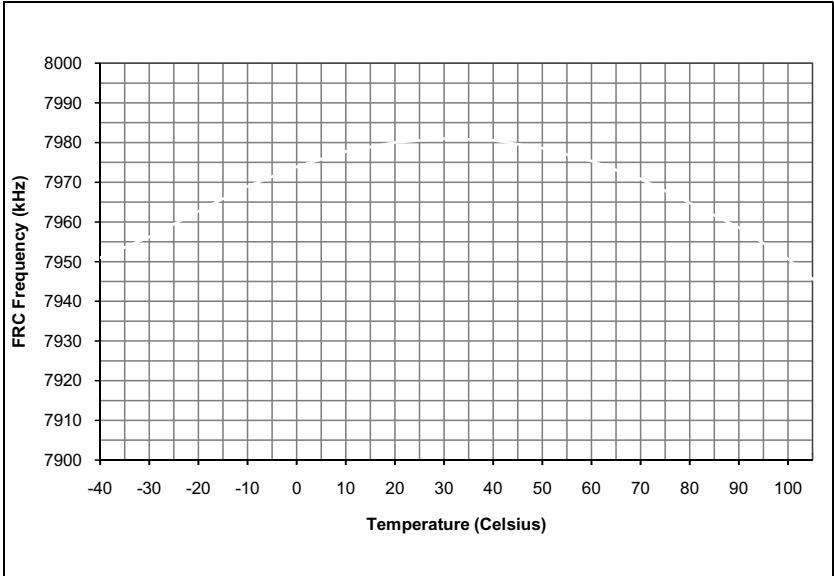


FIGURE 32-7: TYPICAL LPRC FREQUENCY @ V<sub>DD</sub> = 3.3V

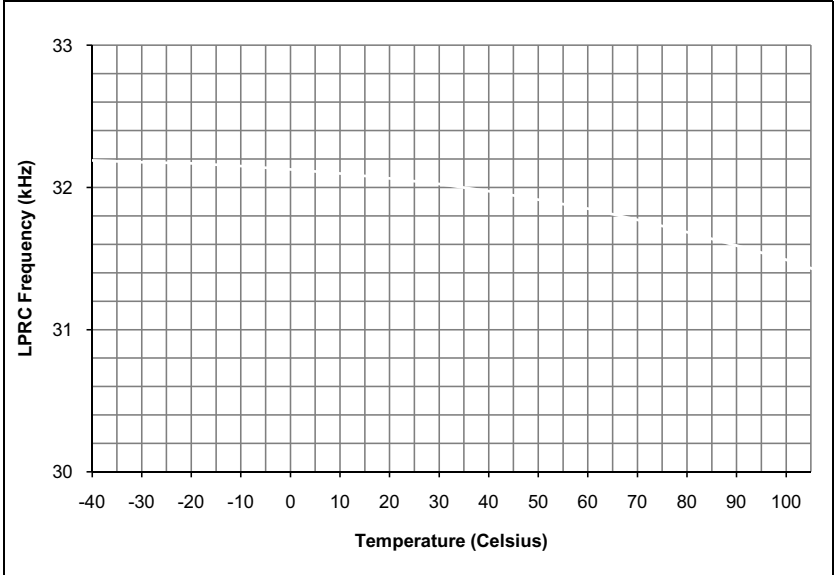
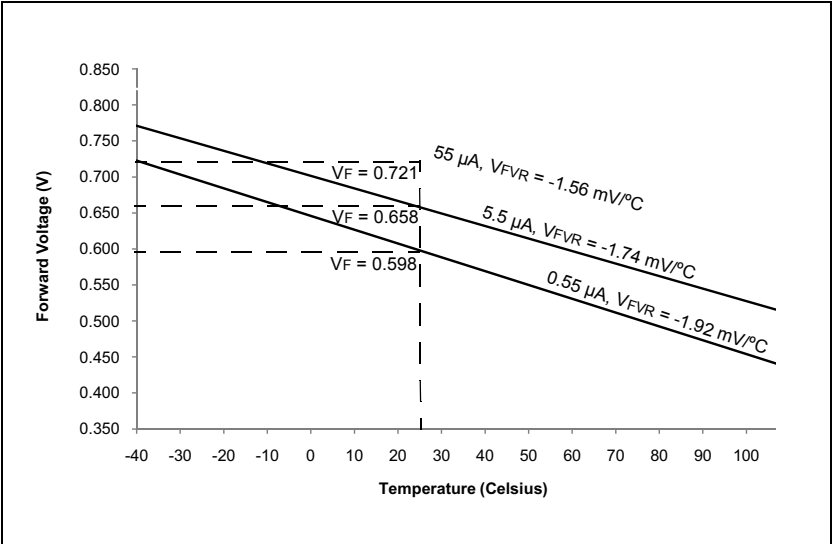


FIGURE 32-8: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE





# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 33.1 Package Marking Information (Continued)

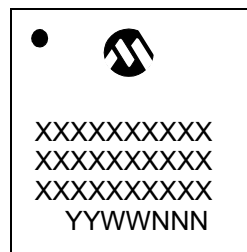
36-Lead VTLA



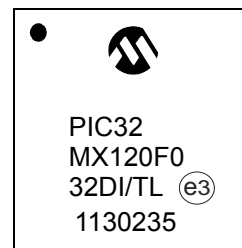
Example



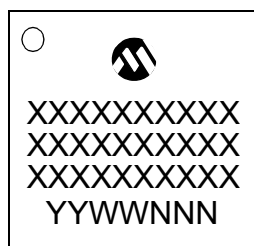
44-Lead VTLA



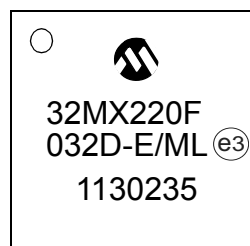
Example



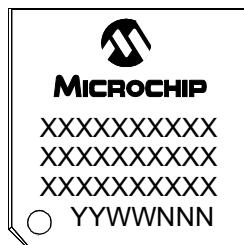
44-Lead QFN



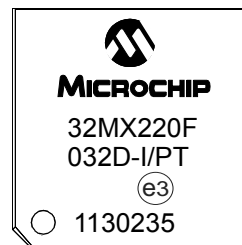
Example



44-Lead TQFP



Example

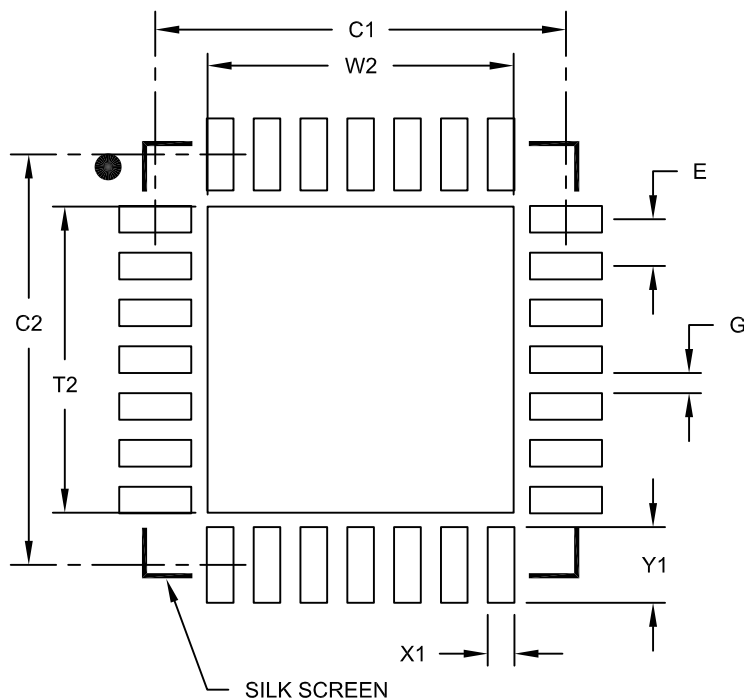


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	<sup>(e3)</sup>	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( <sup>(e3)</sup> ) can be found on the outer packaging for this package.
<b>Note:</b> If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.		

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

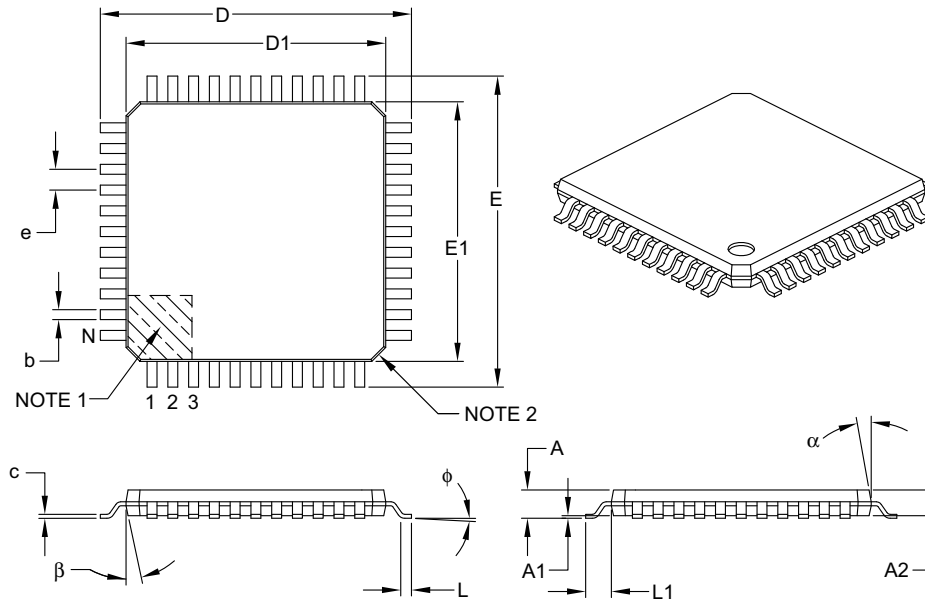
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		44		
Lead Pitch	e		0.80 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	$\phi$		0°	3.5°	7°
Overall Width	E		12.00 BSC		
Overall Length	D		12.00 BSC		
Molded Package Width	E1		10.00 BSC		
Molded Package Length	D1		10.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.30	0.37	0.45
Mold Draft Angle Top	$\alpha$		11°	12°	13°
Mold Draft Angle Bottom	$\beta$		11°	12°	13°

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## Revision F (February 2014)

This revision includes the addition of the following devices:

- PIC32MX170F256B
- PIC32MX270F256B
- PIC32MX170F256D
- PIC32MX270F256D

In addition, this revision includes the following major changes as described in Table A-5, as well as minor updates to text and formatting, which were incorporated throughout the document.

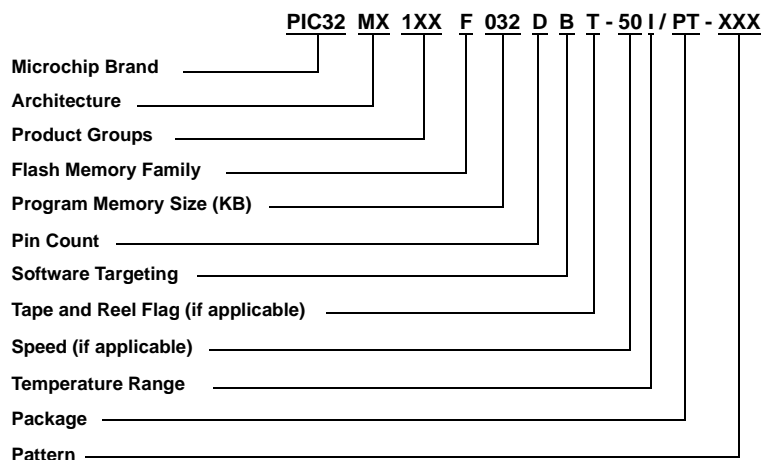
**TABLE A-5: MAJOR SECTION UPDATES**

Section	Update Description
<b>32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog</b>	Added new devices to the family features (see Table 1 and Table 2). Updated pin diagrams to include new devices (see “Pin Diagrams”).
<b>1.0 “Device Overview”</b>	Added Note 3 reference to the following pin names: VBUS, VUSB3V3, VBUSON, D+, D-, and USBID.
<b>2.0 “Guidelines for Getting Started with 32-bit MCUs”</b>	Replaced Figure 2-1: Recommended Minimum Connection. Updated Figure 2-2: MCLR Pin Connections. Added <b>2.9 “Sosc Design Recommendation”</b> .
<b>4.0 “Memory Organization”</b>	Added memory tables for devices with 64 KB RAM (see Table 4-4 through Table 4-5). Changed the Virtual Addresses for all registers and updated the PWP bits in the DEVCFG: Device Configuration Word Summary (see Table 4-17). Updated the ODCA, ODCB, and ODCC port registers (see Table 4-19, Table 4-20, and Table 4-21). The RTCTIME, RTCDATE, ALRMTIME, and ALRMDATE registers were updated (see Table 4-25). Added Data Ram Size value for 64 KB RAM devices (see Register 4-5). Added Program Flash Size value for 256 KB Flash devices (see Register 4-5).
<b>12.0 “Timer1”</b>	The Timer1 block diagram was updated to include the 16-bit data bus (see Figure 12-1).
<b>13.0 “Timer2/3, Timer4/5”</b>	The Timer2-Timer5 block diagram (16-bit) was updated to include the 16-bit data bus (see Figure 13-1). The Timer2/3, Timer4/5 block diagram (32-bit) was updated to include the 32-bit data bus (see Figure 13-1).
<b>19.0 “Parallel Master Port (PMP)”</b>	The CSF<1:0> bit value definitions for ‘00’ and ‘01’ were updated (see Register 19-1). Bit 14 in the Parallel Port Address register (PMADDR) was updated (see Register 19-3).
<b>20.0 “Real-Time Clock and Calendar (RTCC)”</b>	The following registers were updated: RTCTIME (see Register 20-3) RTCDATE (see Register 20-4) ALRMTIME (see Register 20-5) ALRMDATE (see Register 20-6)
<b>26.0 “Special Features”</b>	Updated the PWP bits (see Register 26-1).
<b>29.0 “Electrical Characteristics”</b>	Added parameters DO50 and DO50a to the Capacitive Loading Requirements on Output Pins (see Table 29-14). Added Note 5 to the IDD DC Characteristics (see Table 29-5). Added Note 4 to the IDLE DC Characteristics (see Table 29-6). Added Note 5 to the IPD DC Characteristics (see Table 29-7). Updated the conditions for parameters USB321 (VOL) and USB322 (VOH) in the OTG Electrical Specifications (see Table 29-38).
<b>Product Identification System</b>	Added 40 MHz speed information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



### Example:

PIC32MX110F032DT-I/PT:  
General purpose PIC32,  
32-bit RISC MCU with M4K® core,  
32 KB program memory, 44-pin,  
Industrial temperature,  
TQFP package.

### Flash Memory Family

Architecture	MX = M4K® MCU core
Product Groups	1XX = General purpose microcontroller family 2XX = General purpose microcontroller family
Flash Memory Family	F = Flash program memory
Program Memory Size	016 = 16K 032 = 32K 064 = 64K 128 = 128K 256 = 256K
Pin Count	B = 28-pin C = 36-pin D = 44-pin
Software Targeting	B = Targeted for Bluetooth® Audio Break-in devices
Speed	( ) = 40 MHz – ( ) indicates a blank field; package markings for 40 MHz devices do not include the Speed 50 = 50 MHz
Temperature Range	I = -40°C to +85°C (Industrial) V = -40°C to +105°C (V-temp)
Package	ML = 28-Lead (6x6 mm) QFN (Plastic Quad Flatpack) ML = 44-Lead (8x8 mm) QFN (Plastic Quad Flatpack) PT = 44-Lead (10x10x1 mm) TQFP (Plastic Thin Quad Flatpack) SO = 28-Lead (7.50 mm) SOIC (Plastic Small Outline) SP = 28-Lead (300 mil) SPDIP (Skinny Plastic Dual In-line) SS = 28-Lead (5.30 mm) SSOP (Plastic Shrink Small Outline) TL = 36-Lead (5x5 mm) VTLA (Very Thin Leadless Array) TL = 44-Lead (6x6 mm) VTLA (Very Thin Leadless Array)
Pattern	Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise) ES = Engineering Sample