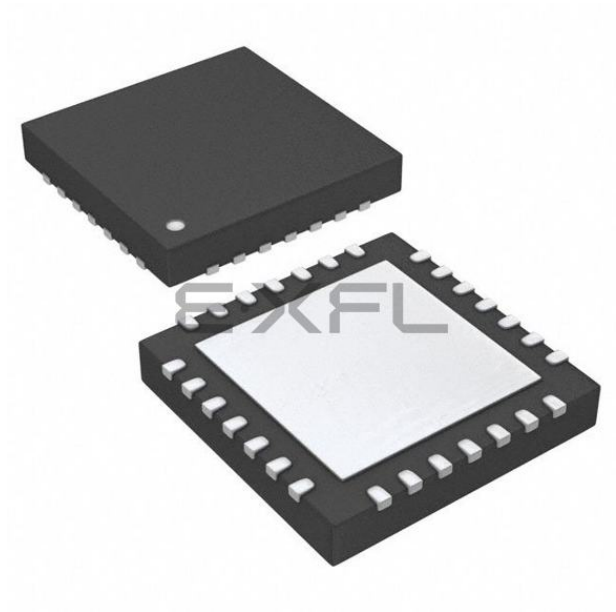
# Microchip Technology - PIC32MX130F256BT-50I/ML Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f256bt-50i-ml |

**TABLE 7: PIN NAMES FOR 36-PIN GENERAL PURPOSE DEVICES**

**36-PIN VTLA (TOP VIEW)(1,2,3,5)**

**PIC32MX110F016C**
**PIC32MX120F032C**
**PIC32MX130F064C**
**PIC32MX150F128C**

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| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2 | 19 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 | 20 | RPC9/CTED7/RC9 |
| 3 | PGED4(4)/AN6/RPC0/RC0 | 21 | VSS |
| 4 | PGEC4(4)/AN7/RPC1/RC1 | 22 | VCAP |
| 5 | VDD | 23 | VDD |
| 6 | VSS | 24 | PGED2/RPB10/CTED11/PMD2/RB10 |
| 7 | OSC1/CLKI/RPA2/RA2 | 25 | PGEC2/TMS/RPB11/PMD1/RB11 |
| 8 | OSC2/CLKO/RPA3/PMA0/RA3 | 26 | AN12/PMD0/RB12 |
| 9 | SOSCI/RPB4/RB4 | 27 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 10 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 28 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14 |
| 11 | RPC3/RC3 | 29 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 12 | VSS | 30 | AVSS |
| 13 | VDD | 31 | AVDD |
| 14 | VDD | 32 | $\overline{\text{MCLR}}$ |
| 15 | PGED3/RPB5/PMD7/RB5 | 33 | VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0 |
| 16 | PGEC3/RPB6/PMD6/RB6 | 34 | VREF-/CVREF-/AN1/RPA1/CTED2/RA1 |
| 17 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 35 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0 |
| 18 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 36 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.
**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
**4:** This pin function is not available on PIC32MX110F016C and PIC32MX120F032C devices.
**5:** Shaded pins are 5V tolerant.

## Table of Contents

## 1.0 DEVICE OVERVIEW

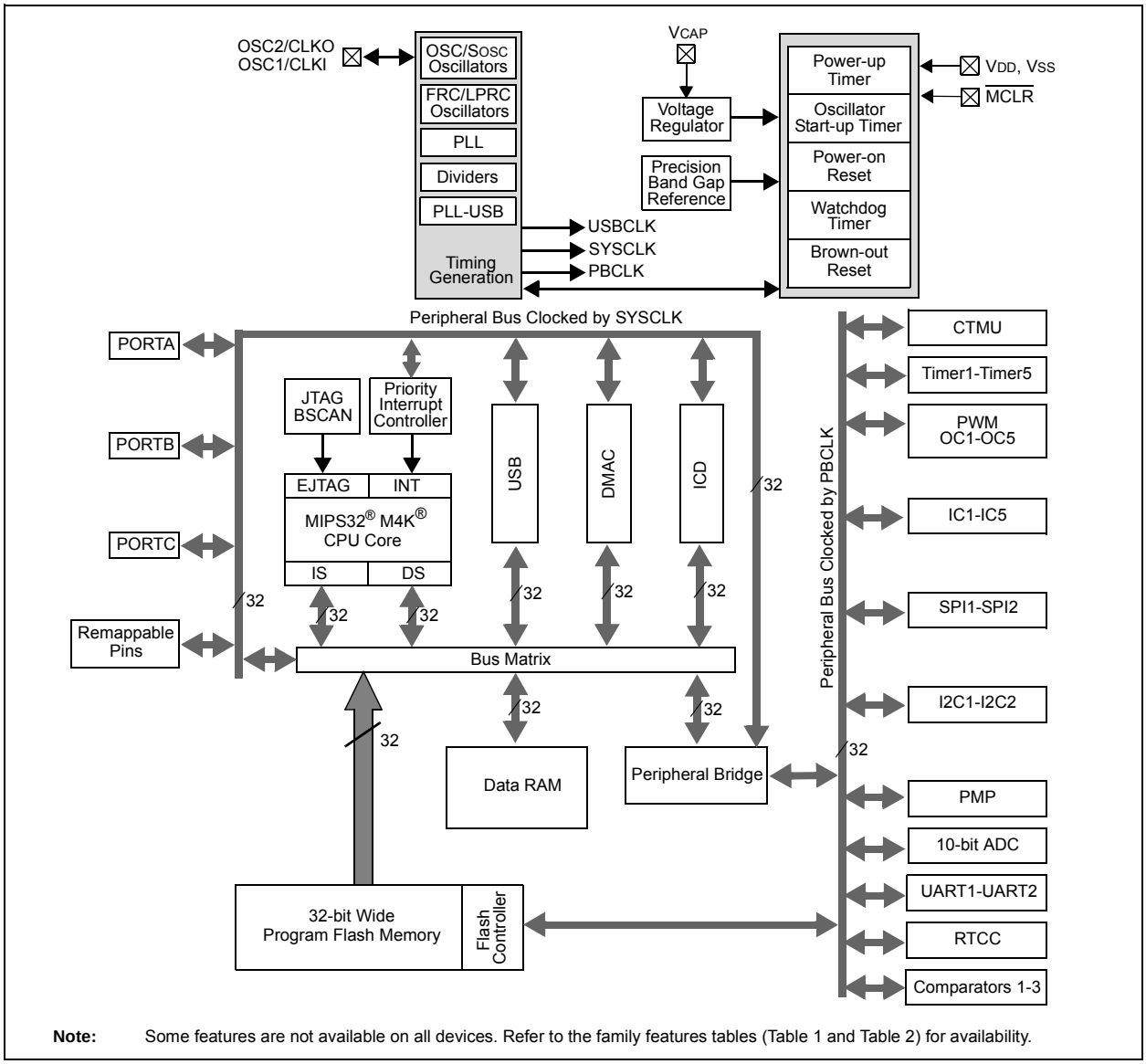
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

This document contains device-specific information for PIC32MX1XX/2XX 28/36/44-pin Family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MX1XX/2XX 28/36/44-pin Family of devices.

Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: BLOCK DIAGRAM**




**Note:** Some features are not available on all devices. Refer to the family features tables (Table 1 and Table 2) for availability.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number[1] | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| SDA1 | 15 | 18 | 19 | 1 | I/O | ST | Synchronous serial data input/output for I2C1 |
| SCL2 | 4 | 7 | 2 | 24 | I/O | ST | Synchronous serial clock input/output for I2C2 |
| SDA2 | 3 | 6 | 1 | 23 | I/O | ST | Synchronous serial data input/output for I2C2 |
| TMS | 19[2]<br>11[3] | 22[2]<br>14[3] | 25[2]<br>15[3] | 12 | I | ST | JTAG Test mode select pin |
| TCK | 14 | 17 | 18 | 13 | I | ST | JTAG test clock input pin |
| TDI | 13 | 16 | 17 | 35 | O | — | JTAG test data input pin |
| TDO | 15 | 18 | 19 | 32 | O | — | JTAG test data output pin |
| RTCC | 4 | 7 | 2 | 24 | O | ST | Real-Time Clock alarm output |
| CVREF- | 28 | 3 | 34 | 20 | I | Analog | Comparator Voltage Reference (low) |
| CVREF+ | 27 | 2 | 33 | 19 | I | Analog | Comparator Voltage Reference (high) |
| CVREFOUT | 22 | 25 | 28 | 14 | O | Analog | Comparator Voltage Reference output |
| C1INA | 4 | 7 | 2 | 24 | I | Analog | Comparator Inputs |
| C1INB | 3 | 6 | 1 | 23 | I | Analog | |
| C1INC | 2 | 5 | 36 | 22 | I | Analog | |
| C1IND | 1 | 4 | 35 | 21 | I | Analog | |
| C2INA | 2 | 5 | 36 | 22 | I | Analog | |
| C2INB | 1 | 4 | 35 | 21 | I | Analog | |
| C2INC | 4 | 7 | 2 | 24 | I | Analog | |
| C2IND | 3 | 6 | 1 | 23 | I | Analog | |
| C3INA | 23 | 26 | 29 | 15 | I | Analog | |
| C3INB | 22 | 25 | 28 | 14 | I | Analog | |
| C3INC | 27 | 2 | 33 | 19 | I | Analog | |
| C3IND | 1 | 4 | 35 | 21 | I | Analog | |
| C1OUT | PPS | PPS | PPS | PPS | O | — | Comparator Outputs |
| C2OUT | PPS | PPS | PPS | PPS | O | — | |
| C3OUT | PPS | PPS | PPS | PPS | O | — | |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

## 4.2 Bus Matrix Control Registers

**TABLE 4-2: BUS MATRIX REGISTER MAP**

| Virtual Address (BF88_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 2000 | BMXCON(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | BMXERRIXI | BMXERRICD | BMXERRDMA | BMXERRDS | BMXERRIS | 001F |
| | | 15:0 | — | — | — | — | — | — | — | — | — | BMXWSDRM | — | — | — | BMXARB<2:0> | | | 0041 |
| 2010 | BMXDKPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDKPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2020 | BMXDUDBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUDBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2030 | BMXDUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | BMXDUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2040 | BMXDRMSZ | 31:16 | BMXDRMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2050 | BMXPUPBA(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | BMXPUPBA<19:16> | | | | 0000 |
| | | 15:0 | BMXPUPBA<15:0> | | | | | | | | | | | | | | | | 0000 |
| 2060 | BMXPFMSZ | 31:16 | BMXPFMSZ<31:0> | | | | | | | | | | | | | | | | xxxx |
| | | 15:0 | | | | | | | | | | | | | | | | | xxxx |
| 2070 | BMXBOOTSZ | 31:16 | BMXBOOTSZ<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0C00 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<31:24> | | | | | | | |
| 23:16 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<23:16> | | | | | | | |
| 15:8 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<15:8> | | | | | | | |
| 7:0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| | NVMKEY<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMKEY<31:0>:** Unlock Register bits
These bits are write-only, and read as '0' on any read

**Note:** This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

**REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<31:24> | | | | | | | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<23:16> | | | | | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<15:8> | | | | | | | |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | NVMADDR<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **NVMADDR<31:0>:** Flash Address bits
Bulk/Chip/PFM Erase: Address is ignored.
Page Erase: Address identifies the page to erase.
Row Program: Address identifies the row to program.
Word Program: Address identifies the word to program.

**REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP03<2:0> | | | IS03<1:0> | |
| 23:16 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP02<2:0> | | | IS02<1:0> | |
| 15:8 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP01<2:0> | | | IS01<1:0> | |
| 7:0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | IP00<2:0> | | | IS00<1:0> | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-29 **Unimplemented:** Read as '0'

bit 28-26 **IP03<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 25-24 **IS03<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 23-21 **Unimplemented:** Read as '0'

bit 20-18 **IP02<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

bit 17-16 **IS02<1:0>:** Interrupt Subpriority bits
- 11 = Interrupt subpriority is 3
- 10 = Interrupt subpriority is 2
- 01 = Interrupt subpriority is 1
- 00 = Interrupt subpriority is 0

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **IP01<2:0>:** Interrupt Priority bits
- 111 = Interrupt priority is 7
- •
- •
- •
- 010 = Interrupt priority is 2
- 001 = Interrupt priority is 1
- 000 = Interrupt is disabled

**Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

## 9.1 DMA Control Registers

**TABLE 9-1: DMA GLOBAL REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3000 | DMACON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | — | SUSPEND | DMABUSY | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| 3010 | DMASTAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RDWR | DMACH<2:0>(2) | | | 0000 |
| 3020 | DMAADDR | 31:16 | DMAADDR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**TABLE 9-2: DMA CRC REGISTER MAP**

| Virtual Address (BF88_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 3030 | DCRCCON | 31:16 | — | — | BYTO<1:0> | | WBO | — | — | BITO | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | PLEN<4:0> | | | | | CRCEN | CRCAPP | CRCTYP | — | — | CRCCH<2:0> | | | 0000 |
| 3040 | DCRCDATA | 31:16 | DCRCDATA<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |
| 3050 | DCRCXOR | 31:16 | DCRCXOR<31:0> | | | | | | | | | | | | | | | | 0000 |
| | | 15:0 | | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**REGISTER 9-7: DCHxCON: DMA CHANNEL 'x' CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
| | CHBUSY | — | — | — | — | — | — | CHCHNS(1) |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R-0 | R/W-0 | R/W-0 |
| | CHEN(2) | CHAED | CHCHN | CHAEN | — | CHEDET | CHPRI<1:0> | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **CHBUSY:** Channel Busy bit
- 1 = Channel is active or has been enabled
- 0 = Channel is inactive or has been disabled

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **CHCHNS:** Chain Channel Selection bit(1)
- 1 = Chain to channel lower in natural priority (CH1 will be enabled by CH2 transfer complete)
- 0 = Chain to channel higher in natural priority (CH1 will be enabled by CH0 transfer complete)

bit 7 **CHEN:** Channel Enable bit(2)
- 1 = Channel is enabled
- 0 = Channel is disabled

bit 6 **CHAED:** Channel Allow Events If Disabled bit
- 1 = Channel start/abort events will be registered, even if the channel is disabled
- 0 = Channel start/abort events will be ignored if the channel is disabled

bit **CHCHN:** Channel Chain Enable bit
- 1 = Allow channel to be chained
- 0 = Do not allow channel to be chained

bit 4 **CHAEN:** Channel Automatic Enable bit
- 1 = Channel is continuously enabled, and not automatically disabled after a block transfer is complete
- 0 = Channel is disabled on block transfer complete

bit 3 **Unimplemented:** Read as '0'

bit 2 **CHEDET:** Channel Event Detected bit
- 1 = An event has been detected
- 0 = No events have been detected

bit 1-0 **CHPRI<1:0>:** Channel Priority bits
- 11 = Channel has priority 3 (highest)
- 10 = Channel has priority 2
- 01 = Channel has priority 1
- 00 = Channel has priority 0

**Note 1:** The chain selection bit takes effect when chaining is enabled (i.e., CHCHN = 1).

**2:** When the channel is suspended by clearing this bit, the user application should poll the CHBUSY bit (if available on the device variant) to see when the channel is suspended, as it may take some clock cycles to complete a current transaction before the channel is suspended.

**REGISTER 9-18: DCHxDAT: DMA CHANNEL 'x' PATTERN DATA REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CHPDAT<7:0> | | | | | | | |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CHPDAT<7:0>:** Channel Data Register bits

Pattern Terminate mode:
Data to be matched must be stored in this register to allow a "terminate on match".

All other modes:
Unused.

**TABLE 11-2: OUTPUT PIN SELECTION**

| RPn Port Pin | RPnR SFR | RPnR bits | RPnR Value to Peripheral Selection |
|---|---|---|---|
| RPA0 | RPA0R | RPA0R<3:0> | 0000 = No Connect<br>0001 = U1TX<br>0010 = U2RTS<br>0011 = SS1<br>0100 = Reserved<br>0101 = OC1<br>0110 = Reserved<br>0111 = C2OUT<br>1000 = Reserved<br>.<br>.<br>.<br>1111 = Reserved |
| RPB3 | RPB3R | RPB3R<3:0> | |
| RPB4 | RPB4R | RPB4R<3:0> | |
| RPB15 | RPB15R | RPB15R<3:0> | |
| RPB7 | RPB7R | RPB7R<3:0> | |
| RPC7 | RPC7R | RPC7R<3:0> | |
| RPC0 | RPC0R | RPC0R<3:0> | |
| RPC5 | RPC5R | RPC5R<3:0> | |
| RPA1 | RPA1R | RPA1R<3:0> | 0000 = No Connect<br>0001 = Reserved<br>0010 = Reserved<br>0011 = SDO1<br>0100 = SDO2<br>0101 = OC2<br>0110 = Reserved<br>0111 = C3OUT<br>.<br>.<br>.<br>1111 = Reserved |
| RPB5 | RPB5R | RPB5R<3:0> | |
| RPB1 | RPB1R | RPB1R<3:0> | |
| RPB11 | RPB11R | RPB11R<3:0> | |
| RPB8 | RPB8R | RPB8R<3:0> | |
| RPA8 | RPA8R | RPA8R<3:0> | |
| RPC8 | RPC8R | RPC8R<3:0> | |
| RPA9 | RPA9R | RPA9R<3:0> | |
| RPA2 | RPA2R | RPA2R<3:0> | 0000 = No Connect<br>0001 = Reserved<br>0010 = Reserved<br>0011 = SDO1<br>0100 = SDO2<br>0101 = OC4<br>0110 = OC5<br>0111 = REFCLKO<br>1000 = Reserved<br>.<br>.<br>.<br>1111 = Reserved |
| RPB6 | RPB6R | RPB6R<3:0> | |
| RPA4 | RPA4R | RPA4R<3:0> | |
| RPB13 | RPB13R | RPB13R<3:0> | |
| RPB2 | RPB2R | RPB2R<3:0> | |
| RPC6 | RPC6R | RPC6R<3:0> | |
| RPC1 | RPC1R | RPC1R<3:0> | |
| RPC3 | RPC3R | RPC3R<3:0> | |
| RPA3 | RPA3R | RPA3R<3:0> | 0000 = No Connect<br>0001 = U1RTS<br>0010 = U2TX<br>0011 = Reserved<br>0100 = SS2<br>0101 = OC3<br>0110 = Reserved<br>0111 = C1OUT<br>1000 = Reserved<br>.<br>.<br>.<br>1111 = Reserved |
| RPB14 | RPB14R | RPB14R<3:0> | |
| RPB0 | RPB0R | RPB0R<3:0> | |
| RPB10 | RPB10R | RPB10R<3:0> | |
| RPB9 | RPB9R | RPB9R<3:0> | |
| RPC9 | RPC9R | RPC9R<3:0> | |
| RPC2 | RPC2R | RPC2R<3:0> | |
| RPC4 | RPC4R | RPC4R<3:0> | |

**REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER**

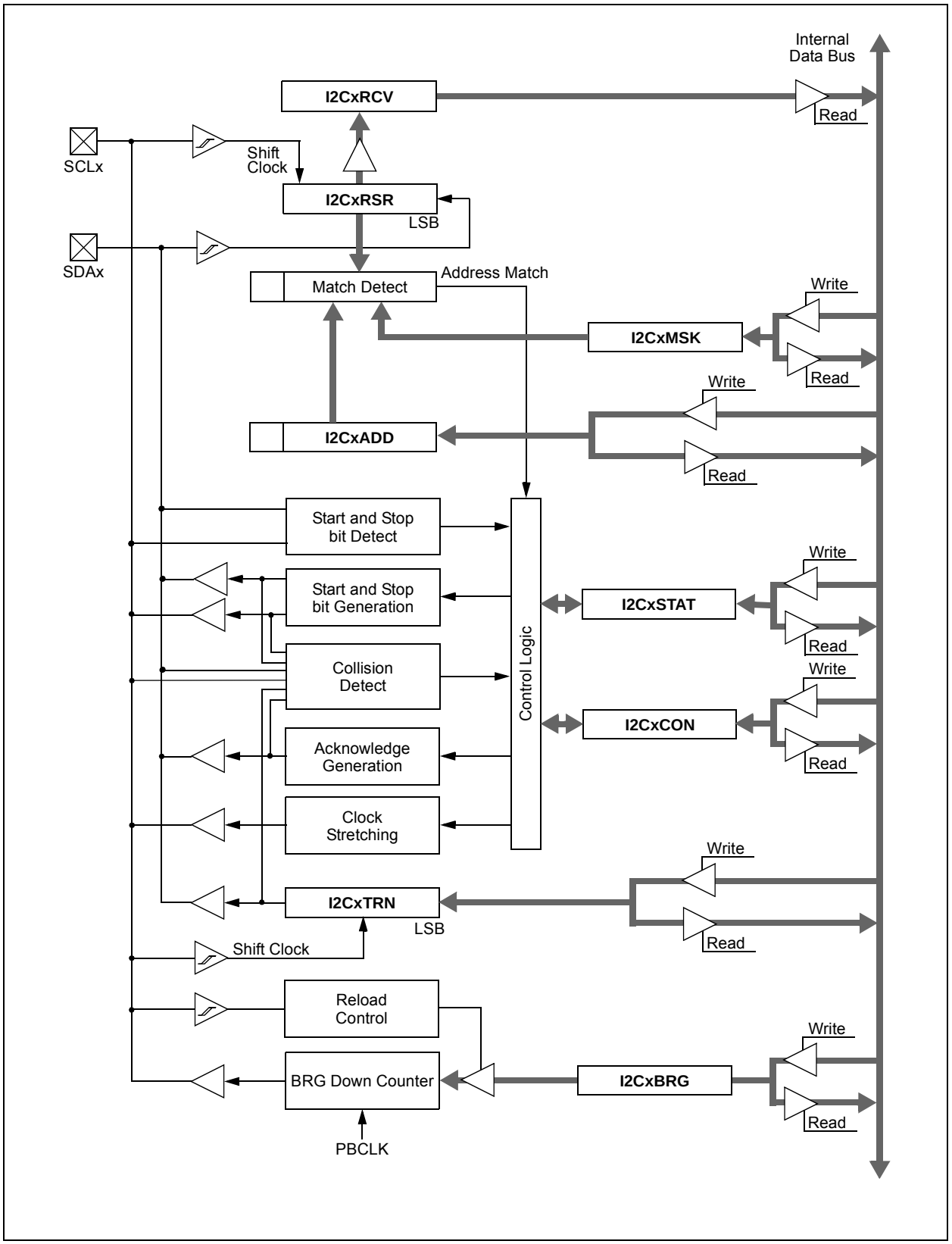
bit 3 **SPITBE:** SPI Transmit Buffer Empty Status bit
1 = Transmit buffer, SPIxTXB is empty
0 = Transmit buffer, SPIxTXB is not empty
Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR.
Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPI Transmit Buffer Full Status bit
1 = Transmit not yet started, SPITXB is full
0 = Transmit buffer is not full
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB.
Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR.
Enhanced Buffer Mode:
Set when CWPTR + 1 = SRPTR; cleared otherwise

bit 0 **SPIRBF:** SPI Receive Buffer Full Status bit
1 = Receive buffer, SPIxRXB is full
0 = Receive buffer, SPIxRXB is not full
Standard Buffer Mode:
Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB.
Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer Mode:
Set when SWPTR + 1 = CRPTR; cleared otherwise

**FIGURE 18-1: I²C BLOCK DIAGRAM**



**NOTES:**

**REGISTER 27-4: DEVCFG3: DEVICE CONFIGURATION WORD 3**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R/P | R/P | R/P | R/P | r-1 | r-1 | r-1 | r-1 |
| | FVBUSONIO | FUSBIDIO | IOL1WAY | PMDL1WAY | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 15:8 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<15:8> | | | | | | | |
| 7:0 | R/P | R/P | R/P | R/P | R/P | R/P | R/P | R/P |
| | USERID<7:0> | | | | | | | |

| **Legend:** | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31 **FVBUSONIO:** USB VBUSON Selection bit
1 = VBUSON pin is controlled by the USB module
0 = VBUSON pin is controlled by the port function

bit 30 **FUSBIDIO:** USB USBID Selection bit
1 = USBID pin is controlled by the USB module
0 = USBID pin is controlled by the port function

bit 29 **IOL1WAY:** Peripheral Pin Select Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 28 **PMDI1WAY:** Peripheral Module Disable Configuration bit
1 = Allow only one reconfiguration
0 = Allow multiple reconfigurations

bit 27-16 **Reserved:** Write '1'

bit 15-0 **USERID<15:0>:** User ID bits
This is a 16-bit value that is user-defined and is readable via ICSP™ and JTAG.

## 29.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

**TABLE 30-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE): Core Off, Clock on Base Current (Notes 1, 4)** | | | | | | |
| DC30a | 1 | 1.5 | mA | 4 MHz **(Note 3)** | | |
| DC31a | 2 | 3 | mA | 10 MHz | | |
| DC32a | 4 | 6 | mA | 20 MHz **(Note 3)** | | |
| DC33a | 5.5 | 8 | mA | 30 MHz **(Note 3)** | | |
| DC34a | 7.5 | 11 | mA | 40 MHz | | |
| DC37a | 100 | — | µA | -40°C | 3.3V | LPRC (31 kHz) **(Note 3)** |
| DC37b | 250 | — | µA | +25°C | | |
| DC37c | 380 | — | µA | +85°C | | |

**Note 1:** The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode (CPU core Halted), and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** This parameter is characterized, but not tested in manufacturing.

**4:** IIDLE electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

**TABLE 30-7: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | |
|---|---|---|---|---|---|
| **Param. No.** | **Typical(2)** | **Max.** | **Units** | **Conditions** | |
| **Power-Down Current ($I_{PD}$) (Notes 1, 5)** | | | | | |
| DC40k | 44 | 70 | μA | -40°C | Base Power-Down Current |
| DC40l | 44 | 70 | μA | +25°C | |
| DC40n | 168 | 259 | μA | +85°C | |
| DC40m | 335 | 536 | μA | +105ºC | |
| **Module Differential Current** | | | | | |
| DC41e | 5 | 20 | μA | 3.6V | Watchdog Timer Current: $\Delta I_{WDT}$ **(Note 3)** |
| DC42e | 23 | 50 | μA | 3.6V | RTCC + Timer1 w/32 kHz Crystal: $\Delta I_{RTCC}$ **(Note 3)** |
| DC43d | 1000 | 1100 | μA | 3.6V | ADC: $\Delta I_{ADC}$ **(Notes 3,4)** |

**Note 1:** The test conditions for $I_{PD}$ current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is set
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to $V_{SS}$
- $\overline{MCLR}$ = $V_{DD}$
- RTCC and JTAG are disabled

**2:** Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

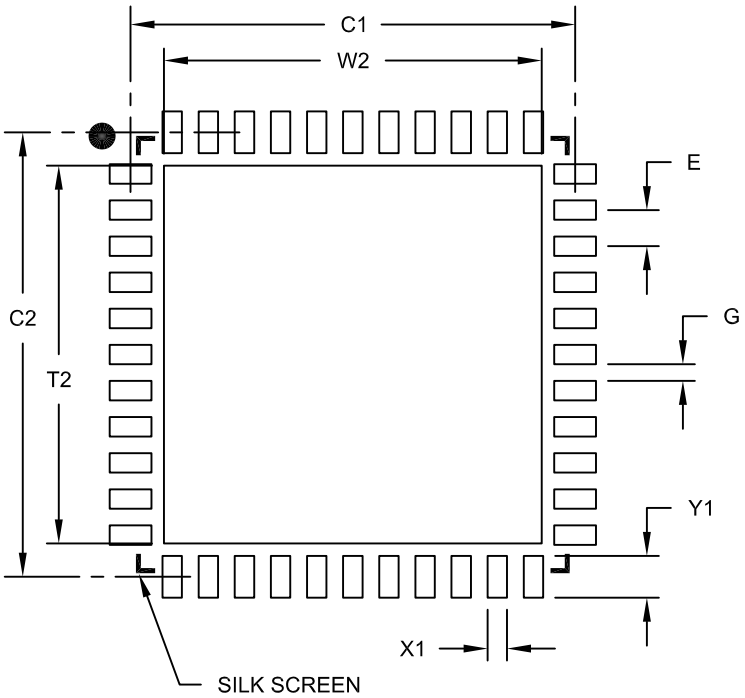
**3:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base $I_{PD}$ current.

**4:** Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

**5:** $I_{PD}$ electrical characteristics for devices with 256 KB Flash are only provided as Preliminary information.

### 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Optional Center Pad Width | W2 | | | 6.80 |
| Optional Center Pad Length | T2 | | | 6.80 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (X44) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.25 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section | Update Description |
|---|---|
| **29.0 "Electrical Characteristics"** | Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to VSS).<br>Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2).<br>Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5).<br>Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6).<br>Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7).<br>Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13).<br>Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17).<br>Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20).<br>Updated all parameters in the CTMU Specifications (see Table 29-39). |
| **31.0 "Packaging Information"** | Added the 28-lead SPDIP package diagram information (see **31.1 "Package Marking Information"** and **31.2 "Package Details"**). |
| **"**Product Identification System**"** | Added the SPDIP (SP) package definition. |

## Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

**TABLE A-2: MAJOR SECTION UPDATES**

| Section | Update Description |
|---|---|
| **"**32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog**"** | Revised the source/sink on I/O pins (see **"Input/Output"** on page 1).<br>Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2). |
| **4.0 "Memory Organization"** | Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20). |
| **29.0 "Electrical Characteristics"** | Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16). |