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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f256bt-v-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

TABLE 4:PIN NAMES FOR 28-PIN USB DEVICES

28	PIN SOIC, SPDIP, SSOP (TOP VIEW) ^(1,2,3)					
	1 SSOP	28	1 SOIC	28	1	28 SPDIP
	PIC32MX210F016B PIC32MX220F032B PIC32MX230F064B PIC32MX230F256B PIC32MX250F128B PIC32MX270F256B					
Pin #	Full Pin Name	Pin #		Full Pin N	Name	
Pin #	Full Pin Name	Pin #	VBUS	Full Pin N	Name	
Pin # 1 2	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	Pin # 15 16	VBUS TDI/RPB7/CTED3/PM	Full Pin N	Name	
Pin # 1 2 3	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	Pin # 15 16 17	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE	Full Pin N D5/INT0/RE	Name 37 /RB8	
Pin # 1 2 3 4	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	Pin # 15 16 17 18	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	Pin # 15 16 17 18 19	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5 6	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	Pin # 15 16 17 18 19 20	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5 6 7	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	Pin # 15 16 17 18 19 20 21	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I FED11/RB10	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INB/C3IND/RPB0/PMD0/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss	Pin # 15 16 17 18 19 20 21 21 22	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I FED11/RB10 11	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8 9	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2	Pin # 15 16 17 18 19 20 21 22 23	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I FED11/RB10 11	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8 9 10	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3	Pin # 15 16 17 18 19 20 21 22 23 24	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/F	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I TED11/RB10 11 PMRD/RB13	Name 37 /RB8 RB9 0 3	
Pin # 1 2 3 4 5 6 7 8 9 10 11	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4	Pin # 15 16 17 18 19 20 21 22 23 24 25	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/I CVREFOUT/AN10/C3IN	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I FED11/RB10 11 IB/RPB14/V	Name 37 /RB8 RB9 0 3 /BUSON/S	SCK1/CTED5/RB14
Pin # 1 2 3 4 5 6 7 8 9 10 11 12	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INB/C3IND/RPB0/PMD0/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	Pin # 15 16 17 18 19 20 21 22 23 24 25 26	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/f CVREFOUT/AN10/C3IN AN9/C3INA/RPB15/SC	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I TED11/RB10 11 PMRD/RB11 IB/RPB14/V CK2/CTED6	Name 37 /RB8 RB9 0 0 3 /BUSON/S 5/PMCS1	SCK1/CTED5/RB14 1/RB15
Pin # 1 2 3 4 5 6 7 8 9 10 11 12 13	Full Pin Name MCLR PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 Vss OSC1/CLKI/RPA2/RA2 OSC2/CLKO/RPA3/PMA0/RA3 SOSCI/RPB4/RB4 SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 VpD	Pin # 15 16 17 18 19 20 21 22 23 24 25 26 27	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/F CVREFOUT/AN10/C3IN AN9/C3INA/RPB15/SC AVSS	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I TED11/RB10 11 PMRD/RB13 IB/RPB14/V CK2/CTED6	Name 37 /RB8 RB9 0 0 3 /BUSON/S 6)/PMCS1	SCK1/CTED5/RB14 1/RB15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB[®] ICD 3 or MPLAB REAL ICETM.

For more information on ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

- "Using MPLAB[®] ICD 3" (poster) (DS50001765)
- *"MPLAB[®] ICD 3 Design Advisory"* (DS50001764)
- "MPLAB[®] REAL ICE™ In-Circuit Debugger User's Guide" (DS50001616)
- "Using MPLAB[®] REAL ICE™ Emulator" (poster) (DS50001749)

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector and the JTAG pins on the device as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (VIH) and input low (VIL) requirements.

2.7 External Oscillator Pins

Many MCUs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 8.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-3.

FIGURE 2-3: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

Unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic-low state.

Alternatively, inputs can be reserved by connecting the pin to Vss through a 1k to 10k resistor and configuring the pin as an input.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	_	—	_		_	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
45.0	R/W-0	R/W-0	R-0	R-0	R-0	U-0	U-0	U-0
15:8	WR	WREN	WRERR ⁽¹⁾	LVDERR ⁽¹⁾	LVDSTAT ⁽¹⁾	—	_	—
7.0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	_	_		_	NVMOP<3:0>			

REGISTER 5-1: NVMCON: PROGRAMMING CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15	WR: Write Control bit
	This bit is writable when WREN = 1 and the unlock sequence is followed.
	 1 = Initiate a Flash operation. Hardware clears this bit when the operation completes 0 = Flash operation is complete or inactive
bit 14	WREN: Write Enable bit
	This is the only bit in this register reset by a device Reset.
	 1 = Enable writes to WR bit and enables LVD circuit 0 = Disable writes to WR bit and disables LVD circuit
bit 13	WRERR: Write Error bit ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	 1 = Program or erase sequence did not complete successfully 0 = Program or erase sequence completed normally
bit 12	LVDERR: Low-Voltage Detect Error bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set by hardware.
	 1 = Low-voltage detected (possible data corruption, if WRERR is set) 0 = Voltage level is acceptable for programming
bit 11	LVDSTAT: Low-Voltage Detect Status bit (LVD circuit must be enabled) ⁽¹⁾
	This bit is read-only and is automatically set and cleared by the hardware.
	1 = Low-voltage event is active
	0 = Low-voltage event is not active
bit 10-4	Unimplemented: Read as '0'
bit 3-0	NVMOP<3:0>: NVM Operation bits
	These bits are writable when WREN = 0.
	1111 = Reserved
	•
	0111 = Reserved
	0110 = No operation
	 0101 = Program Flash Memory (PFM) erase operation: erases PFM, if all pages are not write-protected 0100 = Page erase operation: erases page selected by NVMADDR, if it is not write-protected 0011 = Row program operation: programs row selected by NVMADDR, if it is not write-protected
	0010 = No operation
	0000 = No operation

Note 1: This bit is cleared by setting NVMOP == `b0000, and initiating a Flash operation (i.e., WR).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IFS31	IFS30	IFS29	IFS28	IFS27	IFS26	IFS25	IFS24
22:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IFS23	IFS22	IFS21	IFS20	IFS19	IFS18	IFS17	IFS16
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15:8	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10	IFS09	IFS08
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00

REGISTER 7-4: IFSx: INTERRUPT FLAG STATUS REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 IFS31-IFS00: Interrupt Flag Status bits

- 1 = Interrupt request has occurred
- 0 = No interrupt request has occurred

Note: This register represents a generic definition of the IFSx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 7-5: IECx: INTERRUPT ENABLE CONTROL REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24
22.16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC09	IEC08
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0	IEC07	IEC06	IEC05	IEC04	IEC03	IEC02	IEC01	IEC00

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 IEC31-IEC00: Interrupt Enable bits

1 = Interrupt is enabled

0 = Interrupt is disabled

Note: This register represents a generic definition of the IECx register. Refer to Table 7-1 for the exact bit definitions.

REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

bit 6 **CRCAPP:** CRC Append Mode bit⁽¹⁾

- 1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA
- 0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5 **CRCTYP:** CRC Type Selection bit
 - 1 = The CRC module will calculate an IP header checksum
 - 0 = The CRC module will calculate a LFSR CRC
- bit 4-3 Unimplemented: Read as '0'
- bit 2-0 CRCCH<2:0>: CRC Channel Select bits
 - 111 = CRC is assigned to Channel 7
 - 110 = CRC is assigned to Channel 6
 - 101 = CRC is assigned to Channel 5
 - 100 = CRC is assigned to Channel 4
 - 011 = CRC is assigned to Channel 3
 - 010 = CRC is assigned to Channel 2
 - 001 = CRC is assigned to Channel 1
 - 000 = CRC is assigned to Channel 0
- **Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

REGISTER 10-7: U1IE: USB INTERRUPT ENABLE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	_	—	_		_	—	_	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	—	—
15.9	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	_	—	_		_	—	_	—
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7:0	STALLIE	ATTACHIE	RESIMEIE		TRNIE	SOFIE		URSTIE ⁽²⁾
	OTALLIL			IDELIE		OOLIE	OLIVIL	DETACHIE ⁽³⁾

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7	STALLIE: STALL	Handshake	Interrupt Enable	bit

- 1 = STALL interrupt is enabled
- 0 = STALL interrupt is disabled
- bit 6 ATTACHIE: ATTACH Interrupt Enable bit
 - 1 = ATTACH interrupt is enabled 0 = ATTACH interrupt is disabled
- bit 5 **RESUMEIE:** RESUME Interrupt Enable bit
 - 1 = RESUME interrupt is enabled
 - 0 = RESUME interrupt is disabled
- bit 4 IDLEIE: Idle Detect Interrupt Enable bit
 - 1 = Idle interrupt is enabled
 - 0 = Idle interrupt is disabled
- bit 3 TRNIE: Token Processing Complete Interrupt Enable bit
 - 1 = TRNIF interrupt is enabled
 - 0 = TRNIF interrupt is disabled
- bit 2 SOFIE: SOF Token Interrupt Enable bit
 - 1 = SOFIF interrupt is enabled
 - 0 = SOFIF interrupt is disabled
- bit 1 **UERRIE:** USB Error Interrupt Enable bit⁽¹⁾
 - 1 = USB Error interrupt is enabled
 - 0 = USB Error interrupt is disabled
- bit 0 URSTIE: USB Reset Interrupt Enable bit⁽²⁾
 - 1 = URSTIF interrupt is enabled
 - 0 = URSTIF interrupt is disabled

DETACHIE: USB Detach Interrupt Enable bit⁽³⁾

- 1 = DATTCHIF interrupt is enabled
- 0 = DATTCHIF interrupt is disabled

Note 1: For an interrupt to propagate USBIF, the UERRIE (U1IE<1>) bit must be set.

- 2: Device mode.
- 3: Host mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	LSPDEN			D	EVADDR<6:0)>		

REGISTER 10-12: U1ADDR: USB ADDRESS REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7 LSPDEN: Low-Speed Enable Indicator bit

1 = Next token command to be executed at Low-Speed

0 = Next token command to be executed at Full-Speed

bit 6-0 **DEVADDR<6:0>:** 7-bit USB Device Address bits

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	—	—	—	—	—	_	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	—	—	—	—	—	_	—
15:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	—	—		—
7:0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
				FRML	<7:0>			

REGISTER 10-13: U1FRML: USB FRAME NUMBER LOW REGISTER

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-8 Unimplemented: Read as '0'

bit 7-0 **FRML<7:0>:** The 11-bit Frame Number Lower bits

The register bits are updated with the current frame number whenever a SOF TOKEN is received.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—			—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	_	—	_	_	_			_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—			—
7:0	U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
						FRMH<2:0>		

REGISTER 10-14: U1FRMH: USB FRAME NUMBER HIGH REGISTER

Legend:

•			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-3 Unimplemented: Read as '0'

bit 2-0 **FRMH<2:0>:** The Upper 3 bits of the Frame Numbers bits The register bits are updated with the current frame number whenever a SOF TOKEN is received.

Bit Bit Bit Bit Bit Bit Bit Bit Bit 30/22/14/6 27/19/11/3 26/18/10/2 25/17/9/1 24/16/8/0 Range 31/23/15/7 29/21/13/5 28/20/12/4 U-0 U-0 U-0 U-0 U-0 U-0 U-0 U-0 31:24 ___ ___ ____ ____ ____ ____ ___ ____ U-0 U-0 U-0 U-0 U-0 U-0 U-0 U-0 23:16 _ ___ ____ ____ ____ ____ ____ ___ U-0 U-0 U-0 U-0 U-0 U-0 U-0 U-0 15:8 _ ___ ____ ____ ____ ___ ____ ____ R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 7:0 PID < 3:0 > (1)EP<3:0>

REGISTER 10-15: U1TOK: USB TOKEN REGISTER

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-4 **PID<3:0>:** Token Type Indicator bits⁽¹⁾

1101 = SETUP (TX) token type transaction

- 1001 = IN (RX) token type transaction
- 0001 = OUT (TX) token type transaction

Note: All other values are reserved and must not be used.

bit 3-0 **EP<3:0>:** Token Command Endpoint Address bits The four bit value must specify a valid endpoint.

Note 1: All other values are reserved and must not be used.

14.0 WATCHDOG TIMER (WDT)

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 9. "Watchdog, Deadman, and Power-up Timers" (DS60001114), which are available from the Documentation > Reference Manual section of the Microchip PIC32 web site (www.microchip.com/pic32). The WDT, when enabled, operates from the internal Low-Power Oscillator (LPRC) clock source and can be used to detect system software malfunctions by resetting the device if the WDT is not cleared periodically in software. Various WDT time-out periods can be selected using the WDT postscaler. The WDT can also be used to wake the device from Sleep or Idle mode.

The following are some of the key features of the WDT module:

- · Configuration or software controlled
- User-configurable time-out period
- Can wake the device from Sleep or Idle mode

Figure 14-1 illustrates a block diagram of the WDT and Power-up timer.

FIGURE 14-1: WATCHDOG TIMER AND POWER-UP TIMER BLOCK DIAGRAM



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
24.24	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0	
31:24	—	—	—	RXBUFELM<4:0>					
00.40	U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0	
23:10	—	—	—	TXBUFELM<4:0>					
45.0	U-0	U-0	U-0	R/C-0, HS	R-0	U-0	U-0	R-0	
15:8	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	
7:0	R-0	R/W-0	R-0	U-0	R-1	U-0	R-0	R-0	
	SRMT	SPIROV	SPIRBE	_	SPITBE	_	SPITBF	SPIRBF	

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

Legend:	C = Clearable bit	HS = Set in hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 31-29 Unimplemented: Read as '0'
- bit 28-24 **RXBUFELM<4:0>:** Receive Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 23-21 Unimplemented: Read as '0'
- bit 20-16 **TXBUFELM<4:0>:** Transmit Buffer Element Count bits (valid only when ENHBUF = 1)
- bit 15-13 Unimplemented: Read as '0'
- bit 12 **FRMERR:** SPI Frame Error status bit
 - 1 = Frame error detected
 - 0 = No Frame error detected
 - This bit is only valid when FRMEN = 1.
- bit 11 SPIBUSY: SPI Activity Status bit
 - 1 = SPI peripheral is currently busy with some transactions
 - 0 = SPI peripheral is currently idle
- bit 10-9 Unimplemented: Read as '0'
- bit 8 SPITUR: Transmit Under Run bit
 - 1 = Transmit buffer has encountered an underrun condition
 - 0 = Transmit buffer has no underrun condition

This bit is only valid in Framed Sync mode; the underrun condition must be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or writing a '0' to SPITUR.

- bit 7 **SRMT:** Shift Register Empty bit (valid only when ENHBUF = 1)
 - 1 = When SPI module shift register is empty
 - 0 = When SPI module shift register is not empty
- bit 6 SPIROV: Receive Overflow Flag bit
 - 1 = A new data is completely received and discarded. The user software has not read the previous data in the SPIxBUF register.
 - 0 = No overflow has occurred

This bit is set in hardware; can bit only be cleared by disabling (ON bit = 0) and re-enabling (ON bit = 1) the module, or by writing a '0' to SPIROV.

- bit 5 **SPIRBE:** RX FIFO Empty bit (valid only when ENHBUF = 1) 1 = RX FIFO is empty (CRPTR = SWPTR)
 - 0 = RX FIFO is not empty (CRPTR \neq SWPTR)
- bit 4 Unimplemented: Read as '0'

REGISTER 17-3: SPIxSTAT: SPI STATUS REGISTER

bit 3 SPITBE: SPI Transmit Buffer Empty Status bit 1 = Transmit buffer, SPIxTXB is empty 0 = Transmit buffer, SPIxTXB is not empty Automatically set in hardware when SPI transfers data from SPIxTXB to SPIxSR. Automatically cleared in hardware when SPIxBUF is written to, loading SPIxTXB. bit 2 Unimplemented: Read as '0' bit 1 SPITBF: SPI Transmit Buffer Full Status bit 1 = Transmit not yet started, SPITXB is full 0 = Transmit buffer is not full Standard Buffer Mode: Automatically set in hardware when the core writes to the SPIBUF location, loading SPITXB. Automatically cleared in hardware when the SPI module transfers data from SPITXB to SPISR. Enhanced Buffer Mode: Set when CWPTR + 1 = SRPTR; cleared otherwise bit 0 SPIRBF: SPI Receive Buffer Full Status bit 1 = Receive buffer, SPIxRXB is full

0 = Receive buffer, SPIxRXB is not full

Standard Buffer Mode:

Automatically set in hardware when the SPI module transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.

Enhanced Buffer Mode:

Set when SWPTR + 1 = CRPTR; cleared otherwise

NOTES:

20.0 PARALLEL MASTER PORT (PMP)

Note:	This data sheet summarizes the features
	of the PIC32MX1XX/2XX 28/36/44-pin
	Family of devices. It is not intended to be
	a comprehensive reference source. To
	complement the information in this data
	sheet, refer to Section 13. "Parallel
	Master Port (PMP)" (DS60001128),
	which is available from the Documentation
	> Reference Manual section of the
	Microchip PIC32 web site
	(www.microchip.com/pic32).

The PMP is a parallel 8-bit input/output module specifically designed to communicate with a wide variety of parallel devices, such as communications peripherals, LCDs, external memory devices and microcontrollers. Because the interface to parallel peripherals varies significantly, the PMP module is highly configurable. Key features of the PMP module include:

- Fully multiplexed address/data mode
- Demultiplexed or partially multiplexed address/ data mode
 - up to 11 address lines with single Chip Select
 - up to 12 address lines without Chip Select
- One Chip Select line
- Programmable strobe options
 - Individual read and write strobes or;
 - Read/write strobe with enable strobe
- · Address auto-increment/auto-decrement
- Programmable address/data multiplexing
- Programmable polarity on control signals
- · Legacy parallel slave port support
- · Enhanced parallel slave support
- Address support
- 4-byte deep auto-incrementing buffer
- Programmable Wait states
- · Selectable input voltage levels

Figure 20-1 illustrates the PMP module block diagram.

FIGURE 20-1: PMP MODULE PINOUT AND CONNECTIONS TO EXTERNAL DEVICES



Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
31:24	CH0NB	—	—	—	CH0SB<3:0>			
00.40	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
23:10	CH0NA	—	—	—	CH0SA<3:0>			
45.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	—	—	—	—	_	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
						_		

REGISTER 22-4: AD1CHS: ADC INPUT SELECT REGISTER

CHONB: Negative Input Select bit for Sample B

Legend:

bit 31

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

		 1 = Channel 0 negative input is AN1 0 = Channel 0 negative input is VREFL
bit 30	-28	Unimplemented: Read as '0'
bit 27	-24	CH0SB<3:0>: Positive Input Select bits for Sample B
		1111 = Channel 0 positive input is Open ⁽¹⁾ 1110 = Channel 0 positive input is IVREF ⁽²⁾ 1101 = Channel 0 positive input is CTMU temperature sensor (CTMUT) ⁽³⁾ 1100 = Channel 0 positive input is AN12 ⁽⁴⁾
		•
		•
		•
		0001 = Channel 0 positive input is AN1 0000 = Channel 0 positive input is AN0
bit 23		CH0NA: Negative Input Select bit for Sample A Multiplexer Setting ⁽²⁾
		1 = Channel 0 negative input is AN10 = Channel 0 negative input is VREFL
bit 22	-20	Unimplemented: Read as '0'
bit 19	-16	CH0SA<3:0>: Positive Input Select bits for Sample A Multiplexer Setting 1111 = Channel 0 positive input is Open ⁽¹⁾ 1110 = Channel 0 positive input is IVREF ⁽²⁾ 1101 = Channel 0 positive input is CTMU temperature (CTMUT) ⁽³⁾ 1100 = Channel 0 positive input is AN12 ⁽⁴⁾
		•
		•
		•
		0001 = Channel 0 positive input is AN1 0000 = Channel 0 positive input is AN0
bit 15	-0	Unimplemented: Read as '0'
Note	1: 2: 3: 4:	This selection is only used with CTMU capacitive and time measurement. See Section 24.0 "Comparator Voltage Reference (CVREF)" for more information. See Section 25.0 "Charge Time Measurement Unit (CTMU)" for more information. AN12 is only available on 44-pin devices. AN6-AN8 are not available on 28-pin devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	—	_	—	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	_	—
45.0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
15:8	—	—	IOLOCK ⁽¹⁾	PMDLOCK ⁽¹⁾	—	—		_
7.0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
7:0	—	_	_	_	JTAGEN	_		TDOEN

REGISTER 27-5: CFGCON: CONFIGURATION CONTROL REGISTER

Legend:

Logonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

- bit 13 IOLOCK: Peripheral Pin Select Lock bit⁽¹⁾
 - 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
 - 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.
- bit 12 PMDLOCK: Peripheral Module Disable bit⁽¹⁾
 - 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
 - 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11-4 Unimplemented: Read as '0'

- bit 3 JTAGEN: JTAG Port Enable bit
 - 1 = Enable the JTAG port
 - 0 = Disable the JTAG port
- bit 2-1 Unimplemented: Read as '1'
- bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG bit
 - 1 = 2-wire JTAG protocol uses TDO
 - 0 = 2-wire JTAG protocol does not use TDO
- Note 1: To change this bit, the unlock sequence must be performed. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.



ABLE	ABLE 30-22: RESETS TIMING							
AC CHARACTERISTICS			$\begin{tabular}{lllllllllllllllllllllllllllllllllll$					
Param. No.	Symbol	Characteristics ⁽¹⁾	Min.	Typical ⁽²⁾	Max.	Units	Conditions	
SY00	Τρυ	Power-up Period Internal Voltage Regulator Enabled		400	600	μS	_	
SY02	TSYSDLY	System Delay Period: Time Required to Reload Device Configuration Fuses plus SYSCLK Delay before First instruction is Fetched.		1 μs + 8 SYSCLK cycles	_		_	
SY20	TMCLR	MCLR Pulse Width (low)	2	_	_	μS	_	
SY30	TBOR	BOR Pulse Width (low)	_	1	_	μS	_	

These parameters are characterized, but not tested in manufacturing. Note 1:

2: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Characterized by design but not tested.

44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Linite	N		c
	Units	N		3
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

Revision E (October 2012)

All singular pin diagram occurrences of CVREF were changed to: CVREFOUT. In addition, minor text and formatting changes were incorporated throughout the document.

All major changes are referenced by their respective section in Table A-4.

TABLE A-4:	MAJOR SECTION UPDATI	ΞS
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Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Updated the following feature sections: "Operating Conditions" "Communication Interfaces"
2.0 "Guidelines for Getting Started with 32-bit MCUs"	Removed Section 2.8 "Configuration of Analog and Digital Pins During ICSP Operations".
3.0 "CPU"	Removed references to GPR shadow registers in 3.1 "Features" and 3.2.1 "Execution Unit" .
4.0 "Memory Organization"	Updated the BRG bit range in the SPI1 and SPI2 Register Map (see Table 4-8). Added the PWP<6> bit to the Device Configuration Word Summary (see Table 4-17).
5.0 "Flash Program Memory"	Added a note with Flash page size and row size information.
7.0 "Interrupt Controller"	Updated the TPC<2:0> bit definitions (see Register 7-1). Updated the IPTMR<31:0> bit definition (see Register 7-3).
8.0 "Oscillator Configuration"	Updated the PIC32MX1XX/2XX Family Clock Diagram (see Figure 8-1). Updated the RODIV<14:0> bit definitions (see Register 8-3).
10.0 "USB On-The-Go (OTG)"	Updated the Notes in the USB Interface Diagram (see Figure 10-1).
18.0 "Universal Asynchronous Receiver Transmitter (UART)"	Updated the baud rate range in the list of primary features.
26.0 "Special Features"	Added the PWP<6> bit to the Device Configuration Word 0 (see Register 26-1).
29.0 "Electrical Characteristics"	 Added Note 1 to Operating MIPS vs. Voltage (see Table 29-1). Added Note 2 to DC Temperature and Voltage Specifications (see Table 29-4). Updated the Conditions for parameter DC25 in DC Characteristics: Operating Current (IDD) (see Table 29-5). Added Note 2 to Electrical Characteristics: BOR (see Table 29-10). Added Note 4 to Comparator Specifications (see Table 29-12). Added Note 5 to ADC Module Specifications (see Table 29-32). Updated the 10-bit Conversion Rate Parameters and added Note 3 (see Table 29-33). Added Note 4 to the Analog-to-Digital Conversion Timing Requirements (see Table 29-34). Added Note 3 to CTMU Current Source Specifications (see Table 29-39).
30.0 "50 MHz Electrical Characteristics"	New chapter with electrical characteristics for 50 MHz devices.
31.0 "Packaging Information"	The 36-pin and 44-pin VTLA packages have been updated.

Revision J (April 2016)

This revision includes the following major changes as described in Table A-8, as well as minor updates to text and formatting, which were incorporated throughout the document.

TABLE A-8: MAJOR SECTION UPDATES

Section	Update Description
"32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	The PIC32MX270FDB device and Note 4 were added to TABLE 2: "PIC32MX2XX 28/36/44-pin USB Family Features".
2.0 "Guidelines for Getting Started with 32-bit MCUs"	EXAMPLE 2-1: "Crystal Load Capacitor Calculation" was updated.
30.0 "Electrical Characteristics"	Parameter DO50a (Csosc) was removed from the Capacitive Loading Requirements on Output Pins AC Characteristics (see Table 30-16).
"Product Identification System"	The device mapping was updated to include type B for Software Targeting.

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