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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (256К × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16К х 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx130f256d-50i-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### TABLE 4:PIN NAMES FOR 28-PIN USB DEVICES

28	PIN SOIC, SPDIP, SSOP (TOP VIEW) <sup>(1,2,3)</sup>					
	1 SSOP	28	1 SOIC	28	1	28 SPDIP
	PIC32MX210F016B PIC32MX220F032B PIC32MX230F064B PIC32MX230F256B PIC32MX250F128B PIC32MX270F256B					
Pin #	Full Pin Name	Pin #		Full Pin N	Name	
<b>Pin #</b>	Full Pin Name	<b>Pin #</b>	VBUS	Full Pin N	Name	
<b>Pin #</b> 1 2	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0	<b>Pin #</b> 15 16	VBUS TDI/RPB7/CTED3/PM	Full Pin N	Name	
<b>Pin #</b> 1 2 3	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1	<b>Pin #</b> 15 16 17	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE	Full Pin N D5/INT0/RE	Name 37 /RB8	
Pin # 1 2 3 4	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0	<b>Pin #</b> 15 16 17 18	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0           PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1	<b>Pin #</b> 15 16 17 18 19	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5 6	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0           PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1           AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2	Pin # 15 16 17 18 19 20	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I	Name 37 /RB8 RB9	
Pin # 1 2 3 4 5 6 7	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0           PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1           AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2           AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3	Pin #           15           16           17           18           19           20           21	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I FED11/RB10	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0           PGEC1/AN3/C1INC/C2INB/C3IND/RPB0/PMD0/RB1           AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2           AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3           Vss	Pin # 15 16 17 18 19 20 21 21 22	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I FED11/RB10 11	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8 9	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0           PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1           AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2           AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3           Vss           OSC1/CLKI/RPA2/RA2	Pin #           15           16           17           18           19           20           21           22           23	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I FED11/RB10 11	Name 37 /RB8 RB9 0	
Pin # 1 2 3 4 5 6 7 8 9 10	Full Pin Name           MCLR           PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0           PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1           PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0           PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1           AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2           AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3           Vss           OSC1/CLKI/RPA2/RA2           OSC2/CLKO/RPA3/PMA0/RA3	Pin #           15           16           17           18           19           20           21           22           23           24	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/F	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I TED11/RB10 11 PMRD/RB13	Name 37 /RB8 RB9 0 3	
Pin # 1 2 3 4 5 6 7 8 9 10 11	Full Pin Name         MCLR         PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0         PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1         PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0         PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1         AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2         AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3         Vss         OSC1/CLKI/RPA2/RA2         OSC2/CLKO/RPA3/PMA0/RA3         SOSCI/RPB4/RB4	Pin #           15           16           17           18           19           20           21           22           23           24           25	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/I CVREFOUT/AN10/C3IN	Full Pin N D5/INT0/RE D10/PMD4, ED4/PMD3/I FED11/RB10 11 IB/RPB14/V	Name 37 /RB8 RB9 0 3 /BUSON/S	SCK1/CTED5/RB14
Pin # 1 2 3 4 5 6 7 8 9 10 11 12	Full Pin Name         MCLR         PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0         PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1         PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0         PGEC1/AN3/C1INC/C2INB/C3IND/RPB0/PMD0/RB1         AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2         AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3         Vss         OSC1/CLKI/RPA2/RA2         OSC2/CLKO/RPA3/PMA0/RA3         SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	Pin #           15           16           17           18           19           20           21           22           23           24           25           26	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/f CVREFOUT/AN10/C3IN AN9/C3INA/RPB15/SC	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I TED11/RB10 11 PMRD/RB11 IB/RPB14/V CK2/CTED6	Name 37 /RB8 RB9 0 0 3 /BUSON/S 5/PMCS1	SCK1/CTED5/RB14 1/RB15
Pin # 1 2 3 4 5 6 7 8 9 10 11 12 13	Full Pin Name         MCLR         PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0         PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1         PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0         PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1         AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2         AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3         Vss         OSC1/CLKI/RPA2/RA2         OSC2/CLKO/RPA3/PMA0/RA3         SOSCI/RPB4/RB4         SOSCO/RPA4/T1CK/CTED9/PMA1/RA4         VpD	Pin #           15           16           17           18           19           20           21           22           23           24           25           26           27	VBUS TDI/RPB7/CTED3/PM TCK/RPB8/SCL1/CTE TDO/RPB9/SDA1/CTE VSS VCAP PGED2/RPB10/D+/CT PGEC2/RPB11/D-/RB VUSB3V3 AN11/RPB13/CTPLS/F CVREFOUT/AN10/C3IN AN9/C3INA/RPB15/SC AVSS	Full Pin N D5/INT0/RE D10/PMD4/ ED4/PMD3/I TED11/RB10 11 PMRD/RB13 IB/RPB14/V CK2/CTED6	Name 37 /RB8 RB9 0 0 3 /BUSON/S 6)/PMCS1	SCK1/CTED5/RB14 1/RB15

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: Shaded pins are 5V tolerant.

### TABLE 7: PIN NAMES FOR 36-PIN GENERAL PURPOSE DEVICES

# 36-PIN VTLA (TOP VIEW)<sup>(1,2,3,5)</sup>

PIC32MX110F016C PIC32MX120F032C PIC32MX130F064C PIC32MX150F128C

36

			I
Pin #	Full Pin Name	Pin #	Full Pin Name
1	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2	19	TDO/RPB9/SDA1/CTED4/PMD3/RB9
2	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3	20	RPC9/CTED7/RC9
3	PGED4 <sup>(4)</sup> /AN6/RPC0/RC0	21	Vss
4	PGEC4 <sup>(4)</sup> /AN7/RPC1/RC1	22	VCAP
5	VDD	23	VDD
6	Vss	24	PGED2/RPB10/CTED11/PMD2/RB10
7	OSC1/CLKI/RPA2/RA2	25	PGEC2/TMS/RPB11/PMD1/RB11
8	OSC2/CLKO/RPA3/PMA0/RA3	26	AN12/PMD0/RB12
9	SOSCI/RPB4/RB4	27	AN11/RPB13/CTPLS/PMRD/RB13
10	SOSCO/RPA4/T1CK/CTED9/PMA1/RA4	28	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14
11	RPC3/RC3	29	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15
12	Vss	30	AVss
13	VDD	31	AVdd
14	VDD	32	MCLR
15	PGED3/RPB5/PMD7/RB5	33	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0
16	PGEC3/RPB6/PMD6/RB6	34	VREF-/CVREF-/AN1/RPA1/CTED2/RA1
17	TDI/RPB7/CTED3/PMD5/INT0/RB7	35	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0
18	TCK/RPB8/SCL1/CTED10/PMD4/RB8	36	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016C and PIC32MX120F032C devices.

5: Shaded pins are 5V tolerant.

#### TABLE 11: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES

# 44-PIN TQFP (TOP VIEW)<sup>(1,2,3,5)</sup>

PIC32MX110F016D PIC32MX120F032D PIC32MX130F064D PIC32MX130F256D PIC32MX150F128D PIC32MX170F256D

44

1

Pin #	Full Pin Name	Pin #	Full Pin Name
1		22	
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/C1ED13/RB2
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2
6	Vss	28	Vdd
7	VCAP	29	Vss
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4
12	PGED4 <sup>(4)</sup> /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4
13	PGEC4 <sup>(4)</sup> /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4
16	AVss	38	RPC5/PMA3/RC5
17	AVDD	39	Vss
18	MCLR	40	Vdd
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8

Note 1: The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and Section 11.3 "Peripheral Pin Select" for restrictions.

2: Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See Section 11.0 "I/O Ports" for more information.

3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.

5: Shaded pins are 5V tolerant.

# 3.0 CPU

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 2.** "CPU" (DS60001113), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32). Resources for the MIPS32<sup>®</sup> M4K<sup>®</sup> Processor Core are available at: www.imgtec.com.

The MIPS32<sup>®</sup> M4K<sup>®</sup> Processor Core is the heart of the PIC32MX1XX/2XX family processor. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of instruction execution to the destinations.

## 3.1 Features

- 5-stage pipeline
- 32-bit address and data paths
- MIPS32 Enhanced Architecture (Release 2)
  - Multiply-accumulate and multiply-subtract instructions
  - Targeted multiply instruction
  - Zero/One detect instructions
  - WAIT instruction
  - Conditional move instructions (MOVN, MOVZ)
  - Vectored interrupts
  - Programmable exception vector base
  - Atomic interrupt enable/disable
  - Bit field manipulation instructions

- MIPS16e<sup>®</sup> code compression
  - 16-bit encoding of 32-bit instructions to improve code density
  - Special PC-relative instructions for efficient loading of addresses and constants
  - SAVE and RESTORE macro instructions for setting up and tearing down stack frames within subroutines
  - Improved support for handling 8 and 16-bit data types
- Simple Fixed Mapping Translation (FMT) mechanism
- · Simple dual bus interface
  - Independent 32-bit address and data buses
  - Transactions can be aborted to improve interrupt latency
- · Autonomous multiply/divide unit
  - Maximum issue rate of one 32x16 multiply per clock
  - Maximum issue rate of one 32x32 multiply every other clock
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (*rs*) sign extension-dependent)
- Power control
  - Minimum frequency: 0 MHz
  - Low-Power mode (triggered by WAIT instruction)
  - Extensive use of local gated clocks
- EJTAG debug and instruction trace
  - Support for single stepping
  - Virtual instruction and data address/value
  - Breakpoints

#### FIGURE 3-1: MIPS32<sup>®</sup> M4K<sup>®</sup> PROCESSOR CORE BLOCK DIAGRAM



# 4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3.** "Memory Organization" (DS60001115), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- · Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

# 4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.



#### FIGURE 4-3: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 64 KB FLASH)



#### FIGURE 4-4: MEMORY MAP ON RESET FOR PIC32MX150/250 DEVICES (32 KB RAM, 128 KB FLASH)

2: The size of this memory region is programmable (see Section 3. "Memory Organization" (DS60001115) in the "*PIC32 Family Reference Manual*") and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0			
24.24	R	R	R	R	R	R	R	R			
31:24				BMXPFN	1SZ<31:24>						
22:16	R	R	R	R	R	R	R	R			
23.10	BMXPFMSZ<23:16>										
45.0	R	R	R	R	R	R	R	R			
15:8	BMXPFMSZ<15:8>										
7:0	R	R	R	R	R	R	R	R			
				BMXPF	MSZ<7:0>						

#### REGISTER 4-7: BMXPFMSZ: PROGRAM FLASH (PFM) SIZE REGISTER

# Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-0 BMXPFMSZ<31:0>: Program Flash Memory (PFM) Size bits

Static value that indicates the size of the PFM in bytes: 0x00004000 = Device has 16 KB Flash 0x00008000 = Device has 32 KB Flash 0x00010000 = Device has 64 KB Flash 0x00020000 = Device has 128 KB Flash 0x00040000 = Device has 256 KB Flash

#### REGISTER 4-8: BMXBOOTSZ: BOOT FLASH (IFM) SIZE REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
04.04	R	R	R	R	R	R	R	R		
31:24				BMXBOO	TSZ<31:24>					
22.16	R	R	R	R	R	R	R	R		
23.10	BMXBOOTSZ<23:16>									
45.0	R	R	R	R	R	R	R	R		
15:8	BMXBOOTSZ<15:8>									
7.0	R	R	R	R	R	R	R	R		
7:0		BMXBOOTSZ<7:0>								

Legend:						
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

bit 31-0 **BMXBOOTSZ<31:0>:** Boot Flash Memory (BFM) Size bits Static value that indicates the size of the Boot PFM in bytes: 0x00000C00 = Device has 3 KB boot Flash

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
21.24	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0		
31.24				NVMKE	Y<31:24>					
00.10	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0		
23:10	NVMKEY<23:16>									
45.0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0		
15:8	NVMKEY<15:8>									
7:0	W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0		
				NVMK	EY<7:0>					

#### REGISTER 5-2: NVMKEY: PROGRAMMING UNLOCK REGISTER

# Legend:

Legena.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-0 NVMKEY<31:0>: Unlock Register bits

These bits are write-only, and read as '0' on any read

Note: This register is used as part of the unlock sequence to prevent inadvertent writes to the PFM.

#### REGISTER 5-3: NVMADDR: FLASH ADDRESS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0		
24.24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
31:24				NVMAD	DR<31:24>					
00.40	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
23:10	NVMADDR<23:16>									
15.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
15:8	NVMADDR<15:8>									
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
7:0		NVMADDR<7:0>								

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 31-0 NVMADDR<31:0>: Flash Address bits

Bulk/Chip/PFM Erase: Address is ignored. Page Erase: Address identifies the page to erase. Row Program: Address identifies the row to program. Word Program: Address identifies the word to program. NOTES:

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#### REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—	—	—	—	—		—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	-	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	_	_	_	_		_
7.0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
7.0	ID	_	LSTATE	_	SESVD	SESEND		VBUSVD

#### Legend:

Logonal			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### bit 31-8 Unimplemented: Read as '0'

- bit 7 ID: ID Pin State Indicator bit
  - 1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle
  - 0 = A "type A" OTG cable has been inserted into the USB receptacle
- bit 6 Unimplemented: Read as '0'
- bit 5 LSTATE: Line State Stable Indicator bit
  - 1 = USB line state (SE0 (U1CON<6>) bit and JSTATE (U1CON<7>)) bit has been stable for previous 1 ms 0 = USB line state (SE0 and JSTATE) has not been stable for previous 1 ms

#### bit 4 Unimplemented: Read as '0'

- bit 3 SESVD: Session Valid Indicator bit
  - 1 = VBUS voltage is above Session Valid on the A or B device
  - 0 = VBUS voltage is below Session Valid on the A or B device
- bit 2 SESEND: B-Device Session End Indicator bit
  - 1 = VBUS voltage is below Session Valid on the B device
  - 0 = VBUS voltage is above Session Valid on the B device

#### bit 1 Unimplemented: Read as '0'

- bit 0 VBUSVD: A-Device VBUS Valid Indicator bit
  - 1 = VBUS voltage is above Session Valid on the A device
  - 0 = VBUS voltage is below Session Valid on the A device

#### REGISTER 13-1: TXCON: TYPE B TIMER CONTROL REGISTER (CONTINUED)

- bit 3 T32: 32-Bit Timer Mode Select bit<sup>(2)</sup>
  - 1 = Odd numbered and even numbered timers form a 32-bit timer
  - 0 = Odd numbered and even numbered timers form a separate 16-bit timer
- bit 2 Unimplemented: Read as '0'
- bit 1 **TCS:** Timer Clock Source Select bit<sup>(3)</sup>
  - 1 = External clock from TxCK pin
  - 0 = Internal peripheral clock
- bit 0 Unimplemented: Read as '0'
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: This bit is available only on even numbered timers (Timer2 and Timer4).
  - **3:** While operating in 32-bit mode, this bit has no effect for odd numbered timers (Timer3, and Timer5). All timer functions are set through the even numbered timers.
  - 4: While operating in 32-bit mode, this bit must be cleared on odd numbered timers to enable the 32-bit timer in Idle mode.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	—	—	—	—	—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:16	—	—	—	—	—	—	—	—
45.0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15:8	ON <sup>(1,2)</sup>	—	—	—	—	—	—	—
7:0	U-0	R-y	R-y	R-y	R-y	R-y	R/W-0	R/W-0
	_		S	WDTWINEN	WDTCLR			

#### REGISTER 14-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

Legend:	y = Values set from Configuration bits on POR					
R = Readable bit	W = Writable bit	Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set '0' = Bit is cleared x = Bit is unknown					

#### bit 31-16 Unimplemented: Read as '0'

- bit 15 **ON:** Watchdog Timer Enable bit<sup>(1,2)</sup>
  - 1 = Enables the WDT if it is not enabled by the device configuration
  - 0 = Disable the WDT if it was enabled in software
- bit 14-7 Unimplemented: Read as '0'
- bit 6-2 **SWDTPS<4:0>:** Shadow Copy of Watchdog Timer Postscaler Value from Device Configuration bits On reset, these bits are set to the values of the WDTPS <4:0> of Configuration bits.
- bit 1 WDTWINEN: Watchdog Timer Window Enable bit
  - 1 = Enable windowed Watchdog Timer
  - 0 = Disable windowed Watchdog Timer
- bit 0 **WDTCLR:** Watchdog Timer Reset bit
  - 1 = Writing a '1' will clear the WDT
  - 0 = Software cannot force this bit to a '0'
- **Note 1:** A read of this bit results in a '1' if the Watchdog Timer is enabled by the device configuration or software.
  - 2: When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

#### REGISTER 17-1: SPIxCON: SPI CONTROL REGISTER (CONTINUED)

- bit 5 MSTEN: Master Mode Enable bit
  - 1 = Master mode
  - 0 = Slave mode
- bit 4 DISSDI: Disable SDI bit
  - 1 = SDI pin is not used by the SPI module (pin is controlled by PORT function)
  - 0 = SDI pin is controlled by the SPI module
- bit 3-2 STXISEL<1:0>: SPI Transmit Buffer Empty Interrupt Mode bits
  - 11 = Interrupt is generated when the buffer is not full (has one or more empty elements)
  - 10 = Interrupt is generated when the buffer is empty by one-half or more
  - 01 = Interrupt is generated when the buffer is completely empty
  - 00 = Interrupt is generated when the last transfer is shifted out of SPISR and transmit operations are complete
- bit 1-0 SRXISEL<1:0>: SPI Receive Buffer Full Interrupt Mode bits
  - 11 = Interrupt is generated when the buffer is full
  - 10 = Interrupt is generated when the buffer is full by one-half or more
  - 01 = Interrupt is generated when the buffer is not empty
  - 00 = Interrupt is generated when the last word in the receive buffer is read (i.e., buffer is empty)
- **Note 1:** When using the 1:1 PBCLK divisor, the user's software should not read or write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.
  - 2: This bit can only be written when the ON bit = 0.
  - 3: This bit is not used in the Framed SPI mode. The user should program this bit to '0' for the Framed SPI mode (FRMEN = 1).
  - 4: When AUDEN = 1, the SPI module functions as if the CKP bit is equal to '1', regardless of the actual value of CKP.

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Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	r-1	r-1	r-1	r-1	r-1	r-1	r-1	r-1
31:24	—	—	—	—	—	—	—	—
00.40	r-1	r-1	r-1	r-1	r-1	R/P	R/P	R/P
23:10	—	—	—	—	—	FPLLODIV<2:0>		
45.0	R/P	r-1	r-1	r-1	r-1	R/P	R/P	R/P
15:8	UPLLEN <sup>(1)</sup>	—	—	_	_	UF	PLLIDIV<2:0>	.(1)
7:0	r-1	R/P-1	R/P	R/P-1	r-1	R/P	R/P	R/P
	_	F	PLLMUL<2:0>	•	_	F	PLLIDIV<2:0	>

#### **DEVCFG2: DEVICE CONFIGURATION WORD 2 REGISTER 27-3:**

Legend: r = Reserved bit		P = Programmable bit				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

#### bit 31-19 Reserved: Write '1'

bit 15

bit 7

bit 18-16 FPLLODIV<2:0>: Default PLL Output Divisor bits

- 111 = PLL output divided by 256 110 = PLL output divided by 64 101 = PLL output divided by 32 100 = PLL output divided by 16 011 = PLL output divided by 8 010 = PLL output divided by 4 001 = PLL output divided by 2 000 = PLL output divided by 1 UPLLEN: USB PLL Enable bit<sup>(1)</sup> 1 = Disable and bypass USB PLL 0 = Enable USB PLL bit 14-11 Reserved: Write '1' bit 10-8 UPLLIDIV<2:0>: USB PLL Input Divider bits<sup>(1)</sup> 111 = 12x divider 110 = 10x divider 101 = 6x divider100 = 5x divider 011 = 4x divider 010 = 3x divider 010 = 3x divider 001 = 2x divider000 = 1x divider Reserved: Write '1'
- bit 6-4 FPLLMUL<2:0>: PLL Multiplier bits
  - 111 = 24x multiplier 110 = 21x multiplier
  - 101 = 20x multiplier
  - 100 = 19x multiplier
  - 011 = 18x multiplier
  - 010 = 17x multiplier
  - 001 = 16x multiplier
  - 000 = 15x multiplier
- bit 3 Reserved: Write '1'

Note 1: This bit is only available on PIC32MX2XX devices.

# 30.2 AC Characteristics and Timing Parameters

The information contained in this section defines PIC32MX1XX/2XX 28/36/44-pin Family AC characteristics and timing parameters.

#### FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



#### TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min. Typical <sup>(1)</sup> Max. Units Conditions						
DO56	Сю	All I/O pins and OSC2	50 pF EC mode						
DO58	Св	SCLx, SDAx	— — 400 pF In I <sup>2</sup> C mode						

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

#### FIGURE 30-2: EXTERNAL CLOCK TIMING



#### TABLE 30-32: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

АС СНА	RACTER	ISTICS		Standard Operating Conditions: 2.3V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp					
Param. No.	Symbol	Charact	eristics	Min. <sup>(1)</sup>	Max.	Units	Conditions		
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Трв * (BRG + 2)	_	μs	_		
			400 kHz mode	Трв * (BRG + 2)	_	μs	—		
			1 MHz mode <b>(Note 2)</b>	Трв * (BRG + 2)	—	μs	_		
IM11	THI:SCL	Clock High Time	100 kHz mode	Трв * (BRG + 2)	—	μS	—		
			400 kHz mode	Трв * (BRG + 2)	—	μS	—		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μS	_		
IM20	TF:SCL	SDAx and SCLx	100 kHz mode	—	300	ns	CB is specified to be		
		Fall Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF		
			1 MHz mode (Note 2)	_	100	ns			
IM21	TR:SCL	SDAx and SCLx	100 kHz mode	—	1000	ns	CB is specified to be		
		Rise Time	400 kHz mode	20 + 0.1 Св	300	ns	from 10 to 400 pF		
	1 MHz mode (Note 2)		1 MHz mode (Note 2)	—	300	ns			
IM25	TSU:DAT	Data Input	100 kHz mode	250		ns			
		Setup Time	400 kHz mode	100	—	ns			
			1 MHz mode (Note 2)	100	—	ns			
IM26	THD:DAT	Data Input	100 kHz mode	0	—	μS	—		
		Hold Time	400 kHz mode	0	0.9	μS			
			1 MHz mode (Note 2)	0	0.3	μS			
IM30	TSU:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)		μS	Only relevant for		
		Setup Time	400 kHz mode	Трв * (BRG + 2)	—	μS	Repeated Start		
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs			
IM31	THD:STA	Start Condition	100 kHz mode	Трв * (BRG + 2)		μs	After this period, the		
		Hold Time	400 kHz mode	Трв * (BRG + 2)	—	μS	first clock pulse is		
	1 MHz mode (Note 2)		1 MHz mode (Note 2)	Трв * (BRG + 2)	—	μs	generaleu		
IM33	Tsu:sto	Stop Condition	100 kHz mode	Трв * (BRG + 2)		μs			
		Setup Time	400 kHz mode	Трв * (BRG + 2)		μs			
			1 MHz mode (Note 2)	Трв * (BRG + 2)	RG + 2) —				
IM34	THD:STO	Stop Condition	100 kHz mode	Трв * (BRG + 2)		ns	—		
		Hold Time	400 kHz mode	Трв * (BRG + 2)		ns			
			1 MHz mode (Note 2)	Трв * (BRG + 2)	—	ns			

**Note 1:** BRG is the value of the  $I^2C$  Baud Rate Generator.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**3:** The typical value for this parameter is 104 ns.

#### TABLE 30-34: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 5): 2.5V to 3.6V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +105^{\circ}C$ for V-temp						
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions		
Device	Supply								
AD01	AVDD	Module VDD Supply	Greater of VDD – 0.3 or 2.5	_	Lesser of VDD + 0.3 or 3.6	V	_		
AD02	AVss	Module Vss Supply	Vss	—	AVDD	V	(Note 1)		
Referen	ce Inputs								
AD05 AD05a	Vrefh	Reference Voltage High	AVss + 2.0 2.5	_	AVDD 3.6	V V	(Note 1) VREFH = AVDD (Note 3)		
AD06	Vrefl	Reference Voltage Low	AVss	—	VREFH – 2.0	V	(Note 1)		
AD07	Vref	Absolute Reference Voltage (VREFH – VREFL)	2.0	_	AVdd	V	(Note 3)		
AD08	IREF	Current Drain	—	250	400	μA	ADC operating		
AD08a			—	_	3	μA	ADC off		
Analog	Input								
AD12	VINH-VINL	Full-Scale Input Span	VREFL	_	VREFH	V	—		
AD13	VINL	Absolute Vın∟ Input Voltage	AVss – 0.3	_	AVDD/2	V	—		
AD14	Vin	Absolute Input Voltage	AVss - 0.3	—	AVDD + 0.3	V	—		
AD15	—	Leakage Current	_	±0.001	±0.610	μA	$\label{eq:VINL} \begin{array}{l} VINL = AVSS = VREFL = 0V,\\ AVDD = VREFH = 3.3V\\ Source Impedance = 10\;k\Omega \end{array}$		
AD17	Rin	Recommended Impedance of Analog Voltage Source	_	_	5k	Ω	(Note 1)		
ADC Ac	curacy – N	leasurements with Exte	rnal VREF+/V	REF-		1			
AD20c	Nr	Resolution		10 data bit	s	bits	—		
AD21c	INL	Integral Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V		
AD22c	DNL	Differential Non-linearity	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V (Note 2)		
AD23c	Gerr	Gain Error	> -1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.3V		
AD24c	EOFF	Offset Error	> -1	_	< 1	Lsb	VINL = AVSS = 0V, AVDD = 3.3V		
AD25c	_	Monotonicity		_	_	_	Guaranteed		

Note 1: These parameters are not characterized or tested in manufacturing.

2: With no missing codes.

**3:** These parameters are characterized, but not tested in manufacturing.

**4:** Characterized with a 1 kHz sine wave.

**5:** The ADC module is functional at VBORMIN < VDD < 2.5V, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

#### TABLE 30-37: PARALLEL SLAVE PORT REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}\mbox{C} \leq \mbox{TA} \leq +85^{\circ}\mbox{C for Industrial} \\ -40^{\circ}\mbox{C} \leq \mbox{TA} \leq +105^{\circ}\mbox{C for V-temp} \end{array}$				
Para m.No.	Symbol	Characteristics <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
PS1	TdtV2wr H	Data In Valid before $\overline{WR}$ or $\overline{CS}$ Inactive (setup time)	20			ns	_
PS2	TwrH2dt I	WR or CS Inactive to Data-In Invalid (hold time)	40		—	ns	—
PS3	TrdL2dt V	RD and CS Active to Data-Out Valid	—		60	ns	—
PS4	TrdH2dtl	RD Active or CS Inactive to Data-Out Invalid	0	_	10	ns	—
PS5	Tcs	CS Active Time	Трв + 40		—	ns	—
PS6	TwR	WR Active Time	Трв + 25		_	ns	_
PS7	Trd	RD Active Time	Трв + 25	_	_	ns	_

**Note 1:** These parameters are characterized, but not tested in manufacturing.

## FIGURE 30-21: PARALLEL MASTER PORT READ TIMING DIAGRAM



# 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







	Units		MILLIMETERS		
Dimensior	n Limits	MIN	NOM	MAX	
Number of Pins	N		44		
Pitch	е		0.65 BSC		
Overall Height	Α	0.80	0.90	1.00	
Standoff	A1	0.00 0.02 0.05			
Contact Thickness	A3	0.20 REF			
Overall Width	E		8.00 BSC		
Exposed Pad Width	E2	6.30	6.45	6.80	
Overall Length	D		8.00 BSC		
Exposed Pad Length	D2	6.30	6.45	6.80	
Contact Width	b	0.25 0.30 0.38			
Contact Length	L	0.30 0.40 0.50			
Contact-to-Exposed Pad	К	0.20	-	-	

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B