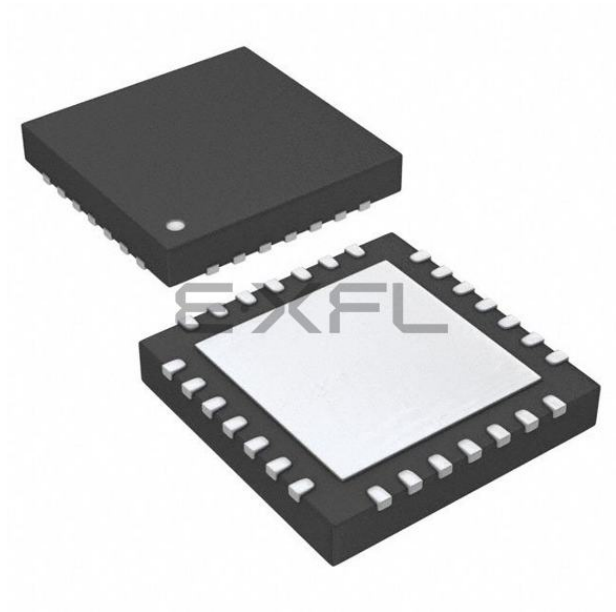

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128b-50i-ml |

**TABLE 4: PIN NAMES FOR 28-PIN USB DEVICES**

**28-PIN SOIC, SPDIP, SSOP (TOP VIEW)(1,2,3)**


**PIC32MX210F016B**
**PIC32MX220F032B**
**PIC32MX230F064B**
**PIC32MX230F256B**
**PIC32MX250F128B**
**PIC32MX270F256B**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | $\overline{\text{MCLR}}$ | 15 | $V_{BUS}$ |
| 2 | PGED3/$V_{REF}$+/$CV_{REF}$+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 | 16 | TDI/RPB7/CTED3/PMD5/INT0/RB7 |
| 3 | PGEC3/$V_{REF}$-/$CV_{REF}$-/AN1/RPA1/CTED2/PMD6/RA1 | 17 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 |
| 4 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 | 18 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 5 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 | 19 | $V_{SS}$ |
| 6 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 20 | $V_{CAP}$ |
| 7 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 | 21 | PGED2/RPB10/D+/CTED11/RB10 |
| 8 | $V_{SS}$ | 22 | PGEC2/RPB11/D-/RB11 |
| 9 | OSC1/CLKI/RPA2/RA2 | 23 | $V_{USB3V3}$ |
| 10 | OSC2/CLKO/RPA3/PMA0/RA3 | 24 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 11 | SOSCI/RPB4/RB4 | 25 | $CV_{REFOUT}$/AN10/C3INB/RPB14/$V_{BUSON}$/SCK1/CTED5/RB14 |
| 12 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 26 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 13 | $V_{DD}$ | 27 | $AV_{SS}$ |
| 14 | TMS/RPB5/USBID/RB5 | 28 | $AV_{DD}$ |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** Shaded pins are 5V tolerant.

**TABLE 5: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES**

**28-PIN QFN (TOP VIEW)(1,2,3.4)**

**PIC32MX110F016B**
**PIC32MX120F032B**
**PIC32MX130F064B**
**PIC32MX130F256B**
**PIC32MX150F128B**
**PIC32MX170F256B**

28 1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0 | 15 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1 | 16 | VSS |
| 3 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2 | 17 | VCAP |
| 4 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 | 18 | PGED2/RPB10/CTED11/PMD2/RB10 |
| 5 | VSS | 19 | PGEC2/TMS/RPB11/PMD1/RB11 |
| 6 | OSC1/CLKI/RPA2/RA2 | 20 | AN12/PMD0/RB12 |
| 7 | OSC2/CLKO/RPA3/PMA0/RA3 | 21 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 8 | SOSCI/RPB4/RB4 | 22 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14 |
| 9 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 23 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 10 | VDD | 24 | AVSS |
| 11 | PGED3/RPB5/PMD7/RB5 | 25 | AVDD |
| 12 | PGEC3/RPB6/PMD6/RB6 | 26 | $\overline{\text{MCLR}}$ |
| 13 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 27 | VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0 |
| 14 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 28 | VREF-/CVREF-/AN1/RPA1/CTED2/RA1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** Shaded pins are 5V tolerant.

## Referenced Sources

This device data sheet is based on the following individual chapters of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note:** To access the following documents, refer to the *Documentation > Reference Manuals* section of the Microchip PIC32 website: http://www.microchip.com/pic32

- **Section 1. "Introduction"** (DS60001127)
- **Section 2. "CPU"** (DS60001113)
- **Section 3. "Memory Organization"** (DS60001115)
- **Section 5. "Flash Program Memory"** (DS60001121)
- **Section 6. "Oscillator Configuration"** (DS60001112)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupt Controller"** (DS60001108)
- **Section 9. "Watchdog Timer and Power-up Timer"** (DS60001114)
- **Section 10. "Power-Saving Features"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 13. "Parallel Master Port (PMP)"** (DS60001128)
- **Section 14. "Timers"** (DS60001105)
- **Section 15. "Input Capture"** (DS60001122)
- **Section 16. "Output Compare"** (DS60001111)
- **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference ($CV_{REF}$)"** (DS60001109)
- **Section 21. "Universal Asynchronous Receiver Transmitter (UART)"** (DS60001107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS60001106)
- **Section 24. "Inter-Integrated Circuit ($I^2C$)"** (DS60001116)
- **Section 27. "USB On-The-Go (OTG)"** (DS60001126)
- **Section 29. "Real-Time Clock and Calendar (RTCC)"** (DS60001125)
- **Section 31. "Direct Memory Access (DMA) Controller"** (DS60001117)
- **Section 32. "Configuration"** (DS60001124)
- **Section 33. "Programming and Diagnostics"** (DS60001129)
- **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167)

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| PMA0 | 7 | 10 | 8 | 3 | I/O | TTL/ST | Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes) |
| PMA1 | 9 | 12 | 10 | 2 | I/O | TTL/ST | Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes) |
| PMA2 | | — | — | 27 | O | — | Parallel Master Port address (Demultiplexed Master modes) |
| PMA3 | | — | — | 38 | O | — | |
| PMA4 | | — | — | 37 | O | — | |
| PMA5 | | — | — | 4 | O | — | |
| PMA6 | | — | — | 5 | O | — | |
| PMA7 | | — | — | 13 | O | — | |
| PMA8 | | — | — | 32 | O | — | |
| PMA9 | | — | — | 35 | O | — | |
| PMA10 | | — | — | 12 | O | — | |
| PMCS1 | 23 | 26 | 29 | 15 | O | — | Parallel Master Port Chip Select 1 strobe |
| PMD0 | 20(2) | 23(2) | 26(2) | 10(2) | I/O | TTL/ST | Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes) |
| | 1(3) | 4(3) | 35(3) | 21(3) | | | |
| PMD1 | 19(2) | 22(2) | 25(2) | 9(2) | I/O | TTL/ST | |
| | 2(3) | 5(3) | 36(3) | 22(3) | | | |
| PMD2 | 18(2) | 21(2) | 24(2) | 8(2) | I/O | TTL/ST | |
| | 3(3) | 6(3) | 1(3) | 23(3) | | | |
| PMD3 | 15 | 18 | 19 | 1 | I/O | TTL/ST | |
| PMD4 | 14 | 17 | 18 | 44 | I/O | TTL/ST | |
| PMD5 | 13 | 16 | 17 | 43 | I/O | TTL/ST | |
| PMD6 | 12(2) | 15(2) | 16(2) | 42(2) | I/O | TTL/ST | |
| | 28(3) | 3(3) | 34(3) | 20(3) | | | |
| PMD7 | 11(2) | 14(2) | 15(2) | 41(2) | I/O | TTL/ST | |
| | 27(3) | 2(3) | 33(3) | 19(3) | | | |
| PMRD | 21 | 24 | 27 | 11 | O | — | Parallel Master Port read strobe |
| PMWR | 22(2) | 25(2) | 28(2) | 14(2) | O | — | Parallel Master Port write strobe |
| | 4(3) | 7(3) | 2(3) | 24(3) | | | |
| VBUS | 12(3) | 15(3) | 16(3) | 42(3) | I | Analog | USB bus power monitor |
| VUSB3V3 | 20(3) | 23(3) | 26(3) | 10(3) | P | — | USB internal transceiver supply. This pin must be connected to VDD. |
| VBUSON | 22(3) | 25(3) | 28(3) | 14(3) | O | — | USB Host and OTG bus power control output |
| D+ | 18(3) | 21(3) | 24(3) | 8(3) | I/O | Analog | USB D+ |
| D- | 19(3) | 22(3) | 25(3) | 9(3) | I/O | Analog | USB D- |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

## 2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MCUs

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the documents listed in the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

### 2.1 Basic Connection Requirements

Getting started with the PIC32MX1XX/2XX 28/36/44-pin Family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **2.2 "Decoupling Capacitors"**)
- VCAP pin (see **2.3 "Capacitor on Internal Voltage Regulator (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **2.7 "External Oscillator Pins"**)

The following pins may be required:

- VREF+/VREF- pins – used when external voltage reference for the ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

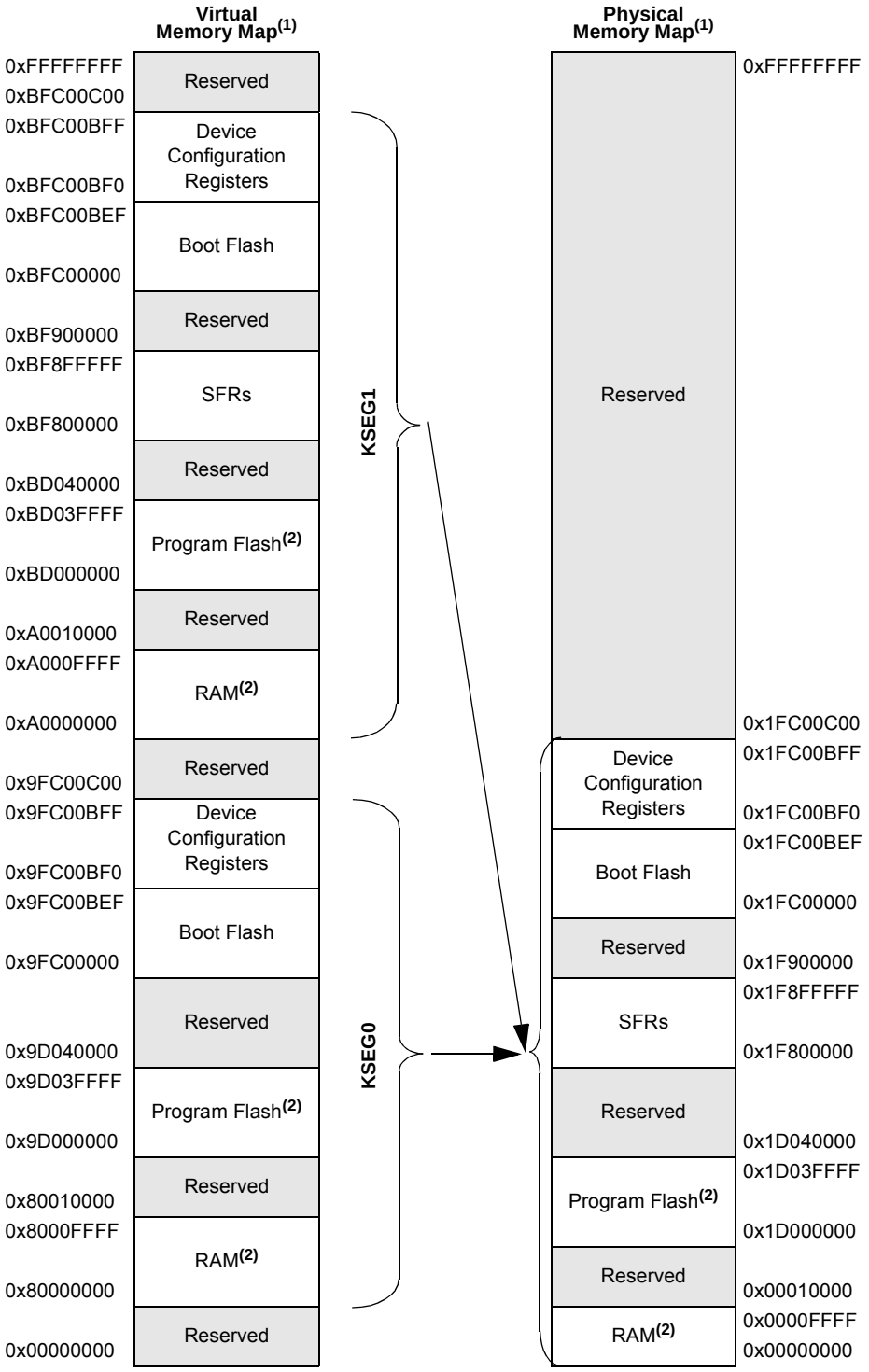
### 2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high frequency noise:** If the board is experiencing high frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB track inductance.

**FIGURE 4-5: MEMORY MAP ON RESET FOR PIC32MX170/270 DEVICES (64 KB RAM, 256 KB FLASH)**




**Note 1:** Memory areas are not shown to scale.

**2:** The size of this memory region is programmable (see **Section 3. "Memory Organization"** (DS60001115) in the *"PIC32 Family Reference Manual"*) and can be changed by initialization code provided by end-user development tools (refer to the specific development tool documentation for information).

**REGISTER 10-1: U1OTGIR: USB OTG INTERRUPT STATUS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | R/WC-0, HS | U-0 | R/WC-0, HS |
| | IDIF | T1MSECIF | LSTATEIF | ACTVIF | SESVDIF | SESENDIF | — | VBUSVDIF |

| **Legend:** | WC = Write '1' to clear | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **IDIF:** ID State Change Indicator bit
- 1 = A change in the ID state was detected
- 0 = No change in the ID state was detected

bit 6 **T1MSECIF:** 1 Millisecond Timer bit
- 1 = 1 millisecond timer has expired
- 0 = 1 millisecond timer has not expired

bit 5 **LSTATEIF:** Line State Stable Indicator bit
- 1 = USB line state has been stable for 1 ms, but different from last time
- 0 = USB line state has not been stable for 1 ms

bit 4 **ACTVIF:** Bus Activity Indicator bit
- 1 = Activity on the D+, D-, ID or VBUS pins has caused the device to wake-up
- 0 = Activity has not been detected

bit 3 **SESVDIF:** Session Valid Change Indicator bit
- 1 = VBUS voltage has dropped below the session end level
- 0 = VBUS voltage has not dropped below the session end level

bit 2 **SESENDIF:** B-Device VBUS Change Indicator bit
- 1 = A change on the session end input was detected
- 0 = No change on the session end input was detected

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVDIF:** A-Device VBUS Change Indicator bit
- 1 = A change on the session valid input was detected
- 0 = No change on the session valid input was detected

**NOTES:**

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

### 26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

**Note 1:** Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

**2:** Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

### 26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

### 26.4.1 CONTROLLING CONFIGURATION CHANGES

Because peripherals can be disabled during run time, some restrictions on disabling peripherals are needed to prevent accidental configuration changes. PIC32 devices include two features to prevent alterations to enabled or disabled peripherals:

- Control register lock sequence
- Configuration bit select lock

#### 26.4.1.1 Control Register Lock

Under normal operation, writes to the PMDx registers are not allowed. Attempted writes appear to execute normally, but the contents of the registers remain unchanged. To change these registers, they must be unlocked in hardware. The register lock is controlled by the Configuration bit, PMDLOCK (CFGCON<12>). Setting PMDLOCK prevents writes to the control registers; clearing PMDLOCK allows writes.

To set or clear PMDLOCK, an unlock sequence must be executed. Refer to **Section 6. "Oscillator"** (DS60001112) in the *"PIC32 Family Reference Manual"* for details.

#### 26.4.1.2 Configuration Bit Select Lock

As an additional level of safety, the device can be configured to prevent more than one write session to the PMDx registers. The Configuration bit, PMDL1WAY (DEVCFG3<28>), blocks the PMDLOCK bit from being cleared after it has been set once. If PMDLOCK remains set, the register unlock procedure does not execute, and the peripheral pin select control registers cannot be written to. The only way to clear the bit and re-enable PMD functionality is to perform a device Reset.

**TABLE 30-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | I/O Pins with PMP | VSS | — | 0.15 VDD | V | |
| | | I/O Pins | VSS | — | 0.2 VDD | V | |
| DI18 | | SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled **(Note 4)** |
| DI19 | | SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled **(Note 4)** |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O Pins not 5V-tolerant(5) | 0.65 VDD | — | VDD | V | **(Note 4,6)** |
| | | I/O Pins 5V-tolerant with PMP(5) | 0.25 VDD + 0.8V | — | 5.5 | V | **(Note 4,6)** |
| | | I/O Pins 5V-tolerant(5) | 0.65 VDD | — | 5.5 | V | |
| DI28 | | SDAx, SCLx | 0.65 VDD | — | 5.5 | V | SMBus disabled **(Note 4,6)** |
| DI29 | | SDAx, SCLx | 2.1 | — | 5.5 | V | SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 **(Note 4,6)** |
| DI30 | ICNPU | **Change Notification Pull-up Current** | — | — | -50 | µA | VDD = 3.3V, VPIN = VSS **(Note 3,6)** |
| DI31 | ICNPD | **Change Notification Pull-down Current(4)** | — | — | -50 | µA | VDD = 3.3V, VPIN = VDD |
| | IIL | **Input Leakage Current (Note 3)** | | | | | |
| DI50 | | I/O Ports | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI51 | | Analog Input Pins | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI55 | | $\overline{\text{MCLR}}$(2) | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | — | — | ±1 | µA | VSS ≤ VPIN ≤ VDD, XT and HS modes |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

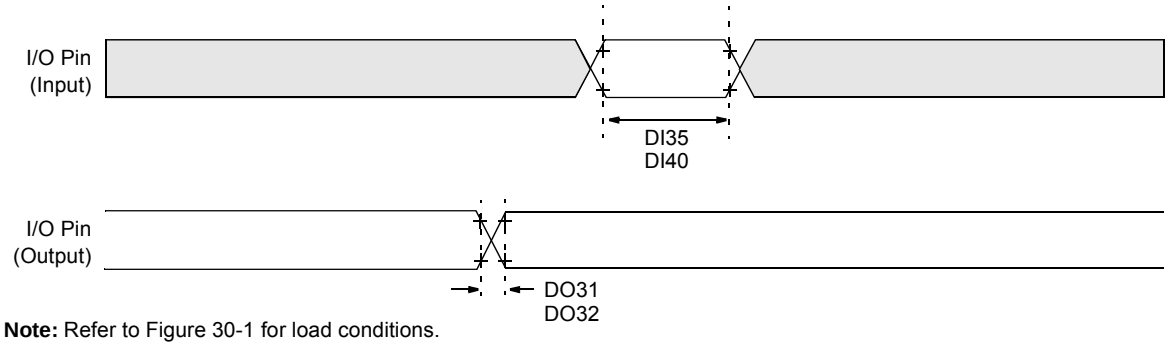
**3:** Negative current is defined as current sourced by the pin.

**4:** This parameter is characterized, but not tested in manufacturing.

**5:** See the **"Pin Diagrams"** section for the 5V-tolerant pins.

**6:** The VIH specifications are only in relation to externally applied inputs, and not with respect to the user-selectable internal pull-ups. External open drain input signals utilizing the internal pull-ups of the PIC32 device are guaranteed to be recognized only as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the minimum value of ICNPU. For External "input" logic inputs that require a pull-up source, to guarantee the minimum VIH of those components, it is recommended to use an external pull-up resistor rather than the internal pull-ups of the PIC32 device.

**FIGURE 30-3: I/O TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-21: I/O TIMING REQUIREMENTS**

| **AC CHARACTERISTICS** | | | **Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(2)** | **Min.** | **Typical(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 15 | ns | VDD < 2.5V |
| | | | — | 5 | 10 | ns | VDD > 2.5V |
| DI35 | TINP | INTx Pin High or Low Time | 10 | — | — | ns | — |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TSYSCLK | — |

**Note 1:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

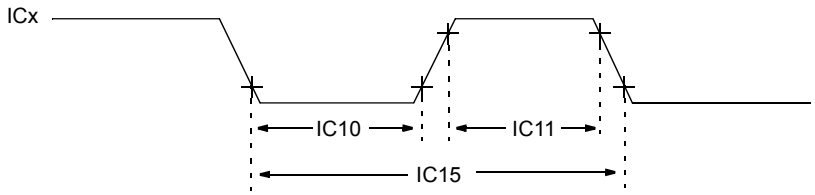
**2:** This parameter is characterized, but not tested in manufacturing.

**TABLE 30-24: TIMER2, 3, 4, 5 EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | | **Min.** | **Max.** | **Units** | **Conditions** | |
| TB10 | TTXH | TxCK High Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter TB15 | N = prescale value (1, 2, 4, 8, 16, 32, 64, 256) |
| TB11 | TTXL | TxCK Low Time | Synchronous, with prescaler | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter TB15 | |
| TB15 | TTXP | TxCK Input Period | Synchronous, with prescaler | [(Greater of [(25 ns or 2 TPB)/N] + 30 ns | — | ns | VDD > 2.7V | |
| | | | | [(Greater of [(25 ns or 2 TPB)/N] + 50 ns | — | ns | VDD < 2.7V | |
| TB20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | — | 1 | TPB | — | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 30-7: INPUT CAPTURE (CAPx) TIMING CHARACTERISTICS**



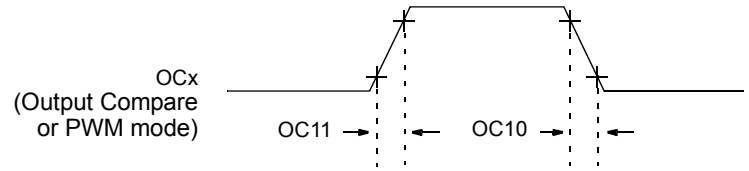

**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-25: INPUT CAPTURE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Max.** | **Units** | **Conditions** | |
| IC10 | TCCL | ICx Input Low Time | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter IC15. | N = prescale value (1, 4, 16) |
| IC11 | TCCH | ICx Input High Time | [(12.5 ns or 1 TPB)/N] + 25 ns | — | ns | Must also meet parameter IC15. | |
| IC15 | TCCP | ICx Input Period | [(25 ns or 2 TPB)/N] + 50 ns | — | ns | — | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 30-8: OUTPUT COMPARE MODULE (OCx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

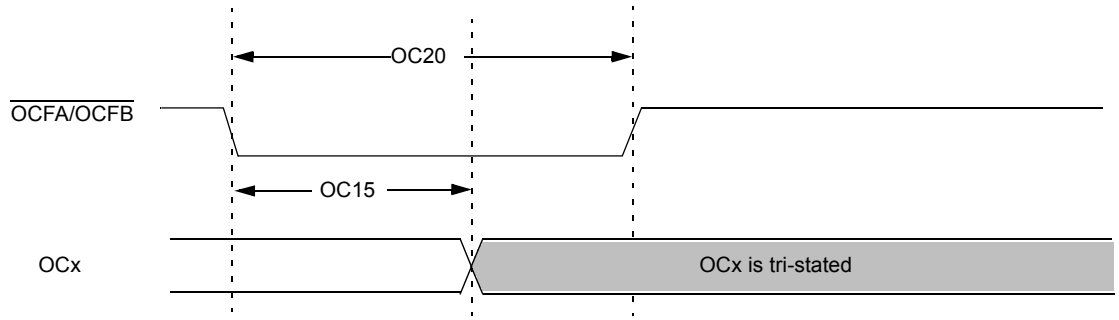
**TABLE 30-26: OUTPUT COMPARE MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| OC10 | TccF | OCx Output Fall Time | — | — | — | ns | See parameter DO32 |
| OC11 | TccR | OCx Output Rise Time | — | — | — | ns | See parameter DO31 |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 30-9: OCx/PWM MODULE TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-27: SIMPLE OCx/PWM MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics(1)** | **Min** | **Typical(2)** | **Max** | **Units** | **Conditions** |
| OC15 | TFD | Fault Input to PWM I/O Change | — | — | 50 | ns | — |
| OC20 | TFLT | Fault Input Pulse Width | 50 | — | — | ns | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 30-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING CHARACTERISTICS**

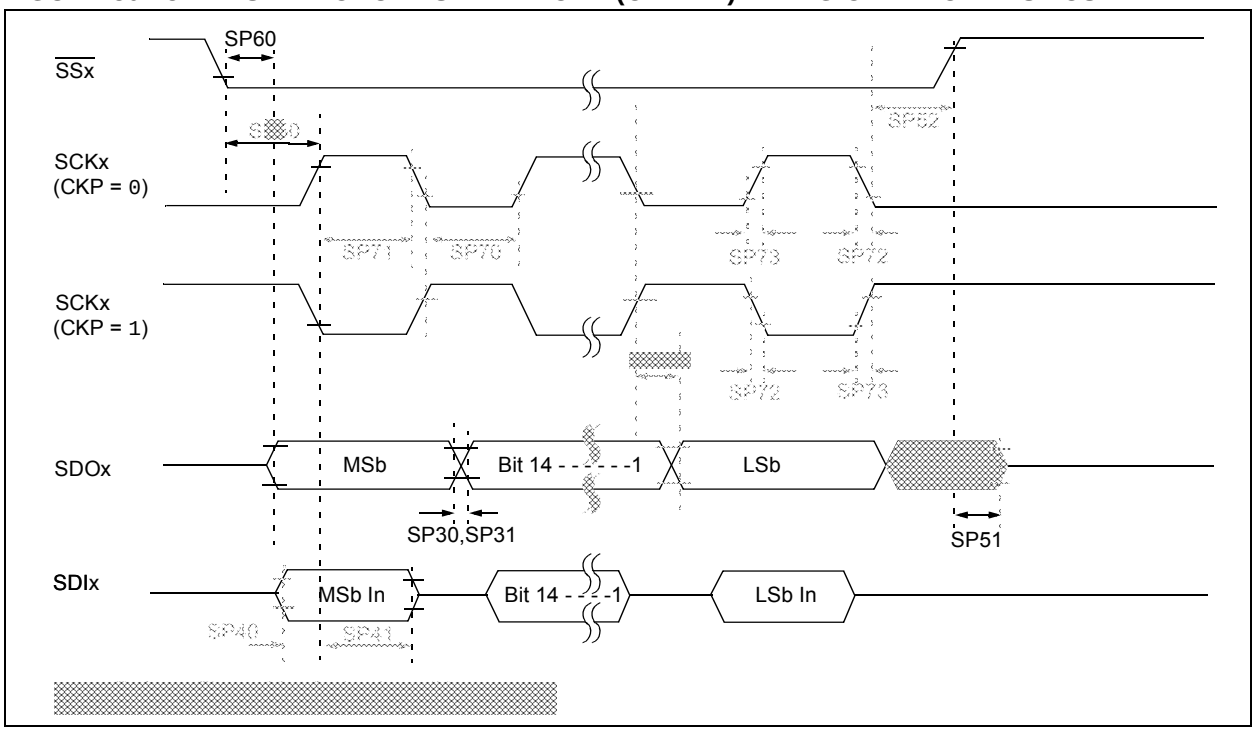



**TABLE 30-31: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typical(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | TscL | SCKx Input Low Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP71 | TscH | SCKx Input High Time **(Note 3)** | Tsck/2 | — | — | ns | — |
| SP72 | TscF | SCKx Input Fall Time | — | 5 | 10 | ns | — |
| SP73 | TscR | SCKx Input Rise Time | — | 5 | 10 | ns | — |
| SP30 | TdoF | SDOx Data Output Fall Time **(Note 4)** | — | — | — | ns | See parameter DO32 |
| SP31 | TdoR | SDOx Data Output Rise Time **(Note 4)** | — | — | — | ns | See parameter DO31 |
| SP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 20 | ns | VDD > 2.7V |
| | | | — | — | 30 | ns | VDD < 2.7V |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 10 | — | — | ns | — |
| SP50 | TssL2scH, TssL2scL | $\overline{SSx}$ ↓ to SCKx ↓ or SCKx ↑ Input | 175 | — | — | ns | — |

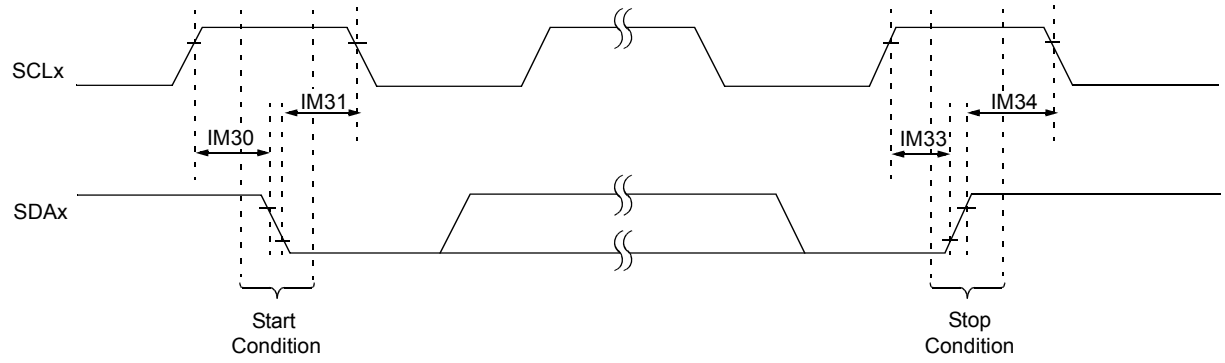
**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** The minimum clock period for SCKx is 50 ns.

**4:** Assumes 50 pF load on all SPIx pins.

**FIGURE 30-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 30-1 for load conditions.

**FIGURE 30-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**

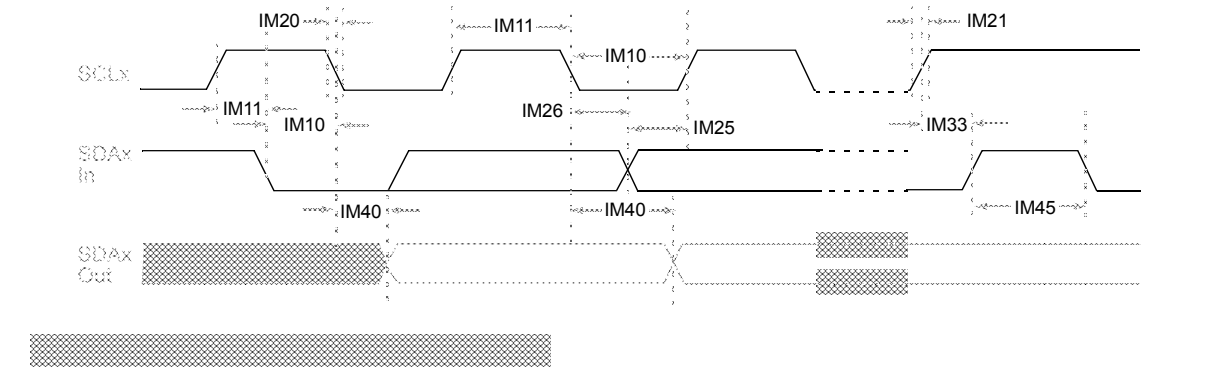
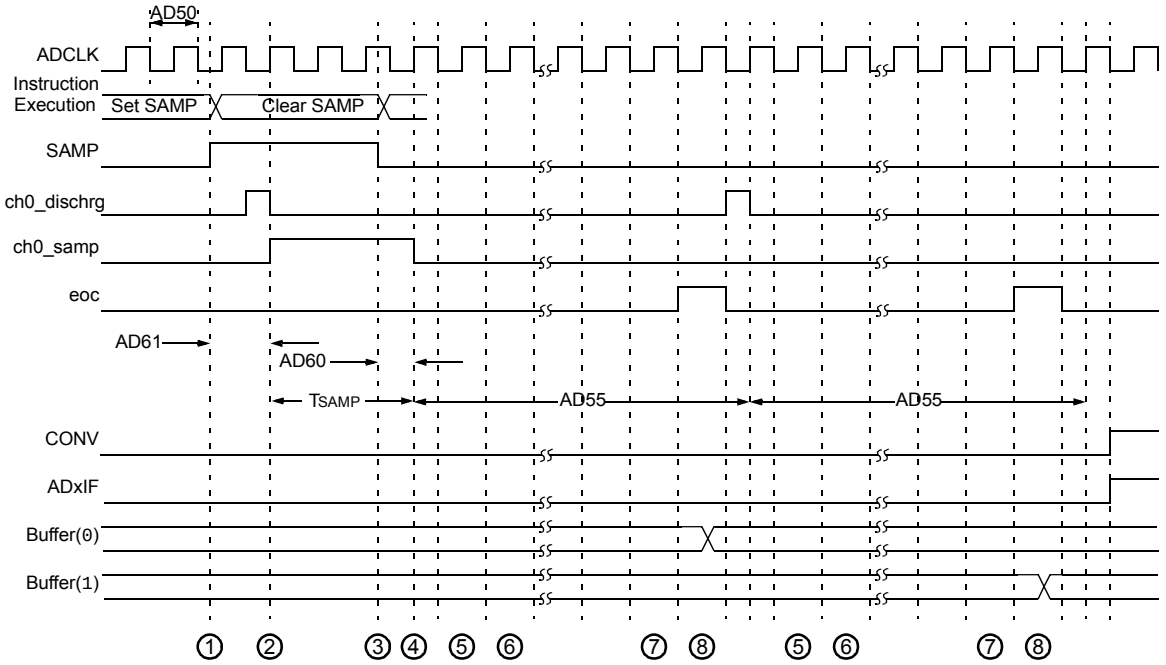


**FIGURE 30-18: ANALOG-TO-DIGITAL CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000)**




(1) – Software sets ADxCON. SAMP to start sampling.

(2) – Sampling starts after discharge period. TSAMP is described in **Section 17. "10-bit Analog-to-Digital Converter (ADC)"** (DS60001104) in the *"PIC32 Family Reference Manual"*.

(3) – Software clears ADxCON. SAMP to start conversion.

(4) – Sampling ends, conversion sequence starts.

(5) – Convert bit 9.

(6) – Convert bit 8.

(7) – Convert bit 0.

(8) – One TAD for end of conversion.

## 31.1 DC Characteristics

**TABLE 31-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts)(1) | Temp. Range (in °C) | Max. Frequency |
|---|---|---|---|
| | | | PIC32MX1XX/2XX 28/36/44-pin Family |
| MDC5 | 2.3-3.6V | -40°C to +85°C | 50 MHz |

**Note 1:** Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.

**TABLE 31-2: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial | |
|---|---|---|---|---|
| Parameter No. | Typical(3) | Max. | Units | Conditions |
| **Operating Current (IDD) (Note 1, 2)** | | | | |
| MDC24 | 25 | 37 | mA | 50 MHz |

**Note 1:** A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

**2:** The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, Program Flash, and SRAM data memory are operational, SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0), but the associated PMD bit is cleared
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash

**3:** RTCC and JTAG are disabled

**4:** Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 32-6: TYPICAL FRC FREQUENCY @ VDD = 3.3V**

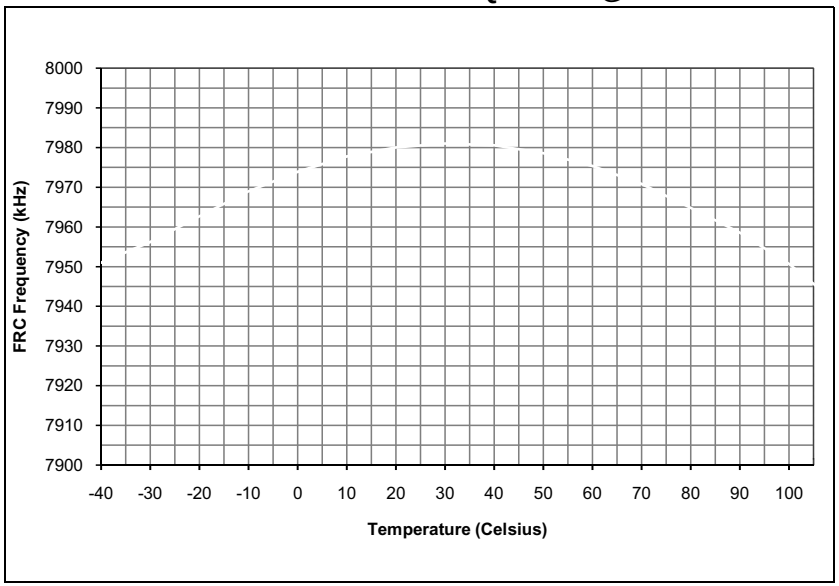



**FIGURE 32-7: TYPICAL LPRC FREQUENCY @ VDD = 3.3V**

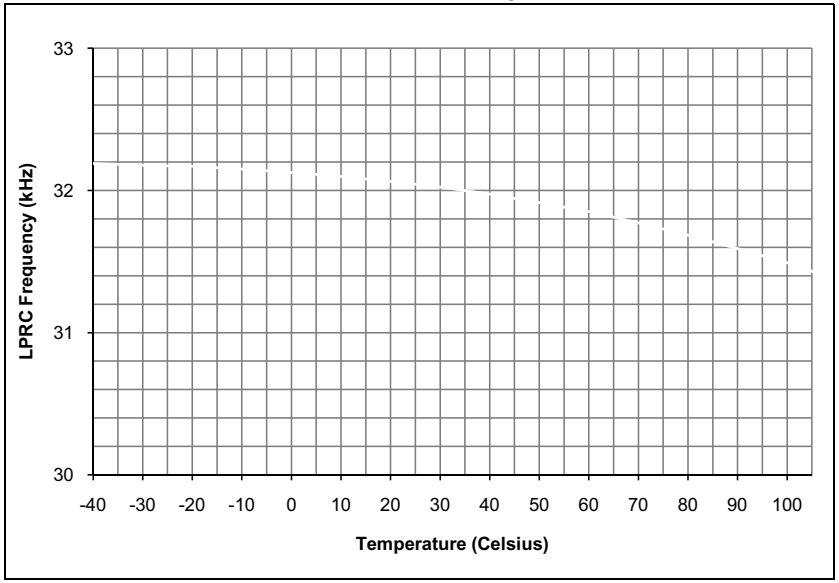
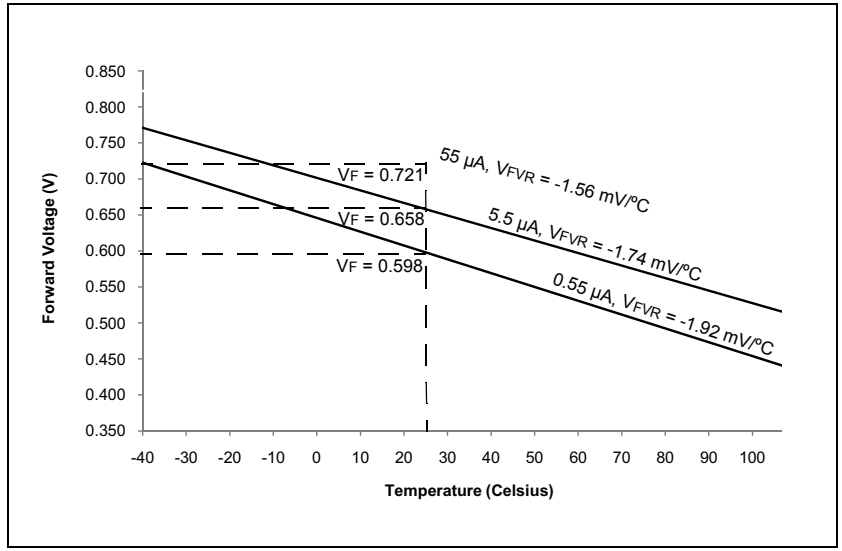
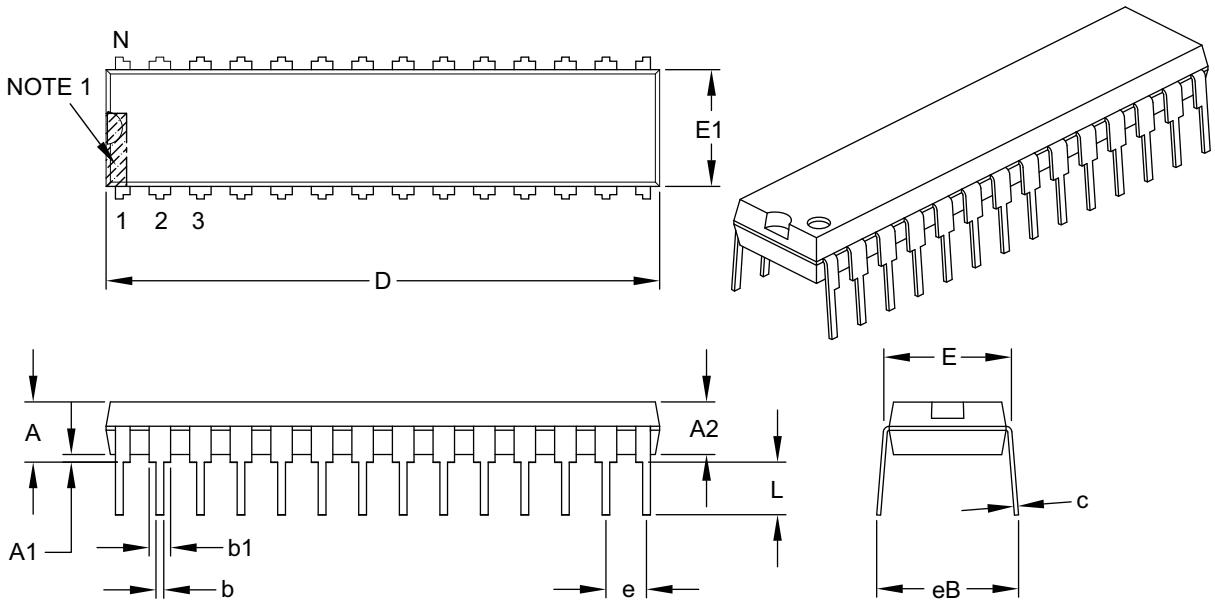



**FIGURE 32-8: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE**



### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B