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#### Details

Product Status	Active
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	21
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128b-v-ml">https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128b-v-ml</a>

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

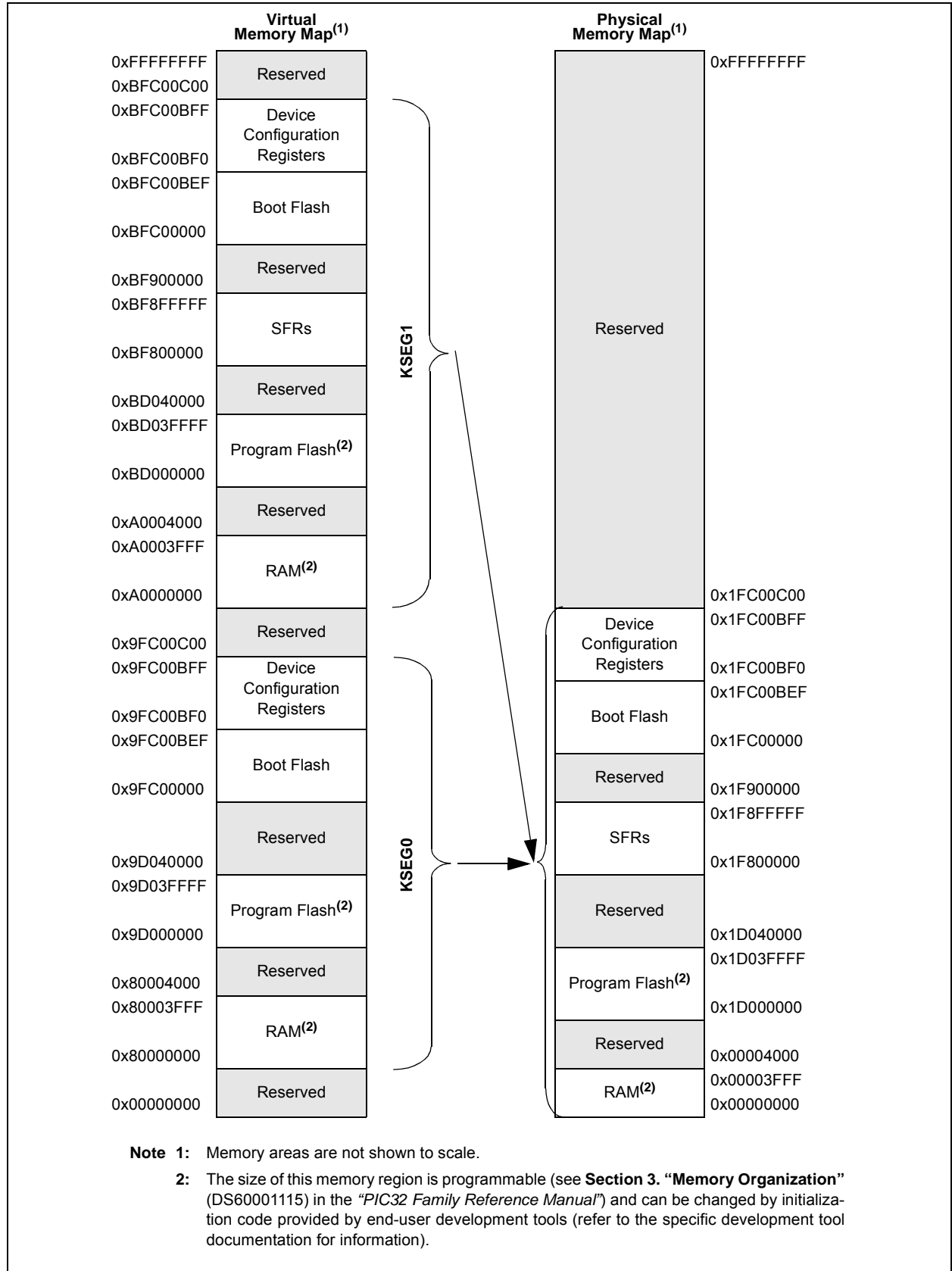
**TABLE 9: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES**

<b>44-PIN QFN (TOP VIEW)<sup>(1,2,3,5)</sup></b>  <b>PIC32MX110F016D</b> <b>PIC32MX120F032D</b> <b>PIC32MX130F064D</b> <b>PIC32MX130F256D</b> <b>PIC32MX150F128D</b> <b>PIC32MX170F256D</b>				44	1
Pin #	Full Pin Name	Pin #	Full Pin Name		
1	RPB9/SDA1/CTED4/PMD3/RB9	23	AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2		
2	RPC6/PMA1/RC6	24	AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3		
3	RPC7/PMA0/RC7	25	AN6/RPC0/RC0		
4	RPC8/PMA5/RC8	26	AN7/RPC1/RC1		
5	RPC9/CTED7/PMA6/RC9	27	AN8/RPC2/PMA2/RC2		
6	V <sub>SS</sub>	28	V <sub>DD</sub>		
7	V <sub>CAP</sub>	29	V <sub>SS</sub>		
8	PGED2/RPB10/CTED11/PMD2/RB10	30	OSC1/CLKI/RPA2/RA2		
9	PGEC2/RPB11/PMD1/RB11	31	OSC2/CLKO/RPA3/RA3		
10	AN12/PMD0/RB12	32	TDO/RPA8/PMA8/RA8		
11	AN11/RPB13/CTPLS/PMRD/RB13	33	SOSCI/RPB4/RB4		
12	PGED4 <sup>(4)</sup> /TMS/PMA10/RA10	34	SOSCO/RPA4/T1CK/CTED9/RA4		
13	PGEC4 <sup>(4)</sup> /TCK/CTED8/PMA7/RA7	35	TDI/RPA9/PMA9/RA9		
14	CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14	36	RPC3/RC3		
15	AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15	37	RPC4/PMA4/RC4		
16	AV <sub>SS</sub>	38	RPC5/PMA3/RC5		
17	AV <sub>DD</sub>	39	V <sub>SS</sub>		
18	MCLR	40	V <sub>DD</sub>		
19	VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0	41	PGED3/RPB5/PMD7/RB5		
20	VREF-/CVREF-/AN1/RPA1/CTED2/RA1	42	PGEC3/RPB6/PMD6/RB6		
21	PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0	43	RPB7/CTED3/PMD5/INT0/RB7		
22	PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1	44	RPB8/SCL1/CTED10/PMD4/RB8		

- Note**
- 1: The RPN pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 “Peripheral Pin Select”** for restrictions.
  - 2: Every I/O port pin (RAX-RCx) can be used as a change notification pin (CNAX-CNCx). See **Section 11.0 “I/O Ports”** for more information.
  - 3: The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to V<sub>SS</sub> externally.
  - 4: This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.
  - 5: Shaded pins are 5V tolerant.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**FIGURE 4-6: MEMORY MAP ON RESET FOR PIC32MX130/230 DEVICES (16 KB RAM, 256 KB FLASH)**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 6.0 RESETS

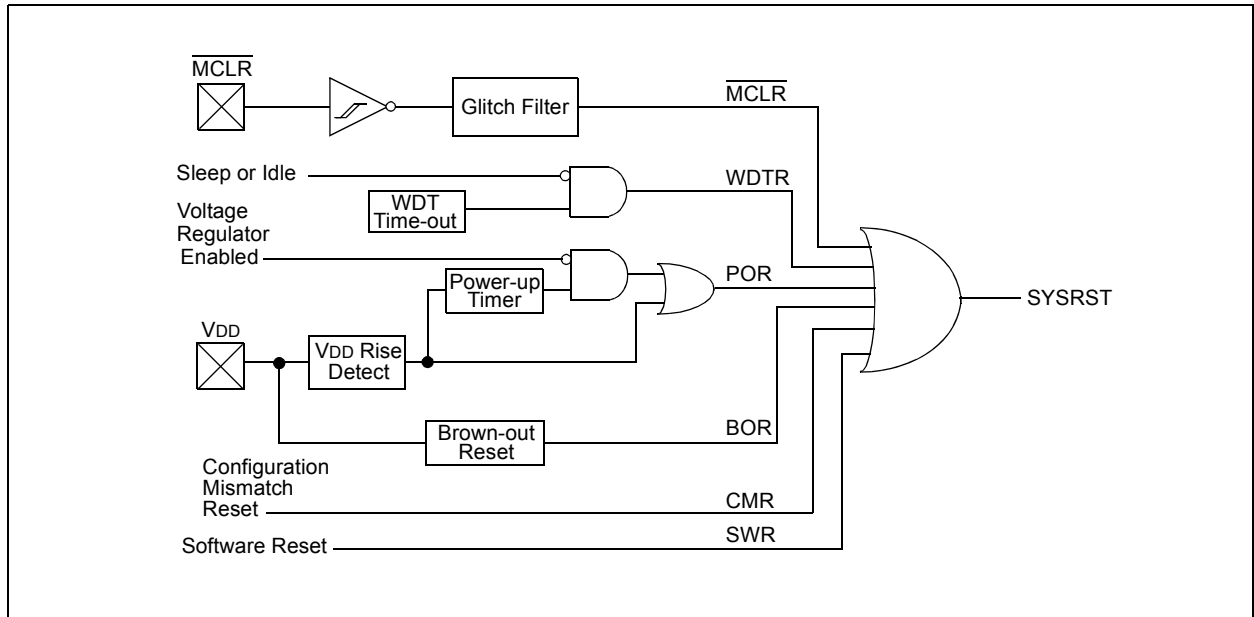
**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 7. “Resets”** (DS60001118), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- Power-on Reset (POR)
- Master Clear Reset pin ( $\overline{\text{MCLR}}$ )
- Software Reset (SWR)
- Watchdog Timer Reset (WDTR)
- Brown-out Reset (BOR)
- Configuration Mismatch Reset (CMR)

A simplified block diagram of the Reset module is illustrated in Figure 6-1.

**FIGURE 6-1: SYSTEM RESET BLOCK DIAGRAM**



# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 9-4: DCRCCON: DMA CRC CONTROL REGISTER (CONTINUED)

- bit 6     **CRCAPP:** CRC Append Mode bit<sup>(1)</sup>  
1 = The DMA transfers data from the source into the CRC but NOT to the destination. When a block transfer completes the DMA writes the calculated CRC value to the location given by CHxDSA  
0 = The DMA transfers data from the source through the CRC obeying WBO as it writes the data to the destination
- bit 5     **CRCTYP:** CRC Type Selection bit  
1 = The CRC module will calculate an IP header checksum  
0 = The CRC module will calculate a LFSR CRC
- bit 4-3   **Unimplemented:** Read as '0'
- bit 2-0   **CRCCH<2:0>:** CRC Channel Select bits  
111 = CRC is assigned to Channel 7  
110 = CRC is assigned to Channel 6  
101 = CRC is assigned to Channel 5  
100 = CRC is assigned to Channel 4  
011 = CRC is assigned to Channel 3  
010 = CRC is assigned to Channel 2  
001 = CRC is assigned to Channel 1  
000 = CRC is assigned to Channel 0

**Note 1:** When WBO = 1, unaligned transfers are not supported and the CRCAPP bit cannot be set.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 9-9: DCHxINT: DMA CHANNEL 'x' INTERRUPT CONTROL REGISTER (CONTINUED)

- bit 4      **CHDHIF:** Channel Destination Half Full Interrupt Flag bit  
1 = Channel Destination Pointer has reached midpoint of destination (CHDPTR = CHDSIZ/2)  
0 = No interrupt is pending
- bit 3      **CHBCIF:** Channel Block Transfer Complete Interrupt Flag bit  
1 = A block transfer has been completed (the larger of CHSSIZ/CHDSIZ bytes has been transferred), or a pattern match event occurs  
0 = No interrupt is pending
- bit 2      **CHCCIF:** Channel Cell Transfer Complete Interrupt Flag bit  
1 = A cell transfer has been completed (CHCSIZ bytes have been transferred)  
0 = No interrupt is pending
- bit 1      **CHTAIF:** Channel Transfer Abort Interrupt Flag bit  
1 = An interrupt matching CHAIRQ has been detected and the DMA transfer has been aborted  
0 = No interrupt is pending
- bit 0      **CHERIF:** Channel Address Error Interrupt Flag bit  
1 = A channel address error has been detected (either the source or the destination address is invalid)  
0 = No interrupt is pending

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 10-3: U1OTGSTAT: USB OTG STATUS REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R-0	U-0	R-0	U-0	R-0	R-0	U-0	R-0
	ID	—	LSTATE	—	SESVD	SESEND	—	VBUSVD

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **ID:** ID Pin State Indicator bit

1 = No cable is attached or a "type B" cable has been inserted into the USB receptacle

0 = A "type A" OTG cable has been inserted into the USB receptacle

bit 6 **Unimplemented:** Read as '0'

bit 5 **LSTATE:** Line State Stable Indicator bit

1 = USB line state (SE0 (U1CON<6>) bit and JSTATE (U1CON<7>)) bit has been stable for previous 1 ms

0 = USB line state (SE0 and JSTATE) has not been stable for previous 1 ms

bit 4 **Unimplemented:** Read as '0'

bit 3 **SESVD:** Session Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A or B device

0 = VBUS voltage is below Session Valid on the A or B device

bit 2 **SESEND:** B-Device Session End Indicator bit

1 = VBUS voltage is below Session Valid on the B device

0 = VBUS voltage is above Session Valid on the B device

bit 1 **Unimplemented:** Read as '0'

bit 0 **VBUSVD:** A-Device VBUS Valid Indicator bit

1 = VBUS voltage is above Session Valid on the A device

0 = VBUS voltage is below Session Valid on the A device

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CNT<7:0>							

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **CNT<7:0>:** SOF Threshold Value bits

Typical values of the threshold are:

01001010 = 64-byte packet

00101010 = 32-byte packet

00011010 = 16-byte packet

00010010 = 8-byte packet

**REGISTER 10-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
	BDTPTRL<15:9>							—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-1 **BDTPTRL<15:9>:** Buffer Descriptor Table Base Address bits

This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory.

The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 **Unimplemented:** Read as '0'

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 11.1 Parallel I/O (PIO) Ports

All port pins have 10 registers directly associated with their operation as digital I/O. The data direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx) read the latch. Writes to the latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx, and TRISx registers for data control, some port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs higher than VDD (e.g., 5V) on any desired 5V-tolerant pins by using external pull-up resistors. The maximum open-drain voltage allowed is the same as the maximum VIH specification.

See the “**Pin Diagrams**” section for the available pins and their functionality.

### 11.1.2 CONFIGURING ANALOG AND DIGITAL PORT PINS

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs must have their corresponding ANSEL and TRIS bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

If the TRIS bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or Comparator module.

When the PORT register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.1.3 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP.

### 11.1.4 INPUT CHANGE NOTIFICATION

The input change notification function of the I/O ports allows the PIC32MX1XX/2XX 28/36/44-pin Family devices to generate interrupt requests to the processor in response to a change-of-state on selected input pins. This feature can detect input change-of-states even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a change-of-state.

Five control registers are associated with the CN functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

The CNSTATx register indicates whether a change occurred on the corresponding pin since the last read of the PORTx bit.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push-button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

**Note:** Pull-ups and pull-downs on change notification pins should always be disabled when the port pin is configured as a digital output.

An additional control register (CNCONx) is shown in Register 11-3.

## 11.2 CLR, SET and INV Registers

Every I/O module register has a corresponding CLR (clear), SET (set) and INV (invert) register designed to provide fast atomic bit manipulations. As the name of the register implies, a value written to a SET, CLR or INV register effectively performs the implied operation, but only on the corresponding base register and only bits specified as '1' are modified. Bits specified as '0' are not modified.

Reading SET, CLR and INV registers returns undefined values. To see the effects of a write operation to a SET, CLR, or INV register, the base register must be read.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 11-1: [pin name]R: PERIPHERAL PIN SELECT INPUT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	[pin name]R<3:0>			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **[pin name]R<3:0>**: Peripheral Pin Select Input bits

Where [pin name] refers to the pins that are used to configure peripheral input mapping. See Table 11-1 for input pin selection values.

**Note:** Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

**REGISTER 11-2: RPnR: PERIPHERAL PIN SELECT OUTPUT REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RPnR<3:0>			

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3-0 **RPnR<3:0>**: Peripheral Pin Select Output bits

See Table 11-2 for output pin selection values.

**Note:** Register values can only be changed if the Configuration bit, IOLOCK (CFGCON<13>), = 0.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 12-1: T1CON: TYPE A TIMER CONTROL REGISTER**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	R/W-0	U-0	R/W-0	R/W-0	R-0	U-0	U-0	U-0
	ON <sup>(1)</sup>	—	SIDL	TWDIS	TWIP	—	—	—
7:0	R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	—	TCKPS<1:0>		—	TSYNC	TCS	—

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 31-16 **Unimplemented:** Read as '0'

bit 15 **ON:** Timer On bit<sup>(1)</sup>

1 = Timer is enabled

0 = Timer is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Discontinue module operation when the device enters Idle mode

0 = Continue module operation when the device enters Idle mode

bit 12 **TWDIS:** Asynchronous Timer Write Disable bit

1 = Writes to Timer1 are ignored until pending write operation completes

0 = Back-to-back writes are enabled (Legacy Asynchronous Timer functionality)

bit 11 **TWIP:** Asynchronous Timer Write in Progress bit

In Asynchronous Timer mode:

1 = Asynchronous write to the Timer1 register in progress

0 = Asynchronous write to Timer1 register is complete

In Synchronous Timer mode:

This bit is read as '0'.

bit 10-8 **Unimplemented:** Read as '0'

bit 7 **TGATE:** Timer Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **TCKPS<1:0>:** Timer Input Clock Prescale Select bits

11 = 1:256 prescale value

10 = 1:64 prescale value

01 = 1:8 prescale value

00 = 1:1 prescale value

**Note 1:** When using 1:1 PBCmLK divisor, the user's software should not read/write the peripheral SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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NOTES:

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 23.0 COMPARATOR

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 19. “Comparator”** (DS60001110), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site ([www.microchip.com/pic32](http://www.microchip.com/pic32)).

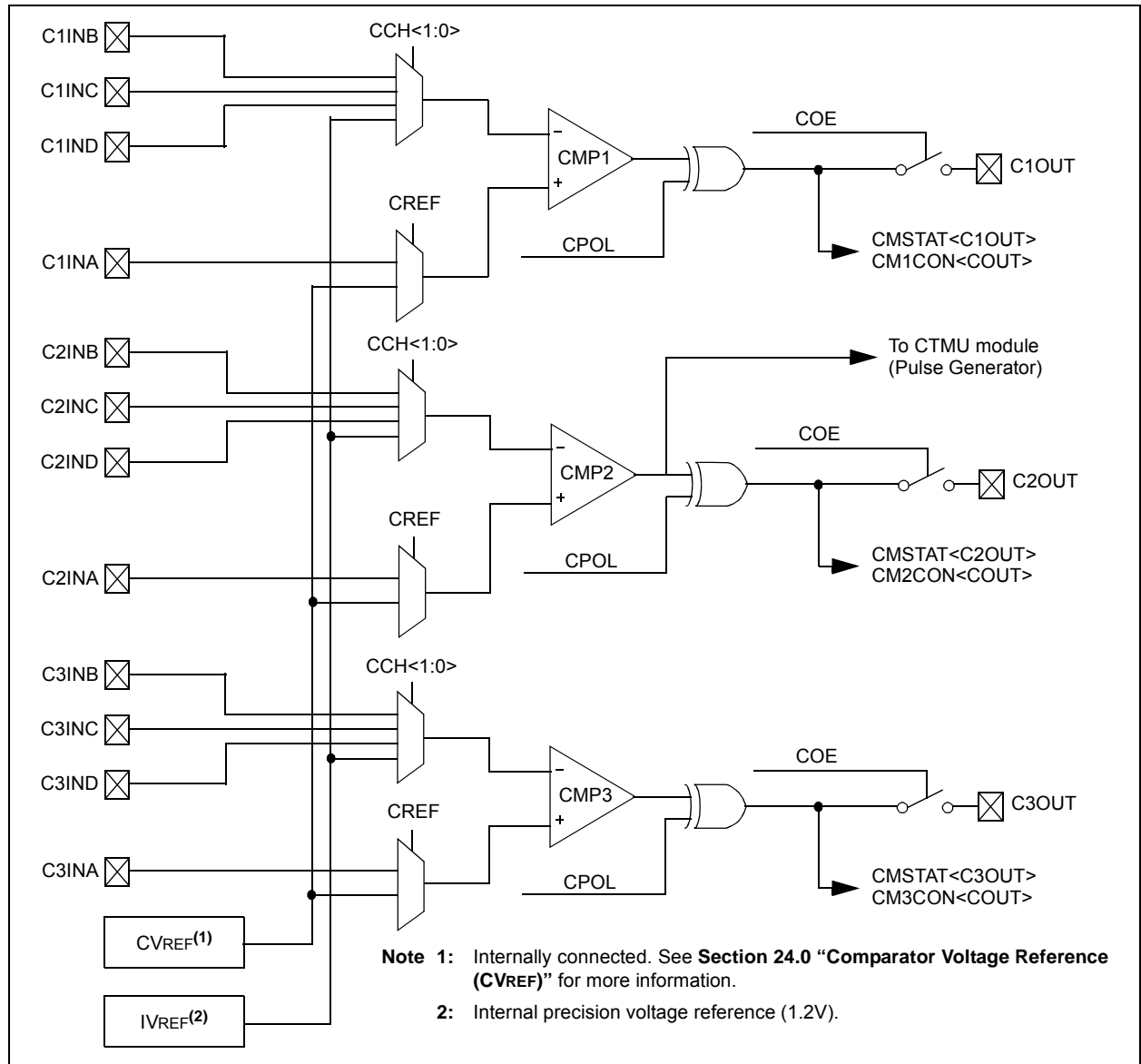
The Analog Comparator module contains three comparators that can be configured in a variety of ways.

Following are some of the key features of this module:

- Selectable inputs available include:
  - Analog inputs multiplexed with I/O pins
  - On-chip internal absolute voltage reference (IVREF)
  - Comparator voltage reference (CVREF)
- Outputs can be Inverted
- Selectable interrupt generation

A block diagram of the comparator module is provided in Figure 23-1.

**FIGURE 23-1: COMPARATOR BLOCK DIAGRAM**



## 23.1 Comparator Control Registers

TABLE 23-1: COMPARATOR REGISTER MAP

Virtual Address (BF80_#)	Register Name <sup>(1)</sup>	Bit Range	Bits																All Resets
			31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	
A000	CM1CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A010	CM2CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A020	CM3CON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	ON	COE	CPOL	—	—	—	—	COUT	EVPOL<1:0>		—	CREF	—	—	CCH<1:0>		00C3
A060	CMSTAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
		15:0	—	—	SIDL	—	—	—	—	—	—	—	—	—	—	C3OUT	C2OUT	C1OUT	0000

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 “CLR, SET and INV Registers” for more information.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

**REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —
23:16	r-1 —	r-1 —	r-1 —	r-1 —	r-1 —	R/P FPLLODIV<2:0>	R/P	R/P
15:8	R/P UPLLEN <sup>(1)</sup>	r-1 —	r-1 —	r-1 —	r-1 —	R/P UPLLDIV<2:0> <sup>(1)</sup>	R/P	R/P
7:0	r-1 —	R/P-1 FPLLMUL<2:0>	R/P	R/P-1	r-1 —	R/P FPLLDIV<2:0>	R/P	R/P

<b>Legend:</b>	r = Reserved bit	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits

111 = PLL output divided by 256  
 110 = PLL output divided by 64  
 101 = PLL output divided by 32  
 100 = PLL output divided by 16  
 011 = PLL output divided by 8  
 010 = PLL output divided by 4  
 001 = PLL output divided by 2  
 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit<sup>(1)</sup>  
 1 = Disable and bypass USB PLL  
 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLDIV<2:0>:** USB PLL Input Divider bits<sup>(1)</sup>

111 = 12x divider  
 110 = 10x divider  
 101 = 6x divider  
 100 = 5x divider  
 011 = 4x divider  
 010 = 3x divider  
 010 = 3x divider  
 001 = 2x divider  
 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits

111 = 24x multiplier  
 110 = 21x multiplier  
 101 = 20x multiplier  
 100 = 19x multiplier  
 011 = 18x multiplier  
 010 = 17x multiplier  
 001 = 16x multiplier  
 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

**Note 1:** This bit is only available on PIC32MX2XX devices.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

bit 2-0 **FPLLIDIV<2:0>**: PLL Input Divider bits

111 = 12x divider

110 = 10x divider

101 = 6x divider

100 = 5x divider

011 = 4x divider

010 = 3x divider

001 = 2x divider

000 = 1x divider

**Note 1:** This bit is only available on PIC32MX2XX devices.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## 29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for  
Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICKit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,  
Evaluation Kits and Starter Kits
- Third-party development tools

## 29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

## 31.0 50 MHz ELECTRICAL CHARACTERISTICS

This section provides an overview of the PIC32MX1XX/2XX 28/36/44-pin Family electrical characteristics for devices operating at 50 MHz.

The specifications for 50 MHz are identical to those shown in **Section 30.0 “Electrical Characteristics”**, with the exception of the parameters listed in this chapter.

Parameters in this chapter begin with the letter “M”, which denotes 50 MHz operation. For example, parameter DC29a in **Section 30.0 “Electrical Characteristics”**, is the up to 40 MHz operation equivalent for MDC29a.

Absolute maximum ratings for the PIC32MX1XX/2XX 28/36/44-pin Family 50 MHz devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias .....	-40°C to +85°C
Storage temperature .....	-65°C to +150°C
Voltage on VDD with respect to VSS .....	-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to VSS ( <b>Note 3</b> ) .....	-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 2.3V ( <b>Note 3</b> ) .....	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to VSS when VDD < 2.3V ( <b>Note 3</b> ) .....	-0.3V to +3.6V
Voltage on D+ or D- pin with respect to VUSB3V3 .....	-0.3V to (VUSB3V3 + 0.3V)
Voltage on VBUS with respect to VSS .....	-0.3V to +5.5V
Maximum current out of VSS pin(s) .....	300 mA
Maximum current into VDD pin(s) ( <b>Note 2</b> ) .....	300 mA
Maximum output current sunk by any I/O pin .....	15 mA
Maximum output current sourced by any I/O pin .....	15 mA
Maximum current sunk by all ports .....	200 mA
Maximum current sourced by all ports ( <b>Note 2</b> ) .....	200 mA

**Note 1:** Stresses above those listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

**3:** See the “**Pin Diagrams**” section for the 5V tolerant pins.

# PIC32MX1XX/2XX 28/36/44-PIN FAMILY

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## Revision J (April 2016)

This revision includes the following major changes as described in Table A-8, as well as minor updates to text and formatting, which were incorporated throughout the document.

**TABLE A-8: MAJOR SECTION UPDATES**

Section	Update Description
<b>“32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog”</b>	The PIC32MX270FDB device and Note 4 were added to <b>TABLE 2: “PIC32MX2XX 28/36/44-pin USB Family Features”</b> .
<b>2.0 “Guidelines for Getting Started with 32-bit MCUs”</b>	<b>EXAMPLE 2-1: “Crystal Load Capacitor Calculation”</b> was updated.
<b>30.0 “Electrical Characteristics”</b>	Parameter DO50a (Csosc) was removed from the Capacitive Loading Requirements on Output Pins AC Characteristics (see Table 30-16).
<b>“Product Identification System”</b>	The device mapping was updated to include type B for Software Targeting.

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