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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | MIPS32® M4K™ |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | I²C, IrDA, LINbus, PMP, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 3.6V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 36-VFTLA Exposed Pad |
| Supplier Device Package | 36-VTLA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128c-50i-tl |

**TABLE 5: PIN NAMES FOR 28-PIN GENERAL PURPOSE DEVICES**

**28-PIN QFN (TOP VIEW)(1,2,3.4)**

**PIC32MX110F016B**
**PIC32MX120F032B**
**PIC32MX130F064B**
**PIC32MX130F256B**
**PIC32MX150F128B**
**PIC32MX170F256B**

28 1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0 | 15 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1 | 16 | VSS |
| 3 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2 | 17 | VCAP |
| 4 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 | 18 | PGED2/RPB10/CTED11/PMD2/RB10 |
| 5 | VSS | 19 | PGEC2/TMS/RPB11/PMD1/RB11 |
| 6 | OSC1/CLKI/RPA2/RA2 | 20 | AN12/PMD0/RB12 |
| 7 | OSC2/CLKO/RPA3/PMA0/RA3 | 21 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 8 | SOSCI/RPB4/RB4 | 22 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14 |
| 9 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 23 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 10 | VDD | 24 | AVSS |
| 11 | PGED3/RPB5/PMD7/RB5 | 25 | AVDD |
| 12 | PGEC3/RPB6/PMD6/RB6 | 26 | $\overline{\text{MCLR}}$ |
| 13 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 27 | VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0 |
| 14 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 28 | VREF-/CVREF-/AN1/RPA1/CTED2/RA1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** Shaded pins are 5V tolerant.

**TABLE 7: PIN NAMES FOR 36-PIN GENERAL PURPOSE DEVICES**

**36-PIN VTLA (TOP VIEW)(1,2,3,5)**

**PIC32MX110F016C**
**PIC32MX120F032C**
**PIC32MX130F064C**
**PIC32MX150F128C**

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1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2 | 19 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 | 20 | RPC9/CTED7/RC9 |
| 3 | PGED4(4)/AN6/RPC0/RC0 | 21 | VSS |
| 4 | PGEC4(4)/AN7/RPC1/RC1 | 22 | VCAP |
| 5 | VDD | 23 | VDD |
| 6 | VSS | 24 | PGED2/RPB10/CTED11/PMD2/RB10 |
| 7 | OSC1/CLKI/RPA2/RA2 | 25 | PGEC2/TMS/RPB11/PMD1/RB11 |
| 8 | OSC2/CLKO/RPA3/PMA0/RA3 | 26 | AN12/PMD0/RB12 |
| 9 | SOSCI/RPB4/RB4 | 27 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 10 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 28 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14 |
| 11 | RPC3/RC3 | 29 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 12 | VSS | 30 | AVSS |
| 13 | VDD | 31 | AVDD |
| 14 | VDD | 32 | $\overline{\text{MCLR}}$ |
| 15 | PGED3/RPB5/PMD7/RB5 | 33 | VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0 |
| 16 | PGEC3/RPB6/PMD6/RB6 | 34 | VREF-/CVREF-/AN1/RPA1/CTED2/RA1 |
| 17 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 35 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0 |
| 18 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 36 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.
**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
**4:** This pin function is not available on PIC32MX110F016C and PIC32MX120F032C devices.
**5:** Shaded pins are 5V tolerant.

**TABLE 8: PIN NAMES FOR 36-PIN USB DEVICES**

**36-PIN VTLA (TOP VIEW)(1,2,3,5)**

**PIC32MX210F016C**
**PIC32MX220F032C**
**PIC32MX230F064C**
**PIC32MX250F128C**

36

1

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/PMD2/RB2 | 19 | TDO/RPB9/SDA1/CTED4/PMD3/RB9 |
| 2 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/PMWR/RB3 | 20 | RPC9/CTED7/RC9 |
| 3 | PGED4(4)/AN6/RPC0/RC0 | 21 | VSS |
| 4 | PGEC4(4)/AN7/RPC1/RC1 | 22 | VCAP |
| 5 | VDD | 23 | VDD |
| 6 | VSS | 24 | PGED2/RPB10/D+/CTED11/RB10 |
| 7 | OSC1/CLKI/RPA2/RA2 | 25 | PGEC2/RPB11/D-/RB11 |
| 8 | OSC2/CLKO/RPA3/PMA0/RA3 | 26 | VUSB3V3 |
| 9 | SOSCI/RPB4/RB4 | 27 | AN11/RPB13/CTPLS/PMRD/RB13 |
| 10 | SOSCO/RPA4/T1CK/CTED9/PMA1/RA4 | 28 | CVREFOUT/AN10/C3INB/RPB14/VBUSON/SCK1/CTED5/RB14 |
| 11 | AN12/RPC3/RC3 | 29 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 |
| 12 | VSS | 30 | AVSS |
| 13 | VDD | 31 | AVDD |
| 14 | VDD | 32 | $\overline{\text{MCLR}}$ |
| 15 | TMS/RPB5/USBID/RB5 | 33 | PGED3/VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/PMD7/RA0 |
| 16 | VBUS | 34 | PGEC3/VREF-/CVREF-/AN1/RPA1/CTED2/PMD6/RA1 |
| 17 | TDI/RPB7/CTED3/PMD5/INT0/RB7 | 35 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/PMD0/RB0 |
| 18 | TCK/RPB8/SCL1/CTED10/PMD4/RB8 | 36 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/PMD1/RB1 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.

**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

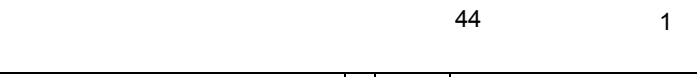
**4:** This pin function is not available on PIC32MX210F016C and PIC32MX120F032C devices.

**5:** Shaded pins are 5V tolerant.

**TABLE 9: PIN NAMES FOR 44-PIN GENERAL PURPOSE DEVICES**

**44-PIN QFN (TOP VIEW)(1,2,3,5)**

**PIC32MX110F016D**
**PIC32MX120F032D**
**PIC32MX130F064D**
**PIC32MX130F256D**
**PIC32MX150F128D**
**PIC32MX170F256D**




| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| 1 | RPB9/SDA1/CTED4/PMD3/RB9 | 23 | AN4/C1INB/C2IND/RPB2/SDA2/CTED13/RB2 |
| 2 | RPC6/PMA1/RC6 | 24 | AN5/C1INA/C2INC/RTCC/RPB3/SCL2/RB3 |
| 3 | RPC7/PMA0/RC7 | 25 | AN6/RPC0/RC0 |
| 4 | RPC8/PMA5/RC8 | 26 | AN7/RPC1/RC1 |
| 5 | RPC9/CTED7/PMA6/RC9 | 27 | AN8/RPC2/PMA2/RC2 |
| 6 | VSS | 28 | VDD |
| 7 | VCAP | 29 | VSS |
| 8 | PGED2/RPB10/CTED11/PMD2/RB10 | 30 | OSC1/CLKI/RPA2/RA2 |
| 9 | PGEC2/RPB11/PMD1/RB11 | 31 | OSC2/CLKO/RPA3/RA3 |
| 10 | AN12/PMD0/RB12 | 32 | TDO/RPA8/PMA8/RA8 |
| 11 | AN11/RPB13/CTPLS/PMRD/RB13 | 33 | SOSCI/RPB4/RB4 |
| 12 | PGED4(4)/TMS/PMA10/RA10 | 34 | SOSCO/RPA4/T1CK/CTED9/RA4 |
| 13 | PGEC4(4)/TCK/CTED8/PMA7/RA7 | 35 | TDI/RPA9/PMA9/RA9 |
| 14 | CVREFOUT/AN10/C3INB/RPB14/SCK1/CTED5/PMWR/RB14 | 36 | RPC3/RC3 |
| 15 | AN9/C3INA/RPB15/SCK2/CTED6/PMCS1/RB15 | 37 | RPC4/PMA4/RC4 |
| 16 | AVSS | 38 | RPC5/PMA3/RC5 |
| 17 | AVDD | 39 | VSS |
| 18 | $\overline{\text{MCLR}}$ | 40 | VDD |
| 19 | VREF+/CVREF+/AN0/C3INC/RPA0/CTED1/RA0 | 41 | PGED3/RPB5/PMD7/RB5 |
| 20 | VREF-/CVREF-/AN1/RPA1/CTED2/RA1 | 42 | PGEC3/RPB6/PMD6/RB6 |
| 21 | PGED1/AN2/C1IND/C2INB/C3IND/RPB0/RB0 | 43 | RPB7/CTED3/PMD5/INT0/RB7 |
| 22 | PGEC1/AN3/C1INC/C2INA/RPB1/CTED12/RB1 | 44 | RPB8/SCL1/CTED10/PMD4/RB8 |

**Note 1:** The RPn pins can be used by remappable peripherals. See Table 1 for the available peripherals and **Section 11.3 "Peripheral Pin Select"** for restrictions.
**2:** Every I/O port pin (RAx-RCx) can be used as a change notification pin (CNAx-CNCx). See **Section 11.0 "I/O Ports"** for more information.
**3:** The metal plane at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.
**4:** This pin function is not available on PIC32MX110F016D and PIC32MX120F032D devices.
**5:** Shaded pins are 5V tolerant.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number(1) | | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | 28-pin QFN | 28-pin SSOP/ SPDIP/ SOIC | 36-pin VTLA | 44-pin QFN/ TQFP/ VTLA | | | |
| PMA0 | 7 | 10 | 8 | 3 | I/O | TTL/ST | Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes) |
| PMA1 | 9 | 12 | 10 | 2 | I/O | TTL/ST | Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes) |
| PMA2 | | — | — | 27 | O | — | Parallel Master Port address (Demultiplexed Master modes) |
| PMA3 | | — | — | 38 | O | — | |
| PMA4 | | — | — | 37 | O | — | |
| PMA5 | | — | — | 4 | O | — | |
| PMA6 | | — | — | 5 | O | — | |
| PMA7 | | — | — | 13 | O | — | |
| PMA8 | | — | — | 32 | O | — | |
| PMA9 | | — | — | 35 | O | — | |
| PMA10 | | — | — | 12 | O | — | |
| PMCS1 | 23 | 26 | 29 | 15 | O | — | Parallel Master Port Chip Select 1 strobe |
| PMD0 | 20(2) | 23(2) | 26(2) | 10(2) | I/O | TTL/ST | Parallel Master Port data (Demultiplexed Master mode) or address/data (Multiplexed Master modes) |
| | 1(3) | 4(3) | 35(3) | 21(3) | | | |
| PMD1 | 19(2) | 22(2) | 25(2) | 9(2) | I/O | TTL/ST | |
| | 2(3) | 5(3) | 36(3) | 22(3) | | | |
| PMD2 | 18(2) | 21(2) | 24(2) | 8(2) | I/O | TTL/ST | |
| | 3(3) | 6(3) | 1(3) | 23(3) | | | |
| PMD3 | 15 | 18 | 19 | 1 | I/O | TTL/ST | |
| PMD4 | 14 | 17 | 18 | 44 | I/O | TTL/ST | |
| PMD5 | 13 | 16 | 17 | 43 | I/O | TTL/ST | |
| PMD6 | 12(2) | 15(2) | 16(2) | 42(2) | I/O | TTL/ST | |
| | 28(3) | 3(3) | 34(3) | 20(3) | | | |
| PMD7 | 11(2) | 14(2) | 15(2) | 41(2) | I/O | TTL/ST | |
| | 27(3) | 2(3) | 33(3) | 19(3) | | | |
| PMRD | 21 | 24 | 27 | 11 | O | — | Parallel Master Port read strobe |
| PMWR | 22(2) | 25(2) | 28(2) | 14(2) | O | — | Parallel Master Port write strobe |
| | 4(3) | 7(3) | 2(3) | 24(3) | | | |
| VBUS | 12(3) | 15(3) | 16(3) | 42(3) | I | Analog | USB bus power monitor |
| VUSB3V3 | 20(3) | 23(3) | 26(3) | 10(3) | P | — | USB internal transceiver supply. This pin must be connected to VDD. |
| VBUSON | 22(3) | 25(3) | 28(3) | 14(3) | O | — | USB Host and OTG bus power control output |
| D+ | 18(3) | 21(3) | 24(3) | 8(3) | I/O | Analog | USB D+ |
| D- | 19(3) | 22(3) | 25(3) | 9(3) | I/O | Analog | USB D- |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
TTL = TTL input buffer; PPS = Peripheral Pin Select; — = N/A

**Note 1:** Pin numbers are provided for reference only. See the **"Pin Diagrams"** section for device pin availability.

**2:** Pin number for PIC32MX1XX devices only.

**3:** Pin number for PIC32MX2XX devices only.

**REGISTER 4-5: BMXDRMSZ: DATA RAM SIZE REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<31:24> | | | | | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<23:16> | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<15:8> | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | BMXDRMSZ<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-0 **BMXDRMSZ<31:0>:** Data RAM Memory (DRM) Size bits
Static value that indicates the size of the Data RAM in bytes:
0x00001000 = Device has 4 KB RAM
0x00002000 = Device has 8 KB RAM
0x00004000 = Device has 16 KB RAM
0x00008000 = Device has 32 KB RAM
0x00010000 = Device has 64 KB RAM

**REGISTER 4-6: BMXPUPBA: PROGRAM FLASH (PFM) USER PROGRAM BASE ADDRESS REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | — | — | — | — | BMXPUPBA<19:16> | | | |
| 15:8 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<15:8> | | | | | | | |
| 7:0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| | BMXPUPBA<7:0> | | | | | | | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

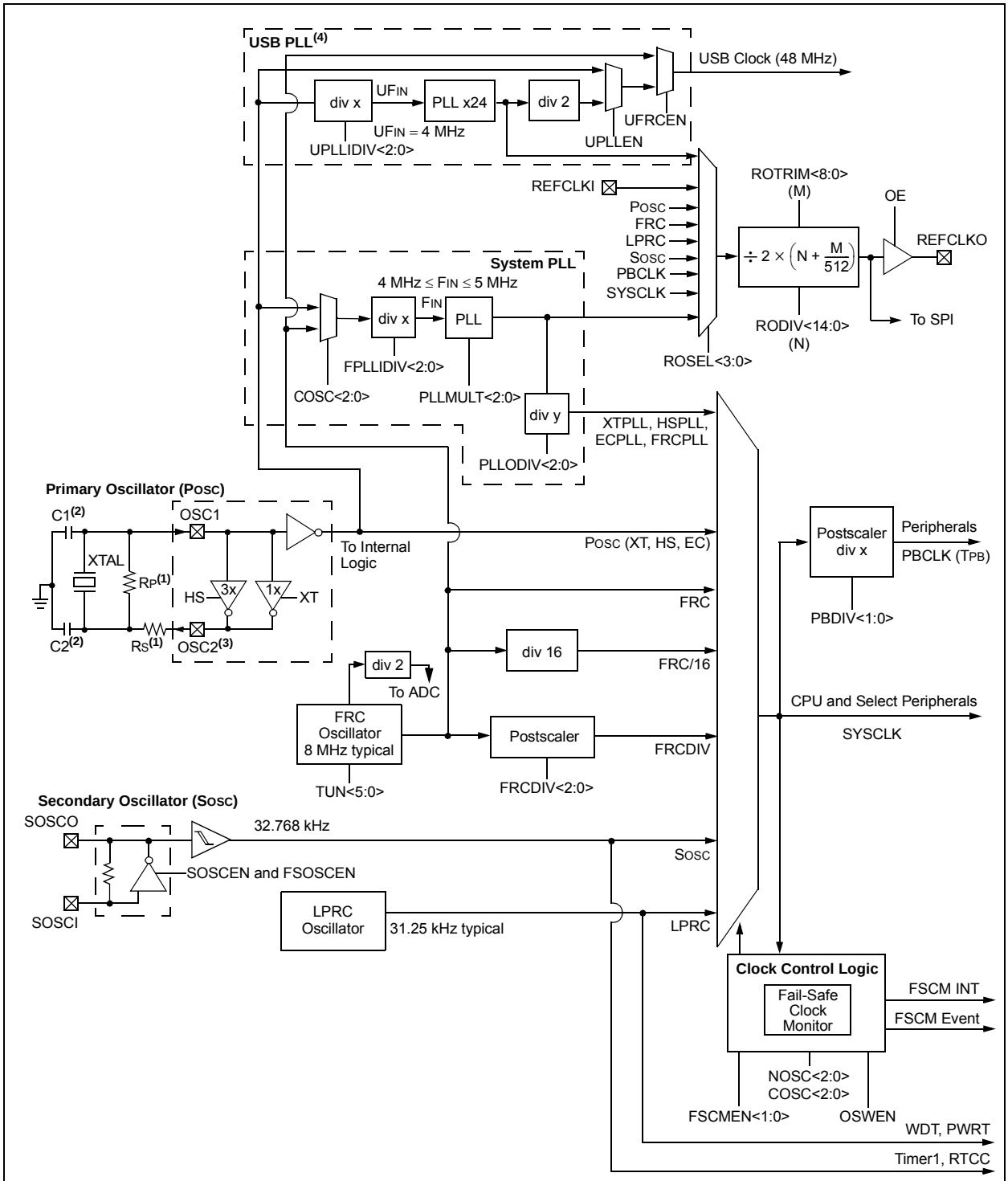
bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **BMXPUPBA<19:11>:** Program Flash (PFM) User Program Base Address bits

bit 10-0 **BMXPUPBA<10:0>:** Read-Only bits
This value is always '0', which forces 2 KB increments

**Note 1:** At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.
**2:** The value in this register must be less than or equal to BMXPFMSZ.

**FIGURE 8-1: OSCILLATOR DIAGRAM**




**Notes:**
1. A series resistor, RS, may be required for AT strip cut crystals or eliminate clipping. Alternately, to increase oscillator circuit gain, add a parallel resistor, RP, with a value of 1 MΩ.
2. Refer to **Section 6. "Oscillator Configuration"** (DS60001112) in the "*PIC32 Family Reference Manual*" for help in determining the best oscillator components.
3. The PBCLK out is only available on the OSC2 pin in certain clock modes.
4. The USB PLL is only available on PIC32MX2XX devices.

**REGISTER 10-11: U1CON: USB CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 23:16 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 15:8 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | — | — | — | — | — | — | — | — |
| 7:0 | R-x | R-x | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | JSTATE | SE0 | PKTDIS(4) / TOKBUSY(1,5) | USBRST | HOSTEN(2) | RESUME(3) | PPBRST | USBEN(4) / SOFEN(5) |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-8 **Unimplemented:** Read as '0'

bit 7 **JSTATE:** Live Differential Receiver JSTATE flag bit
1 = JSTATE was detected on the USB
0 = No JSTATE was detected

bit 6 **SE0:** Live Single-Ended Zero flag bit
1 = Single-Ended Zero was detected on the USB
0 = No Single-Ended Zero was detected

bit 5 **PKTDIS:** Packet Transfer Disable bit(4)
1 = Token and packet processing is disabled (set upon SETUP token received)
0 = Token and packet processing is enabled

**TOKBUSY:** Token Busy Indicator bit(1,5)
1 = Token is being executed by the USB module
0 = No token is being executed

bit 4 **USBRST:** Module Reset bit(5)
1 = USB reset generated
0 = USB reset terminated

bit 3 **HOSTEN:** Host Mode Enable bit(2)
1 = USB host capability is enabled
0 = USB host capability is disabled

bit 2 **RESUME:** RESUME Signaling Enable bit(3)
1 = RESUME signaling is activated
0 = RESUME signaling is disabled

**Note 1:** Software is required to check this bit before issuing another token command to the U1TOK register (see Register 10-15).

**2:** All host control logic is reset any time that the value of this bit is toggled.

**3:** Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB module will append a Low-Speed EOP to the RESUME signaling when this bit is cleared.

**4:** Device mode.

**5:** Host mode.

**TABLE 11-7: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP (CONTINUED)**

| Virtual Address (BF80_#) | Register Name | Bit Range | Bits | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| FB4C | RPB8R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB8<3:0> | | | | 0000 |
| FB50 | RPB9R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB9<3:0> | | | | 0000 |
| FB54 | RPB10R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB10<3:0> | | | | 0000 |
| FB58 | RPB11R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB11<3:0> | | | | 0000 |
| FB60 | RPB13R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB13<3:0> | | | | 0000 |
| FB64 | RPB14R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB14<3:0> | | | | 0000 |
| FB68 | RPB15R | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPB15<3:0> | | | | 0000 |
| FB6C | RPC0R(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC0<3:0> | | | | 0000 |
| FB70 | RPC1R(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC1<3:0> | | | | 0000 |
| FB74 | RPC2R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC2<3:0> | | | | 0000 |
| FB78 | RPC3R(3) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC3<3:0> | | | | 0000 |
| FB7C | RPC4R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC4<3:0> | | | | 0000 |
| FB80 | RPC5R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC5<3:0> | | | | 0000 |
| FB84 | RPC6R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC6<3:0> | | | | 0000 |
| FB88 | RPC7R(1) | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | — | — | — | — | RPC7<3:0> | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This register is only available on 44-pin devices.
**2:** This register is only available on PIC32MX1XX devices.
**3:** This register is only available on 36-pin and 44-pin devices.

## 18.1 I2C Control Registers

**TABLE 18-1: I2C1 AND I2C2 REGISTER MAP**

| Virtual Address (BF80_#) | Register Name(1) | Bit Range | Bits | | | | | | | | | | | | | | | | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 31/15 | 30/14 | 29/13 | 28/12 | 27/11 | 26/10 | 25/9 | 24/8 | 23/7 | 22/6 | 21/5 | 20/4 | 19/3 | 18/2 | 17/1 | 16/0 | |
| 5000 | I2C1CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5010 | I2C1STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| 5020 | I2C1ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 |
| 5030 | I2C1MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Mask Register | | | | | | | | | | 0000 |
| 5040 | I2C1BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5050 | I2C1TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5060 | I2C1RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |
| 5100 | I2C2CON | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ON | — | SIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| 5110 | I2C2STAT | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| 5120 | I2C2ADD | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Register | | | | | | | | | | 0000 |
| 5130 | I2C2MSK | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | Address Mask Register | | | | | | | | | | 0000 |
| 5140 | I2C2BRG | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | Baud Rate Generator Register | | | | | | | | | | | | 0000 |
| 5150 | I2C2TRN | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Transmit Register | | | | | | | | 0000 |
| 5160 | I2C2RCV | 31:16 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| | | 15:0 | — | — | — | — | — | — | — | — | Receive Register | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** All registers in this table except I2CxRCV have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See **Section 11.2 "CLR, SET and INV Registers"** for more information.

**REGISTER 21-1: RTCCON: RTC CONTROL REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
| | — | — | — | — | — | — | CAL<9:8> | |
| 23:16 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| | CAL<7:0> | | | | | | | |
| 15:8 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| | ON(1,2) | — | SIDL | — | — | — | — | — |
| 7:0 | R/W-0 | R-0 | U-0 | U-0 | R/W-0 | R-0 | R-0 | R/W-0 |
| | RTSECSEL(3) | RTCCLKON | — | — | RTCWREN(4) | RTCSYNC | HALFSEC(5) | RTCOE |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-26 **Unimplemented:** Read as '0'

bit 25-16 **CAL<9:0>:** RTC Drift Calibration bits, which contain a signed 10-bit integer value

0111111111 = Maximum positive adjustment, adds 511 RTC clock pulses every one minute
•
•
•
0000000001 = Minimum positive adjustment, adds 1 RTC clock pulse every one minute
0000000000 = No adjustment
1111111111 = Minimum negative adjustment, subtracts 1 RTC clock pulse every one minute
•
•
•
1000000000 = Maximum negative adjustment, subtracts 512 clock pulses every one minute

bit 15 **ON:** RTCC On bit(1,2)

1 = RTCC module is enabled
0 = RTCC module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SIDL:** Stop in Idle Mode bit

1 = Disables the PBCLK to the RTCC when the device enters Idle mode
0 = Continue normal operation when the device enters Idle mode

bit 12-8 **Unimplemented:** Read as '0'

bit 7 **RTSECSEL:** RTCC Seconds Clock Output Select bit(3)

1 = RTCC Seconds Clock is selected for the RTCC pin
0 = RTCC Alarm Pulse is selected for the RTCC pin

bit 6 **RTCCLKON:** RTCC Clock Enable Status bit

1 = RTCC Clock is actively running
0 = RTCC Clock is not running

**Note 1:** The ON bit is only writable when RTCWREN = 1.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

**4:** The RTCWREN bit can be set only when the write sequence is enabled.

**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

**Note:** This register is reset only on a Power-on Reset (POR).

**REGISTER 21-1: RTCCON: RTC CONTROL REGISTER (CONTINUED)**

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **RTCWREN:** RTC Value Registers Write Enable bit(4)
- 1 = RTC Value registers can be written to by the user
- 0 = RTC Value registers are locked out from being written to by the user

bit 2 **RTCSYNC:** RTCC Value Registers Read Synchronization bit
- 1 = RTC Value registers can change while reading, due to a rollover ripple that results in an invalid data read If the register is read twice and results in the same data, the data can be assumed to be valid
- 0 = RTC Value registers can be read without concern about a rollover ripple

bit 1 **HALFSEC:** Half-Second Status bit(5)
- 1 = Second half period of a second
- 0 = First half period of a second

bit 0 **RTCOE:** RTCC Output Enable bit
- 1 = RTCC clock output enabled – clock presented onto an I/O
- 0 = RTCC clock output disabled

**Note 1:** The ON bit is only writable when RTCWREN = 1.

**2:** When using the 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

**3:** Requires RTCOE = 1 (RTCCON<0>) for the output to be active.

**4:** The RTCWREN bit can be set only when the write sequence is enabled.

**5:** This bit is read-only. It is cleared to '0' on a write to the seconds bit fields (RTCTIME<14:8>).

| **Note:** | This register is reset only on a Power-on Reset (POR). |
|---|---|

## 25.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

**Note:** This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 37. "Charge Time Measurement Unit (CTMU)"** (DS60001167), which is available from the *Documentation > Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

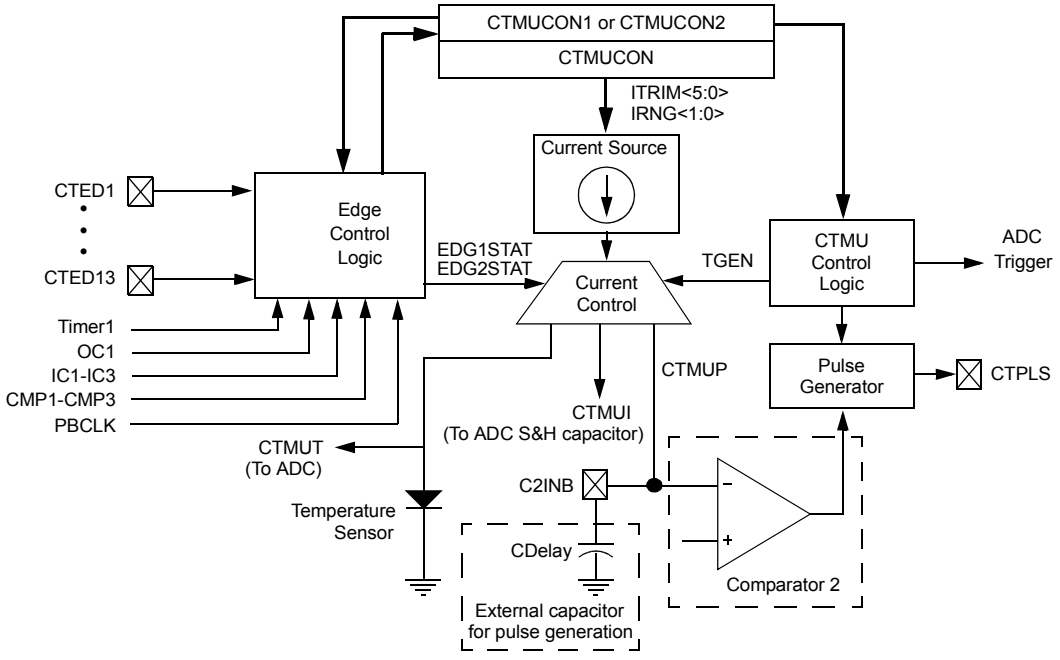
The Charge Time Measurement Unit (CTMU) is a flexible analog module that has a configurable current source with a digital configuration circuit built around it. The CTMU can be used for differential time measurement between pulse sources and can be used for generating an asynchronous pulse. By working with other on-chip analog modules, the CTMU can be used for high resolution time measurement, measure capacitance, measure relative changes in capacitance or generate output pulses with a specific time delay. The CTMU is ideal for interfacing with capacitive-based sensors.

The CTMU module includes the following key features:

- Up to 13 channels available for capacitive or time measurement input
- On-chip precision current source
- 16-edge input trigger sources
- Selection of edge or level-sensitive inputs
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- High precision time measurement
- Time delay of external or internal signal asynchronous to system clock
- Integrated temperature sensing diode
- Control of current source during auto-sampling
- Four current source ranges
- Time measurement resolution of one nanosecond

A block diagram of the CTMU is shown in Figure 25-1.

**FIGURE 25-1: CTMU BLOCK DIAGRAM**




| Current Control Selection | TGEN | EDG1STAT, EDG2STAT |
|---|---|---|
| CTMUT | 0 | EDG1STAT = EDG2STAT |
| CTMUI | 0 | EDG1STAT ≠ EDG2STAT |
| CTMUP | 1 | EDG1STAT ≠ EDG2STAT |
| No Connect | 1 | EDG1STAT = EDG2STAT |

**NOTES:**

The processor will exit, or 'wake-up', from Sleep on one of the following events:

- On any interrupt from an enabled source that is operating in Sleep. The interrupt priority must be greater than the current CPU priority.
- On any form of device Reset
- On a WDT time-out

If the interrupt priority is lower than or equal to the current priority, the CPU will remain Halted, but the PBCLK will start running and the device will enter into Idle mode.

### 26.3.2 IDLE MODE

In Idle mode, the CPU is Halted but the System Clock (SYSCLK) source is still enabled. This allows peripherals to continue operation when the CPU is Halted. Peripherals can be individually configured to Halt when entering Idle by setting their respective SIDL bit. Latency, when exiting Idle mode, is very low due to the CPU oscillator source remaining active.

**Note 1:** Changing the PBCLK divider ratio requires recalculation of peripheral timing. For example, assume the UART is configured for 9600 baud with a PB clock ratio of 1:1 and a POSC of 8 MHz. When the PB clock divisor of 1:2 is used, the input frequency to the baud clock is cut in half; therefore, the baud rate is reduced to 1/2 its former value. Due to numeric truncation in calculations (such as the baud rate divisor), the actual baud rate may be a tiny percentage different than expected. For this reason, any timing calculation required for a peripheral should be performed with the new PB clock frequency instead of scaling the previous value based on a change in the PB divisor ratio.

**2:** Oscillator start-up and PLL lock delays are applied when switching to a clock source that was disabled and that uses a crystal and/or the PLL. For example, assume the clock source is switched from POSC to LPRC just prior to entering Sleep in order to save power. No oscillator start-up delay would be applied when exiting Idle. However, when switching back to POSC, the appropriate PLL and/or oscillator start-up/lock delays would be applied.

The device enters Idle mode when the SLPEN (OSCCON<4>) bit is clear and a `WAIT` instruction is executed.

The processor will wake or exit from Idle mode on the following events:

- On any interrupt event for which the interrupt source is enabled. The priority of the interrupt event must be greater than the current priority of the CPU. If the priority of the interrupt event is lower than or equal to current priority of the CPU, the CPU will remain Halted and the device will remain in Idle mode.
- On any form of device Reset
- On a WDT time-out interrupt

### 26.3.3 PERIPHERAL BUS SCALING METHOD

Most of the peripherals on the device are clocked using the PBCLK. The Peripheral Bus can be scaled relative to the SYSCLK to minimize the dynamic power consumed by the peripherals. The PBCLK divisor is controlled by PBDIV<1:0> (OSCCON<20:19>), allowing SYSCLK to PBCLK ratios of 1:1, 1:2, 1:4 and 1:8. All peripherals using PBCLK are affected when the divisor is changed. Peripherals such as the USB, Interrupt Controller, DMA, and the bus matrix are clocked directly from SYSCLK. As a result, they are not affected by PBCLK divisor changes.

Changing the PBCLK divisor affects:

- The CPU to peripheral access latency. The CPU has to wait for next PBCLK edge for a read to complete. In 1:8 mode, this results in a latency of one to seven SYSCLKs.
- The power consumption of the peripherals. Power consumption is directly proportional to the frequency at which the peripherals are clocked. The greater the divisor, the lower the power consumed by the peripherals.

To minimize dynamic power, the PB divisor should be chosen to run the peripherals at the lowest frequency that provides acceptable system performance. When selecting a PBCLK divider, peripheral clock requirements, such as baud rate accuracy, should be taken into account. For example, the UART peripheral may not be able to achieve all baud rate values at some PBCLK divider depending on the SYSCLK value.

**REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 | r-1 |
| | — | — | — | — | — | — | — | — |
| 23:16 | r-1 | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | — | — | — | — | — | FPLLODIV<2:0> | | |
| 15:8 | R/P | r-1 | r-1 | r-1 | r-1 | R/P | R/P | R/P |
| | UPLLEN(1) | — | — | — | — | UPLLIDIV<2:0>(1) | | |
| 7:0 | r-1 | R/P-1 | R/P | R/P-1 | r-1 | R/P | R/P | R/P |
| | — | FPLLMUL<2:0> | | | — | FPLLIDIV<2:0> | | |

| Legend: | r = Reserved bit | P = Programmable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-19 **Reserved:** Write '1'

bit 18-16 **FPLLODIV<2:0>:** Default PLL Output Divisor bits
- 111 = PLL output divided by 256
- 110 = PLL output divided by 64
- 101 = PLL output divided by 32
- 100 = PLL output divided by 16
- 011 = PLL output divided by 8
- 010 = PLL output divided by 4
- 001 = PLL output divided by 2
- 000 = PLL output divided by 1

bit 15 **UPLLEN:** USB PLL Enable bit(1)
- 1 = Disable and bypass USB PLL
- 0 = Enable USB PLL

bit 14-11 **Reserved:** Write '1'

bit 10-8 **UPLLIDIV<2:0>:** USB PLL Input Divider bits(1)
- 111 = 12x divider
- 110 = 10x divider
- 101 = 6x divider
- 100 = 5x divider
- 011 = 4x divider
- 010 = 3x divider
- 010 = 3x divider
- 001 = 2x divider
- 000 = 1x divider

bit 7 **Reserved:** Write '1'

bit 6-4 **FPLLMUL<2:0>:** PLL Multiplier bits
- 111 = 24x multiplier
- 110 = 21x multiplier
- 101 = 20x multiplier
- 100 = 19x multiplier
- 011 = 18x multiplier
- 010 = 17x multiplier
- 001 = 16x multiplier
- 000 = 15x multiplier

bit 3 **Reserved:** Write '1'

**Note 1:** This bit is only available on PIC32MX2XX devices.

**REGISTER 27-6: DEVID: DEVICE AND REVISION ID REGISTER**

| Bit Range | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|
| 31:24 | R | R | R | R | R | R | R | R |
| | VER<3:0>(1) | | | | DEVID<27:24>(1) | | | |
| 23:16 | R | R | R | R | R | R | R | R |
| | DEVID<23:16>(1) | | | | | | | |
| 15:8 | R | R | R | R | R | R | R | R |
| | DEVID<15:8>(1) | | | | | | | |
| 7:0 | R | R | R | R | R | R | R | R |
| | DEVID<7:0>(1) | | | | | | | |

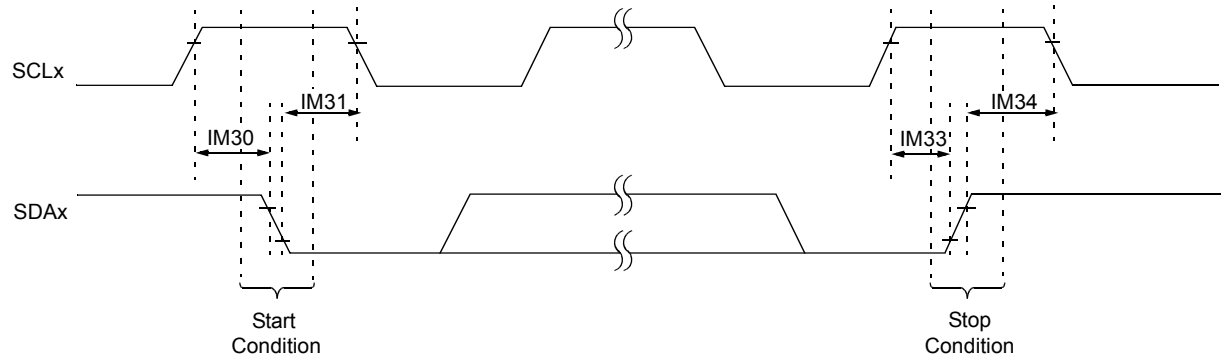
| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 31-28 **VER<3:0>:** Revision Identifier bits(1)

bit 27-0 **DEVID<27:0>:** Device ID bits(1)

**Note 1:** See the *"PIC32 Flash Programming Specification"* (DS60001145) for a list of Revision and Device ID values.

**FIGURE 30-14: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 30-1 for load conditions.

**FIGURE 30-15: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**

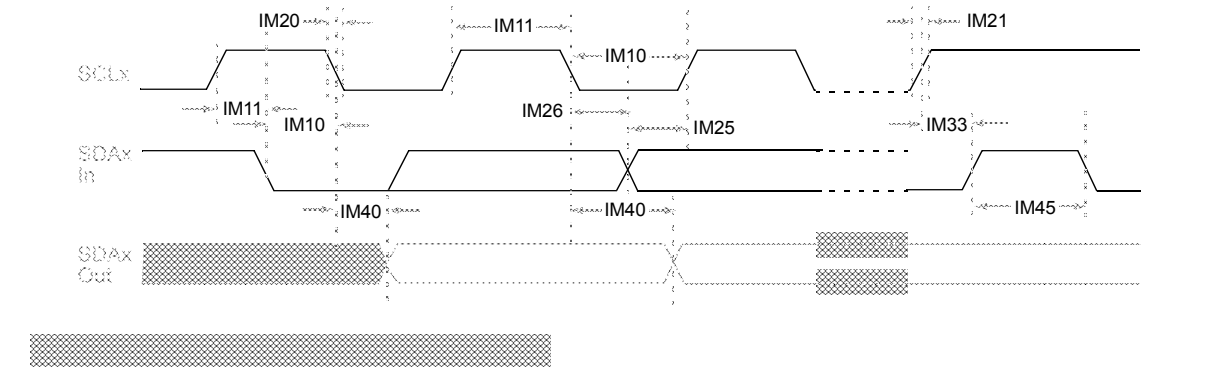


**TABLE 30-39: PARALLEL MASTER PORT WRITE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| PM11 | TWR | PMWR Pulse Width | — | 1 TPB | — | — | — |
| PM12 | TDVSU | Data Out Valid before PMWR or PMENB goes Inactive (data setup time) | — | 2 TPB | — | — | — |
| PM13 | TDVHOLD | PMWR or PMEMB Invalid to Data Out Invalid (data hold time) | — | 1 TPB | — | — | — |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

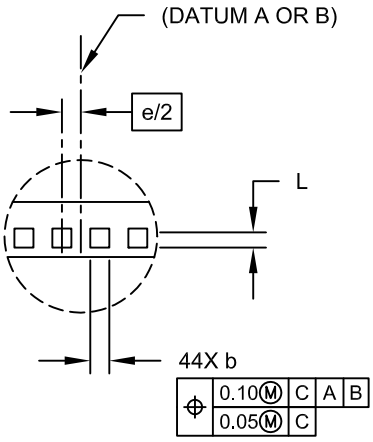
**TABLE 30-40: OTG ELECTRICAL SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +105°C for V-temp | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| USB313 | VUSB3V3 | USB Voltage | 3.0 | — | 3.6 | V | Voltage on VUSB3V3 must be in this range for proper USB operation |
| USB315 | VILUSB | Input Low Voltage for USB Buffer | — | — | 0.8 | V | — |
| USB316 | VIHUSB | Input High Voltage for USB Buffer | 2.0 | — | — | V | — |
| USB318 | VDIFS | Differential Input Sensitivity | — | — | 0.2 | V | The difference between D+ and D- must exceed this value while VCM is met |
| USB319 | VCM | Differential Common Mode Range | 0.8 | — | 2.5 | V | — |
| USB320 | ZOUT | Driver Output Impedance | 28.0 | — | 44.0 | Ω | — |
| USB321 | VOL | Voltage Output Low | 0.0 | — | 0.3 | V | 1.425 kΩ load connected to VUSB3V3 |
| USB322 | VOH | Voltage Output High | 2.8 | — | 3.6 | V | 1.425 kΩ load connected to ground |

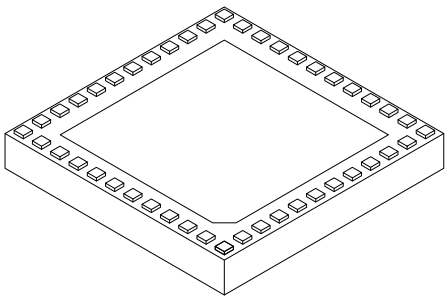
**Note 1:** These parameters are characterized, but not tested in manufacturing.

### 44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension | Limits | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Number of Pins per Side | ND | | 12 | |
| Number of Pins per Side | NE | | 10 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.025 | - | 0.075 |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 4.40 | 4.55 | 4.70 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 4.40 | 4.55 | 4.70 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157C Sheet 2 of 2