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Details

Product Status	Obsolete
Core Processor	MIPS32® M4K™
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, PMP, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	25
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	· ·
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	36-VFTLA Exposed Pad
Supplier Device Package	36-VTLA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic32mx150f128c-v-tl

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		Pin Nu	mber ⁽¹⁾				
Pin Name	28-pin QFN	28-pin SSOP/ SPDIP/ SOIC	36-pin VTLA	44-pin QFN/ TQFP/ VTLA	Pin Type	Buffer Type	Description
PMA0	7	10	8	3	I/O	TTL/ST	Parallel Master Port Address bit 0 input (Buffered Slave modes) and output (Master modes)
PMA1	9	12	10	2	I/O	TTL/ST	Parallel Master Port Address bit 1 input (Buffered Slave modes) and output (Master modes)
PMA2		_	_	27	0	_	Parallel Master Port address
PMA3				38	0	—	(Demultiplexed Master modes)
PMA4				37	0	—	
PMA5		_	_	4	0	_	
PMA6		_	_	5	0	_	
PMA7				13	0	—	
PMA8		_	_	32	0	_	
PMA9		_	_	35	0	_	
PMA10		_	_	12	0	_	
PMCS1	23	26	29	15	0	_	Parallel Master Port Chip Select 1 strobe
	20 ⁽²⁾	23 ⁽²⁾	26 ⁽²⁾	10 ⁽²⁾	1/0	TTI /CT	Parallel Master Port data (Demultiplexed
	1 ⁽³⁾	4 ⁽³⁾	35 ⁽³⁾	21 ⁽³⁾	1/0	111/31	Master mode) or address/data
	19 (2)	22 ⁽²⁾	25 ⁽²⁾	9(2)	1/0	TTI /CT	(Multiplexed Master modes)
	2 ⁽³⁾	5 ⁽³⁾	36 ⁽³⁾	22 ⁽³⁾	1/0	111/31	
	18 ⁽²⁾	21 ⁽²⁾	24 ⁽²⁾	8 ⁽²⁾	1/0	TTI /ST	
	3(3)	6 ⁽³⁾	1 ⁽³⁾	23 ⁽³⁾	1/0	116/01	
PMD3	15	18	19	1	I/O	TTL/ST	
PMD4	14	17	18	44	I/O	TTL/ST	
PMD5	13	16	17	43	I/O	TTL/ST	
PMD6	12 ⁽²⁾	15 ⁽²⁾	16 ⁽²⁾	42 ⁽²⁾	1/0	TTI /CT	1
	28 ⁽³⁾	3(3)	34 (3)	20 ⁽³⁾	1/0	111/31	
PMD7	11(2)	14 ⁽²⁾	15 (2)	41 ⁽²⁾	1/0	TTI /ST	
	27 ⁽³⁾	2 ⁽³⁾	33 (3)	19 ⁽³⁾	1/0	112/01	
PMRD	21	24	27	11	0	—	Parallel Master Port read strobe
	22 ⁽²⁾	25 ⁽²⁾	28 ⁽²⁾	14 ⁽²⁾	0		Parallel Master Port write strope
	4 ⁽³⁾	7 ⁽³⁾	2 ⁽³⁾	24 ⁽³⁾	Ŭ		T arallel master Fort while strobe
VBUS	12 ⁽³⁾	15 ⁽³⁾	16 (3)	42 ⁽³⁾	Ι	Analog	USB bus power monitor
VUSB3V3	20 ⁽³⁾	23 ⁽³⁾	26 ⁽³⁾	10 ⁽³⁾	Р	_	USB internal transceiver supply. This pin must be connected to VDD.
VBUSON	22 ⁽³⁾	25 ⁽³⁾	28 ⁽³⁾	14 ⁽³⁾	0		USB Host and OTG bus power control output
D+	18 ⁽³⁾	21 ⁽³⁾	24 ⁽³⁾	8 ⁽³⁾	I/O	Analog	USB D+
D-	19 ⁽³⁾	22 ⁽³⁾	25 ⁽³⁾	9(3)	I/O	Analog	USB D-
Legend:	CMOS = C	MOS compa	atible input	or output		Analog =	Analog input P = Power
	ST = Schmi	tt Trigger in	put with CN	NOS levels		O = Outp	but I=Input
	L = L	nput buffer				PPS = P	eripheral Pin Select — = N/A

Note 1: Pin numbers are provided for reference only. See the "Pin Diagrams" section for device pin availability.

2: Pin number for PIC32MX1XX devices only.

3: Pin number for PIC32MX2XX devices only.

4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source.For detailed information, refer to **Section 3.** "Memory Organization" (DS60001115), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers provide 4 GB unified virtual memory address space. All memory regions, including program, data memory, Special Function Registers (SFRs), and Configuration registers, reside in this address space at their respective unique addresses. The program and data memories can be optionally partitioned into user and kernel memories. In addition, the data memory can be made executable, allowing PIC32MX1XX/2XX 28/36/44-pin Family devices to execute from data memory.

Key features include:

- 32-bit native data width
- Separate User (KUSEG) and Kernel (KSEG0/KSEG1) mode address space
- · Flexible program Flash memory partitioning
- Flexible data RAM partitioning for data and program space
- Separate boot Flash memory for protected code
- Robust bus exception handling to intercept runaway code
- Simple memory mapping with Fixed Mapping Translation (FMT) unit
- Cacheable (KSEG0) and non-cacheable (KSEG1) address regions

4.1 PIC32MX1XX/2XX 28/36/44-pin Family Memory Layout

PIC32MX1XX/2XX 28/36/44-pin Family microcontrollers implement two address schemes: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions as well as access peripherals. Physical addresses are used by bus master peripherals, such as DMA and the Flash controller, that access memory independently of the CPU.

The memory maps for the PIC32MX1XX/2XX 28/36/44-pin Family devices are illustrated in Figure 4-1 through Figure 4-6.

Table 4-1 provides SFR memory map details.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	
04.04	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
31:24	_	—	_	—	_	—	—	—	
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
23:10	—	—	_	—	_	—	—	—	
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	
15:8	BMXDUDBA<15:8>								
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	
7:0				BMXDU	DBA<7:0>				

REGISTER 4-3: BMXDUDBA: DATA RAM USER DATA BASE ADDRESS REGISTER

Legend:

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUDBA<15:10>: DRM User Data Base Address bits

When non-zero, the value selects the relative base address for User mode data space in RAM, the value must be greater than BMXDKPBA.

bit 9-0 BMXDUDBA<9:0>: Read-Only bits This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	—	—	_	—	—		—	—
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	_	—	—	—	—	—
45.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0
15:8				BMXDU	PBA<15:8>			
7.0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
7:0				BMXDU	PBA<7:0>			

REGISTER 4-4: BMXDUPBA: DATA RAM USER PROGRAM BASE ADDRESS REGISTER

Legend:

Logona.			
R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

bit 15-10 BMXDUPBA<15:10>: DRM User Program Base Address bits

When non-zero, the value selects the relative base address for User mode program space in RAM, BMXDUPBA must be greater than BMXDUDBA.

bit 9-0 **BMXDUPBA<9:0>:** Read-Only bits This value is always '0', which forces 1 KB increments

Note 1: At Reset, the value in this register is forced to zero, which causes all of the RAM to be allocated to Kernal mode data usage.

2: The value in this register must be less than or equal to BMXDRMSZ.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
24.24	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
31.24	_	_	_		IP03<2:0>			<1:0>
22.16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23.10	—	—	—		IP02<2:0>			<1:0>
15.9	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15.0	—	—	—		IP01<2:0>			<1:0>
7.0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0		_		IP00<2:0>			IS00-	<1:0>

REGISTER 7-6: IPCx: INTERRUPT PRIORITY CONTROL REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, rea	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 31-29 Unimplemented: Read as '0'
- bit 28-26 IP03<2:0>: Interrupt Priority bits
- 111 = Interrupt priority is 7 010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled bit 25-24 IS03<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0 bit 23-21 Unimplemented: Read as '0' bit 20-18 IP02<2:0>: Interrupt Priority bits 111 = Interrupt priority is 7 010 = Interrupt priority is 2 001 = Interrupt priority is 1 000 = Interrupt is disabled bit 17-16 IS02<1:0>: Interrupt Subpriority bits 11 = Interrupt subpriority is 3 10 = Interrupt subpriority is 2 01 = Interrupt subpriority is 1 00 = Interrupt subpriority is 0 bit 15-13 Unimplemented: Read as '0' bit 12-10 IP01<2:0>: Interrupt Priority bits 111 = Interrupt priority is 7 010 = Interrupt priority is 2 001 = Interrupt priority is 1
 - 000 = Interrupt is disabled
- **Note:** This register represents a generic definition of the IPCx register. Refer to Table 7-1 for the exact bit definitions.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
51.24	—	—	—	—	—	—	—	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	—	—	—	—	—	—	—	—
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—	—	—	—	—	—
7.0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7.0				CNT	<7:0>			

REGISTER 10-16: U1SOF: USB SOF THRESHOLD REGISTER

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

- bit 7-0 CNT<7:0>: SOF Threshold Value bits Typical values of the threshold are:

 - 01001010 = 64-byte packet 00101010 = **32-byte packet**
 - 00011010 = **16-byte packet**
 - 00010010 = 8-byte packet

REGISTER 10-17: U1BDTP1: USB BUFFER DESCRIPTOR TABLE PAGE 1 REGISTER

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	-	-	-	-	_
22:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—					_
15.0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
15.0	—	—	—				-	_
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
7.0			B	DTPTRL<15:9)>			_

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ad as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 Unimplemented: Read as '0'

bit 7-1 BDTPTRL<15:9>: Buffer Descriptor Table Base Address bits This 7-bit value provides address bits 15 through 9 of the Buffer Descriptor Table base address, which defines the starting location of the Buffer Descriptor Table in system memory. The 32-bit Buffer Descriptor Table base address is 512-byte aligned.

bit 0 Unimplemented: Read as '0'

11.0 I/O PORTS

Note: This data sheet summarizes the features of the PIC32MX1XX/2XX 28/36/44-pin Family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to Section 12. "I/O Ports" (DS60001120), which is available from the *Documentation* > *Reference Manual* section of the Microchip PIC32 web site (www.microchip.com/pic32).

General purpose I/O pins are the simplest of peripherals. They allow the PIC[®] MCU to monitor and control other devices. To add flexibility and functionality, some pins are multiplexed with alternate functions. These functions depend on which peripheral features are on the device. In general, when a peripheral is functioning, that pin may not be used as a general purpose I/O pin.

Key features of this module include:

- · Individual output pin open-drain enable/disable
- Individual input pin weak pull-up and pull-down
- Monitor selective inputs and generate interrupt when change in pin state is detected
- Operation during Sleep and Idle modes
- Fast bit manipulation using CLR, SET, and INV registers

Figure 11-1 illustrates a block diagram of a typical multiplexed I/O port.



15.1 **Input Capture Control Registers**

AB	LE 15-1:	IN	PUT CA	PTURE	E 1-INPU		URE 5	REGIST	ER MA	2							
ess		<u>í</u>								Bi	ts						
Virtual Addr (BF80_#)	Register Name	Bit Range	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1
2000		31:16				—	—	_	—						—		—
2000	IC ICON.	15:0	ON		SIDL	_	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2010	IC1BUF	31:16 15:0								IC1BUF	<31:0>						
2200	10000N(1)	31:16	_	_	_	—	—	_	—	—	_	_	-	_	—	—	_
	1020011	15:0	ON		SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2210	IC2BUF	31:16 15:0								IC2BUF	<31:0>						
2400		31:16	—	—	_	_	_	—	_	—	_	—	_	—	_	—	_
2400	IC3CON /	15:0	ON	_	SIDL	—	—	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2410	IC3BUF	31:16 15:0								IC3BUF	<31:0>						
2600		31:16	_		_	-	-	-	—	—	_				—	—	_
2000	1040011	15:0	ON	—	SIDL	—	—	—	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2610	IC4BUF	31:16 15:0	IC4BUF<31:0>														
2800		31:16	_		_	-	-	-	—	—	_				—	—	—
2000	1000010	15:0	ON	_	SIDL	—	_	_	FEDGE	C32	ICTMR	ICI<	1:0>	ICOV	ICBNE		ICM<2:0
2810	IC5BUF	31:16 15:0								IC5BUF	<31:0>						

T

Legend:

This register has corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information. Note 1:

All Resets

0000

0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx 0000 0000 xxxx xxxx

16/0

—

REGISTER 15-1: ICXCON: INPUT CAPTURE 'x' CONTROL REGISTER (CONTINUED)

ICM<2:0>: Input Capture Mode Select bits

bit 2-0

- 111 = Interrupt-Only mode (only supported while in Sleep mode or Idle mode)
- 110 = Simple Capture Event mode every edge, specified edge first and every edge thereafter
- 101 = Prescaled Capture Event mode every sixteenth rising edge
- 100 = Prescaled Capture Event mode every fourth rising edge
- 011 = Simple Capture Event mode every rising edge
- 010 = Simple Capture Event mode every falling edge
- 001 = Edge Detect mode every edge (rising and falling)
- 000 = Input Capture module is disabled
- **Note 1:** When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

REGISTER 17-2: SPIxCON2: SPI CONTROL REGISTER 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
21.24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31.24	—	—	—	—	—	—	-	—
22.16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23.10	—	—	—	—	—	—	_	—
15.0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
10.0	SPISGNEXT	—	—	FRMERREN	SPIROVEN	SPITUREN	IGNROV	IGNTUR
7:0	R/W-0	U-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
7.0	AUDEN ⁽¹⁾	—	—	—	AUDMONO ^(1,2)	—	AUDMOD)<1:0> ^(1,2)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-16 Unimplemented: Read as '0'

- bit 15 SPISGNEXT: Sign Extend Read Data from the RX FIFO bit
 - 1 = Data from RX FIFO is sign extended
 - 0 = Data from RX FIFO is not sign extended
- bit 14-13 Unimplemented: Read as '0'
- bit 12 **FRMERREN:** Enable Interrupt Events via FRMERR bit
 - 1 = Frame Error overflow generates error events
 - 0 = Frame Error does not generate error events
- bit 11 SPIROVEN: Enable Interrupt Events via SPIROV bit
 - 1 = Receive overflow generates error events
 - 0 = Receive overflow does not generate error events
- bit 10 SPITUREN: Enable Interrupt Events via SPITUR bit
 - 1 = Transmit underrun generates error events
 - 0 = Transmit underrun does not generate error events
- bit 9 IGNROV: Ignore Receive Overflow bit (for Audio Data Transmissions)
 - 1 = A ROV is not a critical error; during ROV data in the FIFO is not overwritten by receive data
 0 = A ROV is a critical error that stops SPI operation
- bit 8 **IGNTUR:** Ignore Transmit Underrun bit (for Audio Data Transmissions)
 - 1 = A TUR is not a critical error and zeros are transmitted until the SPIxTXB is not empty
 - 0 = A TUR is a critical error that stops SPI operation
- bit 7 AUDEN: Enable Audio CODEC Support bit⁽¹⁾
- 1 = Audio protocol enabled
 - 0 = Audio protocol disabled
- bit 6-5 Unimplemented: Read as '0'
- bit 3 AUDMONO: Transmit Audio Data Format bit^(1,2)
 - 1 = Audio data is mono (Each data word is transmitted on both left and right channels)
 - 0 = Audio data is stereo
- bit 2 Unimplemented: Read as '0'
- bit 1-0 AUDMOD<1:0>: Audio Protocol Mode bit^(1,2)
 - 11 = PCM/DSP mode
 - 10 = Right-Justified mode
 - 01 = Left-Justified mode
 - $00 = I^2S \mod$
- **Note 1:** This bit can only be written when the ON bit = 0.
 - 2: This bit is only valid for AUDEN = 1.

FIGURE 18-1: I²C BLOCK DIAGRAM



23.1 Comparator Control Registers

TABLE 23-1: COMPARATOR REGISTER MAP

ess	Register Name ⁽¹⁾	0	Bits															6	
Virtual Addı (BF80_#		Bit Rang	31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0	All Reset
A000		31:16	—		_			_		—	_	—	—	—	—	—			0000
A000	CINTCON	15:0	ON	COE	CPOL	_	_	_	_	COUT	EVPO	L<1:0>	_	CREF	-	—	CCH	<1:0>	00C3
A010	CM2CON	31:16	_	_	_	_	_	_	_	_	_	_	—	—	—	—	_	_	0000
AUTU	CIVIZCON	15:0	ON	COE	CPOL	_	_	_	_	COUT	EVPO	L<1:0>	_	CREF	-	—	CCH	<1:0>	00C3
A020	CM3CON	31:16	_	_	_	_	_	_	_	_	_	_	—	—	—	—	_	_	0000
A020	CINISCON	15:0	ON	COE	CPOL	_	_	_	_	COUT	EVPO	L<1:0>	_	CREF	-	—	CCH	<1:0>	00C3
4060	CMSTAT	31:16	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	0000
A000	CIVISTAI	15:0	_	—	SIDL	—	—	_	—	-	—	—	—	—	—	C3OUT	C2OUT	C10UT	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: All registers in this table have corresponding CLR, SET and INV registers at their virtual addresses, plus offsets of 0x4, 0x8 and 0xC, respectively. See Section 11.2 "CLR, SET and INV Registers" for more information.

REGISTER 27-3: DEVCFG2: DEVICE CONFIGURATION WORD 2 (CONTINUED)

- bit 2-0 **FPLLIDIV<2:0>:** PLL Input Divider bits
 - 111 = 12x divider
 - 110 = 10x divider
 - 101 = 6x divider
 - 100 = 5x divider
 - 011 = 4x divider
 - 010 = 3x divider
 - 001 = 2x divider
 - 000 = 1x divider
- Note 1: This bit is only available on PIC32MX2XX devices.

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
31:24	_	_	_	—	_	_	_	_
00.40	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
23:10	_	—	—	—	—	—	_	—
45.0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
15:8	—	—	IOLOCK ⁽¹⁾	PMDLOCK ⁽¹⁾	—	—		_
7.0	U-0	U-0	U-0	U-0	R/W-1	U-0	U-1	R/W-1
7:0	—	_	_	_	JTAGEN	_		TDOEN

REGISTER 27-5: CFGCON: CONFIGURATION CONTROL REGISTER

Legend:

Logonan			
R = Readable bit	W = Writable bit	U = Unimplemented bit, re	ead as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-14 Unimplemented: Read as '0'

- bit 13 IOLOCK: Peripheral Pin Select Lock bit⁽¹⁾
 - 1 = Peripheral Pin Select is locked. Writes to PPS registers is not allowed.
 - 0 = Peripheral Pin Select is not locked. Writes to PPS registers is allowed.
- bit 12 PMDLOCK: Peripheral Module Disable bit⁽¹⁾
 - 1 = Peripheral module is locked. Writes to PMD registers is not allowed.
 - 0 = Peripheral module is not locked. Writes to PMD registers is allowed.

bit 11-4 Unimplemented: Read as '0'

- bit 3 JTAGEN: JTAG Port Enable bit
 - 1 = Enable the JTAG port
 - 0 = Disable the JTAG port
- bit 2-1 Unimplemented: Read as '1'
- bit 0 **TDOEN:** TDO Enable for 2-Wire JTAG bit
 - 1 = 2-wire JTAG protocol uses TDO
 - 0 = 2-wire JTAG protocol does not use TDO
- Note 1: To change this bit, the unlock sequence must be performed. Refer to Section 6. "Oscillator" (DS60001112) in the "PIC32 Family Reference Manual" for details.

TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHA	ARACTER	ISTICS	$\begin{array}{l} \mbox{Standard Operating Conditions: 2.3V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +105^{\circ}C \mbox{ for V-temp} \end{array}$						
Param. No.	Symbol	Characteristics	Min.	Тур.	Max.	Units	Conditions		
Operati	Operating Voltage								
DC10	Vdd	Supply Voltage (Note 2)	2.3		3.6	V	—		
DC12	Vdr	RAM Data Retention Voltage (Note 1)	1.75	_	—	V	—		
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	1.75	_	2.1	V	_		
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.00005	_	0.115	V/μs	_		

Note 1: This is the limit to which VDD can be lowered without losing RAM data.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested, but not characterized. All device Analog modules, such as ADC, etc., will function, but with degraded performance below VDDMIN. Refer to parameter BO10 in Table 30-11 for BOR values.





28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-052C Sheet 1 of 2

TABLE A-1:	MAJOR SECTION UPDATES	(CONTINUED)	
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Section	Update Description
29.0 "Electrical Characteristics"	Updated the Absolute Maximum Ratings (removed Voltage on VCORE with respect to Vss).
	Added the SPDIP specification to the Thermal Packaging Characteristics (see Table 29-2).
	Updated the Typical values for parameters DC20-DC24 in the Operating Current (IDD) specification (see Table 29-5).
	Updated the Typical values for parameters DC30a-DC34a in the Idle Current (IIDLE) specification (see Table 29-6).
	Updated the Typical values for parameters DC40i and DC40n and removed parameter DC40m in the Power-down Current (IPD) specification (see Table 29-7).
	Removed parameter D320 (VCORE) from the Internal Voltage Regulator Specifications and updated the Comments (see Table 29-13).
	Updated the Minimum, Typical, and Maximum values for parameter F20b in the Internal FRC Accuracy specification (see Table 29-17).
	Removed parameter SY01 (TPWRT) and removed all Conditions from Resets Timing (see Table 29-20).
	Updated all parameters in the CTMU Specifications (see Table 29-39).
31.0 "Packaging Information"	Added the 28-lead SPDIP package diagram information (see 31.1 "Package Marking Information" and 31.2 "Package Details").
"Product Identification System"	Added the SPDIP (SP) package definition.

Revision C (November 2011)

All major changes are referenced by their respective section in Table A-2.

TABLE A-2:	MAJOR SECTION UPDATES
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Section	Update Description
"32-bit Microcontrollers (up to 128 KB Flash and 32 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog"	Revised the source/sink on I/O pins (see "Input/Output" on page 1). Added the SPDIP package to the PIC32MX220F032B device in the PIC32MX2XX USB Family Features (see Table 2).
4.0 "Memory Organization"	Removed ANSB6 from the ANSELB register and added the ODCB6, ODCB10, and ODCB11 bits in the PORTB Register Map (see Table 4-20).
29.0 "Electrical Characteristics"	Updated the minimum value for parameter OS50 in the PLL Clock Timing Specifications (see Table 29-16).

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